# **Protected Power MOSFET**

# 2.6 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ ESD Protection

#### **Features**

- Diode Clamp Between Gate and Source
- ESD Protection Human Body Model 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher R<sub>DS(on)</sub>
- Internal Series Gate Resistance
- These are Pb-Free Devices

#### **Benefits**

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

### **Applications**

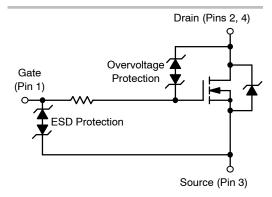
- Automotive and Industrial Markets:
   Solenoid Drivers, Lamp Drivers, Small Motor Drivers
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

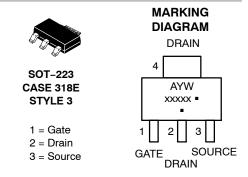


# ON Semiconductor®

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| V <sub>DSS</sub><br>(Clamped) | R <sub>DS(ON)</sub> TYP | I <sub>D</sub> MAX |  |
|-------------------------------|-------------------------|--------------------|--|
| 52 V                          | 95 mΩ @ 10 V            | 2.6 A              |  |





A = Assembly Location

/ = Year

W = Work Week xxxxx = V8440 or 8440A ■ Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

1

# $\textbf{MAXIMUM RATINGS} \ (T_J = 25^{\circ}C \ unless \ otherwise \ noted)$

| Rating   | Symbol  | Value      | Unit |
|--|---|------------|------|
| Drain-to-Source Voltage Internally Clamped   | $V_{DSS}$   | 52–59      | V    |
| Gate-to-Source Voltage - Continuous  | V <sub>GS</sub>   | ±15        | V    |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Single Pulse ( $t_p$ = 10 $\mu$ s) (Note 1)  | I <sub>D</sub>  | 2.6<br>10  | Α    |
| Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1)   | $P_{D}$   | 1.69       | W    |
| Operating and Storage Temperature Range  | T <sub>J</sub> , T <sub>stg</sub>                       | -55 to 150 | °C   |
| Single Pulse Drain-to–Source Avalanche Energy (V <sub>DD</sub> = 50 V, I <sub>D(pk)</sub> = 1.17 A, V <sub>GS</sub> = 10 V, L = 160 mH, R <sub>G</sub> = 25 $\Omega$ ) | E <sub>AS</sub>   | 110        | mJ   |
| Load Dump Voltage (V <sub>GS</sub> = 0 and 10 V, R <sub>I</sub> = $2.0~\Omega$ , R <sub>L</sub> = $9.0~\Omega$ , td = $400~ms$ )                                       | $V_{LD}$  | 60         | V    |
| Thermal Resistance,  Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)   | $egin{aligned} R_{	hetaJA} \ R_{	hetaJA} \end{aligned}$ | 74<br>169  | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds   | TL  | 260        | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in²).

2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in²).

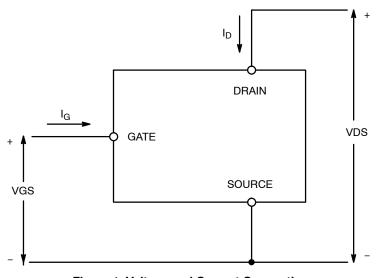


Figure 1. Voltage and Current Convention

# MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25$ °C unless otherwise noted)

| Characteristic  |  | Symbol               | Min        | Тур              | Max               | Unit            |
|---|--|----------------------|------------|------------------|-------------------|-----------------|
| OFF CHARACTERISTICS   |  |                      |            |                  |                   |                 |
| Drain-to-Source Breakdown Voltage (Note 3) ( $V_{GS} = 0 \text{ V, } I_D = 1.0 \text{ mA, } T_J = 25^{\circ}\text{C}$ ) ( $V_{GS} = 0 \text{ V, } I_D = 1.0 \text{ mA, } T_J = -40^{\circ}\text{C}$ to 125°C) (Note 4) Temperature Coefficient (Negative) |  | V <sub>(BR)DSS</sub> | 52<br>50.8 | 55<br>54<br>–9.3 | 59<br>59.5        | V<br>V<br>mV/°C |
| Zero Gate Voltage Drain Current $(V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V})$ $(V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C})$ (Note 4)   |  | I <sub>DSS</sub>     |            |                  | 10<br>25          | μΑ              |
| Gate-Body Leakage Current $(V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V})$ $(V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V})$  |  | I <sub>GSS</sub>     |            | ±35              | ±10               | μΑ              |
| ON CHARACTERISTICS (Note 3)   |  |                      |            |                  |                   |                 |
| Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 100 \mu A)$ Threshold Temperature Coefficient (Negative)   |  | V <sub>GS(th)</sub>  | 1.1        | 1.5<br>-4.1      | 1.9               | V<br>mV/°C      |
| Static Drain-to-Source On-Resistance (Note 3)   |  | R <sub>DS(on)</sub>  |            | 150<br>135<br>95 | 180<br>160<br>110 | mΩ              |
| Forward Transconductance (Note 3) (V  | <sub>OS</sub> = 15 V, I <sub>D</sub> = 2.6 A)                | 9FS                  |            | 3.8              |                   | Mhos            |
| DYNAMIC CHARACTERISTICS   |  |                      |            |                  |                   |                 |
| Input Capacitance   |  | C <sub>iss</sub>     |            | 155              |                   | pF              |
| Output Capacitance  | $V_{DS} = 35 \text{ V}, V_{GS} = 0 \text{ V},$<br>f = 10 kHz | C <sub>oss</sub>     |            | 60               |                   |                 |
| Transfer Capacitance  |  | C <sub>rss</sub>     |            | 25               |                   |                 |
| Input Capacitance   |  | C <sub>iss</sub>     |            | 170              |                   | pF              |
| Output Capacitance  | $V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$<br>f = 10 kHz | C <sub>oss</sub>     |            | 70               |                   |                 |
| Transfer Capacitance  |  | C <sub>rss</sub>     |            | 30               |                   |                 |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 3. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%.
- 4. Not subject to production testing.5. Switching characteristics are independent of operating junction temperatures.

#### MOSFET ELECTRICAL CHARACTERISTICS (T<sub>.I</sub> = 25°C unless otherwise noted)

| Charac                              | Symbol   | Min                 | Тур  | Max          | Unit |    |
|-------------------------------------|--|---------------------|------|--------------|------|----|
| SWITCHING CHARACTERISTICS (No       | ote 5)   |                     |      |              |      |    |
| Turn-On Delay Time                  |  | t <sub>d(on)</sub>  |      | 375          |      | ns |
| Rise Time                           | V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 40 V,   | t <sub>r</sub>      |      | 1525         |      |    |
| Turn-Off Delay Time                 | $I_D = 2.6 \text{ A}, R_D = 15.4 \Omega$   | t <sub>d(off)</sub> |      | 1530         |      |    |
| Fall Time                           | 7  | t <sub>f</sub>      |      | 1160         |      |    |
| Turn-On Delay Time                  |  | t <sub>d(on)</sub>  |      | 325          |      | ns |
| Rise Time                           | V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 40 V,   | t <sub>r</sub>      |      | 1275         |      |    |
| Turn-Off Delay Time                 | $I_D = 1.0 \text{ A}, R_D = 40 \Omega$   | t <sub>d(off)</sub> |      | 1860         |      |    |
| Fall Time                           | 7  | t <sub>f</sub>      |      | 1150         |      |    |
| Turn-On Delay Time                  |  | t <sub>d(on)</sub>  |      | 190          |      | ns |
| Rise Time                           | V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 15 V,  | t <sub>r</sub>      |      | 710          |      |    |
| Turn-Off Delay Time                 | $I_D = 2.6 \text{ A}, R_D = 5.8 \Omega$  | t <sub>d(off)</sub> |      | 2220         |      |    |
| Fall Time                           | 7  | t <sub>f</sub>      |      | 1180         |      |    |
| Gate Charge                         |  | Q <sub>T</sub>      |      | 4.5          |      | nC |
|                                     | $V_{GS} = 4.5 \text{ V}, V_{DS} = 40 \text{ V},$ $I_{D} = 2.6 \text{ A (Note 3)}$                      | Q <sub>1</sub>      |      | 0.9          |      |    |
|                                     |  | $Q_2$               |      | 2.6          |      |    |
| Gate Charge                         |  | Q <sub>T</sub>      |      | 3.9          |      | nC |
|                                     | $V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$<br>$I_{D} = 1.5 \text{ A} \text{ (Note 3)}$           | Q <sub>1</sub>      |      | 1.0          |      |    |
|                                     | 10 = 1.0 / (Note 6)  | Q <sub>2</sub>      |      | 1.7          |      |    |
| SOURCE-DRAIN DIODE CHARACTE         | RISTICS  |                     | •    |              |      |    |
| Forward On-Voltage                  | $I_S$ = 2.6 A, $V_{GS}$ = 0 V (Note 3)<br>$I_S$ = 2.6 A, $V_{GS}$ = 0 V, $T_J$ = 125°C                 | V <sub>SD</sub>     |      | 0.81<br>0.66 | 1.5  | V  |
| Reverse Recovery Time               |  | t <sub>rr</sub>     |      | 730          |      | ns |
|                                     | $I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V},$<br>$dI_S/dt = 100 \text{ A/}\mu\text{s} \text{ (Note 3)}$ | t <sub>a</sub>      |      | 200          |      | 1  |
|                                     | αιεταί - 100 / γμο (14010 0)   | t <sub>b</sub>      |      | 530          |      |    |
| Reverse Recovery Stored Charge      |  | Q <sub>RR</sub>     |      | 6.3          |      | μC |
| ESD CHARACTERISTICS (Note 4)        |  | •                   |      |              |      |    |
| Electro-Static Discharge Capability | Human Body Model (HBM)   | ESD                 | 5000 |              |      | V  |
|                                     | -  | 4                   | -    |              |      |    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 3. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%.
- 4. Not subject to production testing.
- 5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL PERFORMANCE CURVES**

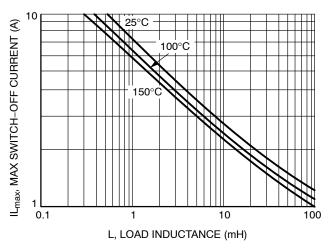


Figure 1. Single Pulse Maximum Switch-off Current vs. Load Inductance

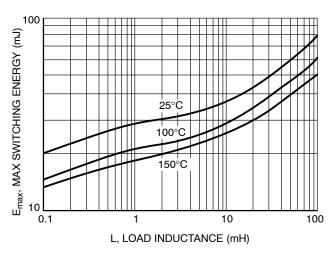
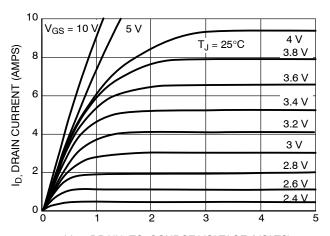
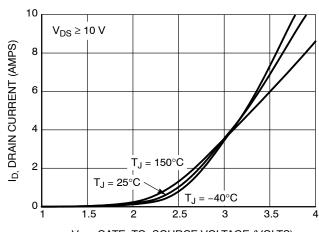


Figure 2. Single Pulse Maximum Switching Energy vs. Load Inductance



V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (VOLTS)



 $V_{GS}$ , GATE-TO-SOURCE VOLTAGE (VOLTS) Figure 4. Transfer Characteristics



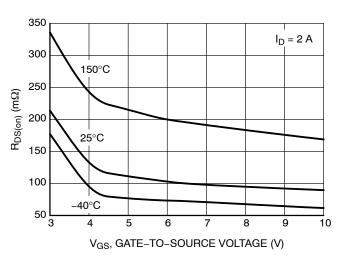


Figure 5. R<sub>DS(on)</sub> vs. Gate-Source Voltage

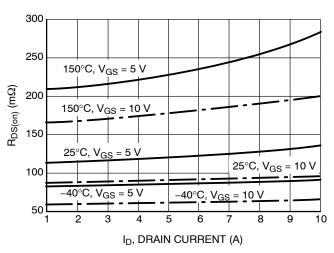


Figure 6. R<sub>DS(on)</sub> vs. Drain Current

#### TYPICAL PERFORMANCE CURVES

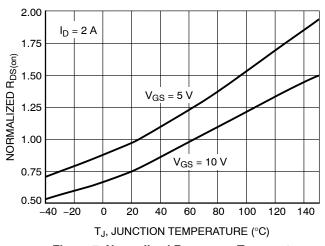


Figure 7. Normalized R<sub>DS(on)</sub> vs. Temperature

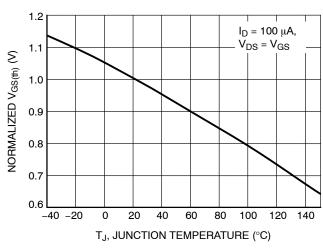


Figure 8. Normalized Threshold Voltage vs.
Temperature

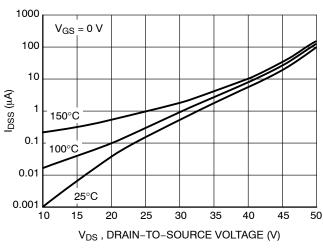


Figure 9. Drain-to-Source Leakage Current

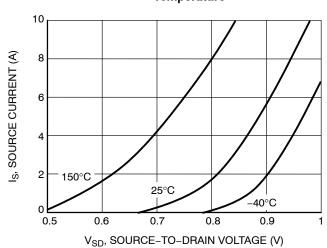
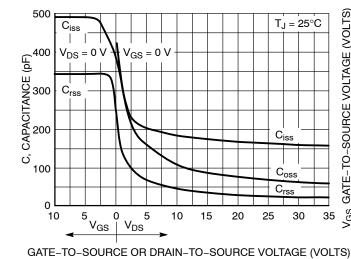


Figure 10. Source-Drain Diode Forward Characteristics



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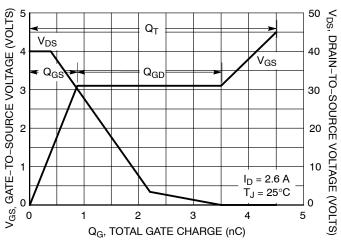


Figure 12. Gate-to-Source Voltage vs. Total Gate Charge

#### **TYPICAL PERFORMANCE CURVES**

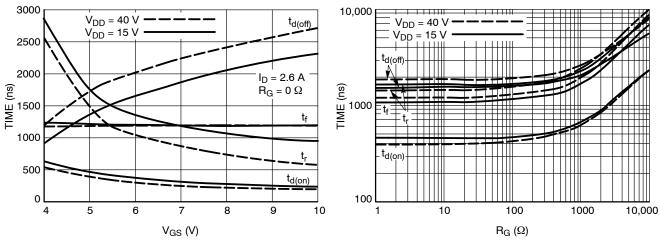


Figure 13. Resistive Load Switching Time vs.
Gate-Source Voltage

Figure 14. Resistive Load Switching Time vs. Gate Resistance ( $V_{GS} = 5 \text{ V}, I_D = 2.6 \text{ A}$ )

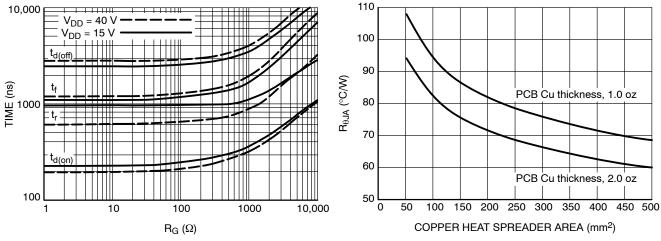


Figure 15. Resistive Load Switching Time vs. Gate Resistance ( $V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}$ )

Figure 16.  $R_{\theta JA}$  vs. Copper Area

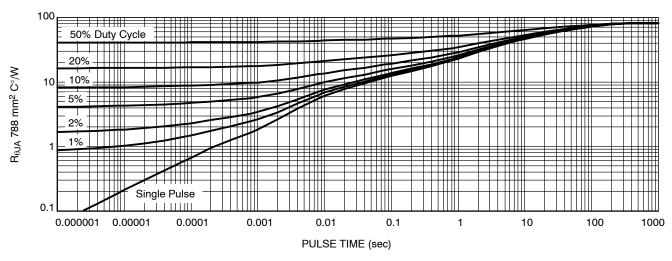


Figure 17. Transient Thermal Resistance

## **ORDERING INFORMATION**

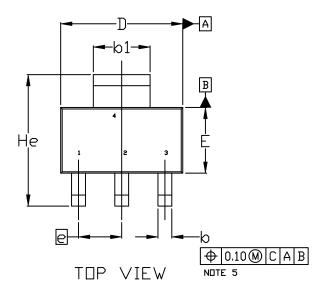
| Device        | Package              | Shipping <sup>†</sup> |
|---------------|----------------------|-----------------------|
| NCV8440STT1G  | SOT-223<br>(Pb-Free) | 1000 / Tape & Reel    |
| NCV8440ASTT1G | SOT-223<br>(Pb-Free) | 1000 / Tape & Reel    |
| NCV8440STT3G  | SOT-223<br>(Pb-Free) | 4000 / Tape & Reel    |
| NCV8440ASTT3G | SOT-223<br>(Pb-Free) | 4000 / Tape & Reel    |

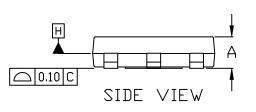
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



**SOT-223 (TO-261)** CASE 318E-04 ISSUE R

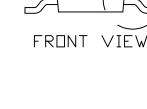
**DATE 02 OCT 2018** 





DETAIL A

A1

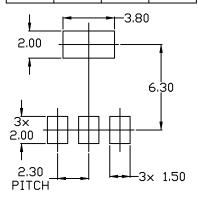


SEE DETAIL A

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5. ALLIS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS 6 AND 61.

|     | MILLIMETERS |          |      |  |
|-----|-------------|----------|------|--|
| DIM | MIN.        | N□M.     | MAX. |  |
| Α   | 1.50        | 1.63     | 1.75 |  |
| A1  | 0.02        | 0.06     | 0.10 |  |
| b   | 0.60        | 0.75     | 0.89 |  |
| b1  | 2.90        | 3.06     | 3.20 |  |
| c   | 0.24        | 0.29     | 0.35 |  |
| D   | 6.30        | 6.50     | 6.70 |  |
| E   | 3.30        | 3.50     | 3.70 |  |
| е   |             | 5'30 B2C | ,    |  |
| L   | 0.20        |          |      |  |
| L1  | 1.50        | 1.75     | 2.00 |  |
| He  | 6.70        | 7.00     | 7.30 |  |
| θ   | 0°          |          | 10°  |  |



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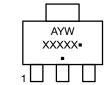
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## **SOT-223 (TO-261)** CASE 318E-04 ISSUE R

**DATE 02 OCT 2018** 

| STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE            | STYLE 3:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN   | STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE                |
|---|--|--|--|--|
| STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT        | STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE     | 4. DHAIN STYLE 8: CANCELLED  | STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| STYLE 11:<br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2 | STYLE 12:<br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT | STYLE 13:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |  |  |

# GENERIC MARKING DIAGRAM\*



A = Assembly Location

Y = Year W = Work Week

XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)
\*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may
not follow the Generic Marking.

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