FACULTY OF COMPUTING AND INFORMATICS

DMA5301
DISCRETE STRUCTURES
TRIMESTER 1 SESSION 2021/2022

ASSIGNMENT PART 2

GROUP:

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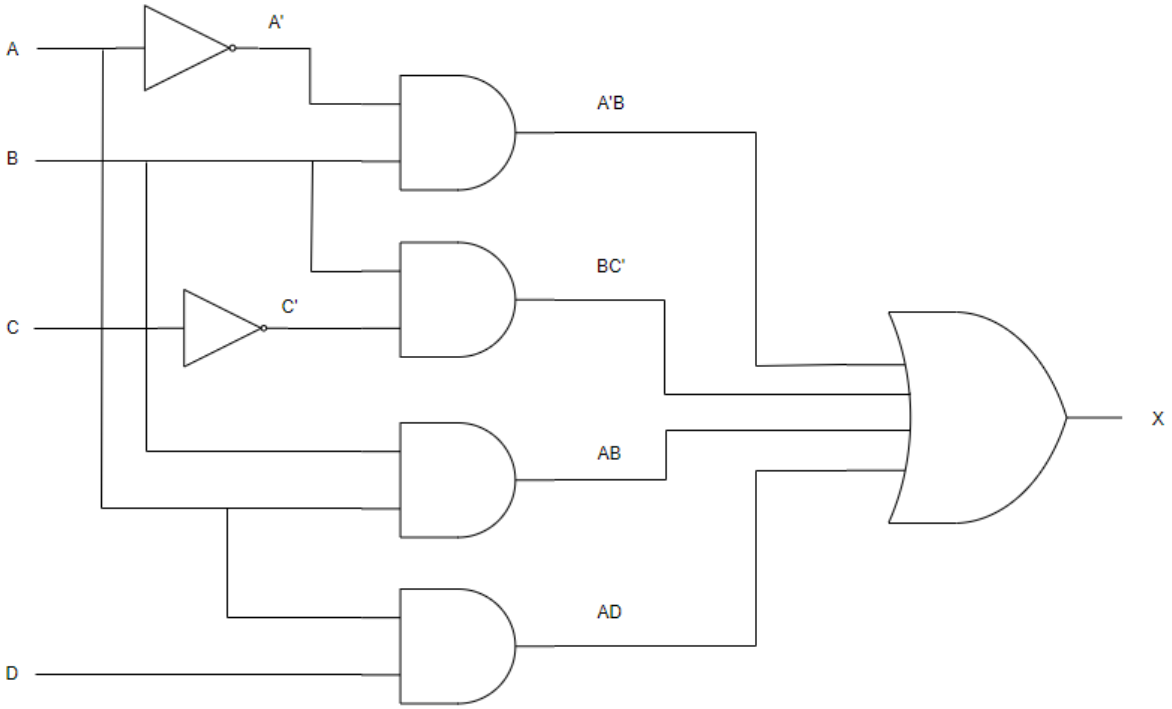
CHAPTER 8 & 9

A. Create your own LOGIC GATE CIRCUIT that fulfil all requirement below:
I. Must have 3 or 4 INPUT variables.
II. Circuit must have a combination of 6 to 7 logic gates with at least 3 different gates.
III. Draw the circuit and indicate the FINAL OUTPUT.
IV. Next, construct a truth table of Boolean Algebra based on your final output.

ANSWER

i) 4 inputs - A,B,C,D
ii) 3 different Gates - NOT gate, AND gate, OR gate
Combination of 7 logic gates -
2 NOT gates
4 AND gates
1 OR gate
iii) Logic Gate Circuit:



FINAL OUTPUT: X = (A'B)+(BC')+(AB)+(AD)

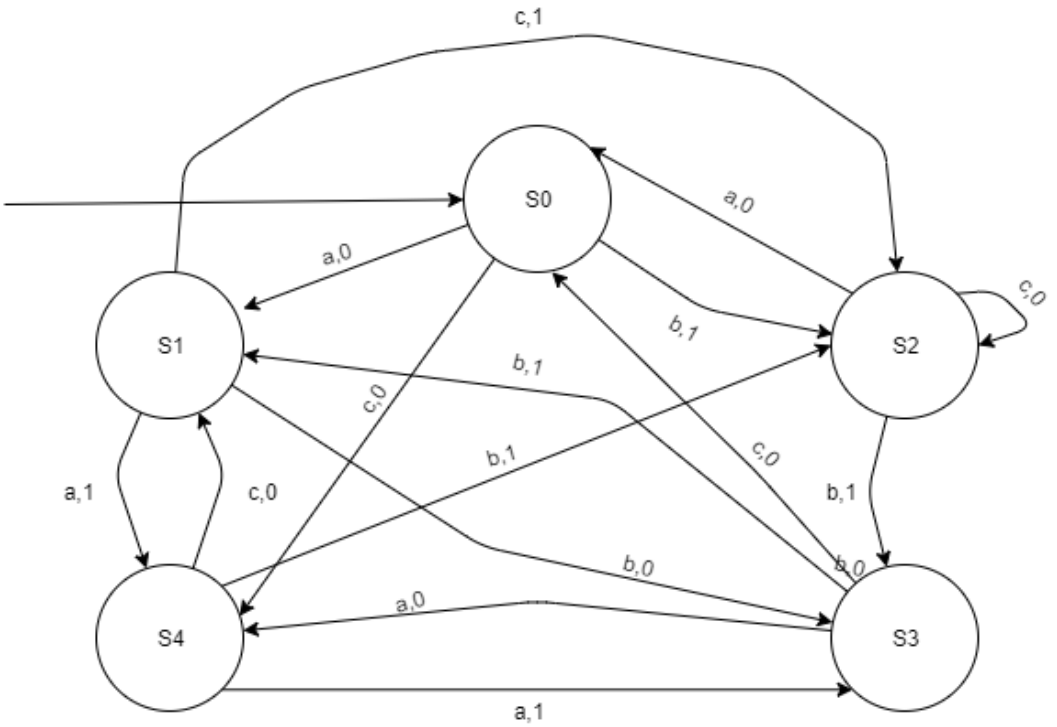
iv) Boolean Algebra = **(A'B)+(BC')+(AB)+(AD)**

A	B	C	D	A'	C'	(A'B)	(BC')	(AB)	(AD)	X
0	0	0	0	1	1	0	0	0	0	**0**
0	0	0	1	1	1	0	0	0	0	**0**
0	0	1	0	1	0	0	0	0	0	**0**
0	0	1	1	1	0	0	0	0	0	**0**
0	1	0	0	1	1	1	1	0	0	**1**
0	1	0	1	1	1	1	1	0	0	**1**
0	1	1	0	1	0	1	0	0	0	**1**
0	1	1	1	1	0	1	0	0	0	**1**
1	0	0	0	0	1	0	0	0	0	**0**
1	0	0	1	0	1	0	0	0	1	**1**
1	0	1	0	0	0	0	0	0	0	**0**
1	0	1	1	0	0	0	0	0	1	**1**
1	1	0	0	0	1	0	1	1	0	**1**
1	1	0	1	0	1	0	1	1	1	**1**
1	1	1	0	0	0	0	0	1	0	**1**
1	1	1	1	0	0	0	0	1	1	**1**

B. Create your own Finite State Machine M (FSM) that satisfy all requirement below:
I. 3 inputs, I = {a, b, c}
II. 5 states, S = {S0, S1, S2, S3, S4}
III. Output, O = {0, 1}
IV. Initial state S0.
a) Draw the state diagram of the machine M.
b) Construct the state table of the machine M.
c) Create one example of input string from machine M that has at least 8 strings and find the output string.
d) Can you redraw your Finite State Machine M (FSM) as a Finite State Automaton? Why (justify your answer)?

ANSWER

a) State Diagram:



b) State Table:

	INPUTS			OUTPUTS		
State	a	b	c	a	b	c
S0	S1	S2	S4	0	1	0
S1	S4	S3	S2	1	0	1
S2	S0	S3	S2	0	1	0
S3	S4	S1	S0	0	1	0
S4	S3	S2	S1	1	1	0

c) Input String: abcbacbb

OUTPUT: 00010011

d) Can you redraw your Finite State Machine M (FSM) as a Finite State Automaton?

Answer:

The Final State Machine can not be redrawn as a Finite State Automaton as long as the outputs from all of the states are not the same individually i.e s0 is required to output 0 in all of its outputs and i.e s1 is required to output 1 on all given outputs from s1.