

Technical Report:

Manufacturing Packaging Substrate

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2. Process Flow

1. Introduction

In this process, a substrate with a variety of embedded structures and components was manufactured. The objective of this experiment was to manufacture a multi-layer substrate with a large variety of embedded structures and components (each having desired characteristics) using standard techniques in the industry.

Substrates mechanically support and electrically connect IC components. In order to facilitate the electrical connection of IC components, passives and actives can be embedded inside of a substrate. In addition, thermal structures can be embedded to help maintain desired temperatures. In order to increase the density of these components, substrates can have multiple layers connected by vias.

When manufacturing substrate, there's always more than one way to reach some result. The procedure followed in this experiment focused on semi-additive processes because it reduces undercut. During the photolithography stages, contact lithography was selected over proximity, projection, or laser direct imaging because contact lithography has high resolution. However, during contact lithography, the mask can be damaged by debris caught between it and the substrate. In addition, a sequential build up process was selected over a parallel one. Using the sequential build up process helped reduce misalignment between the layers.

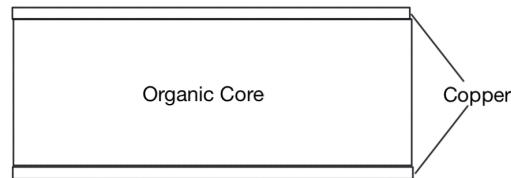


Figure 1. Image depicting the initial state of the substrate.

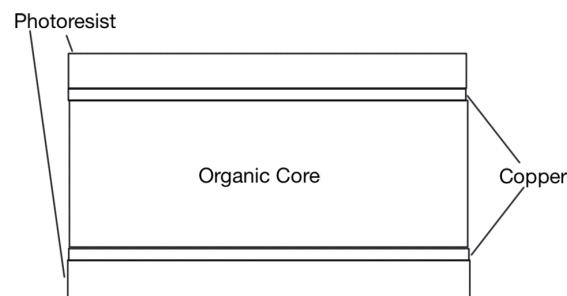


Figure 2. Image depicting the substrate after lamination.

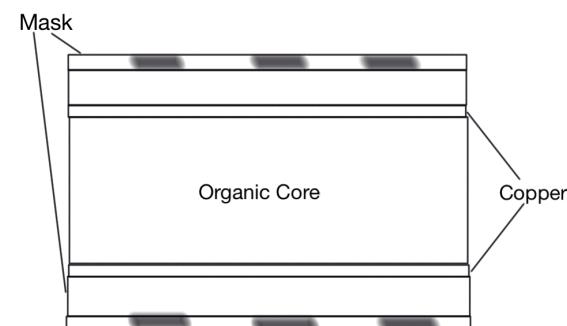


Figure 3. Image depicting the substrate after placing a negative, dry-film mask.

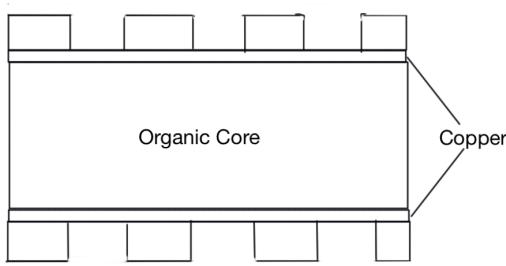


Figure 4. Image depicting the substrate after photoresist development.

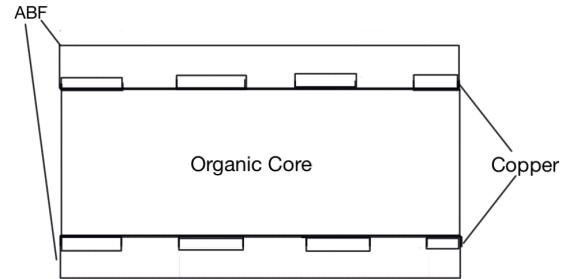


Figure 7. Image depicting substrate after treating with novabond process, vacuum lamination, hot press, and curing.

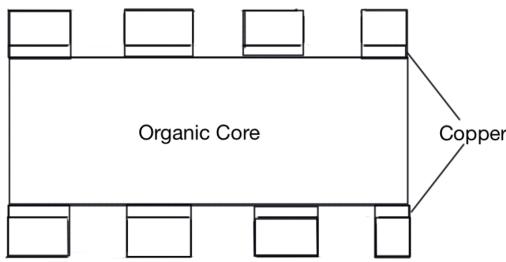


Figure 5. Image depicting the substrate after etching copper.

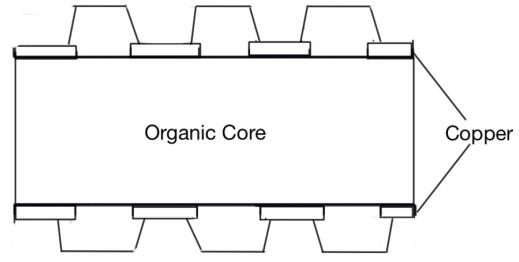


Figure 8. Image depicting the substrate after drilling micro vias.

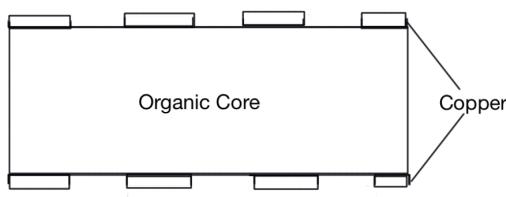


Figure 6. Image depicting the substrate after stripping photoresist.

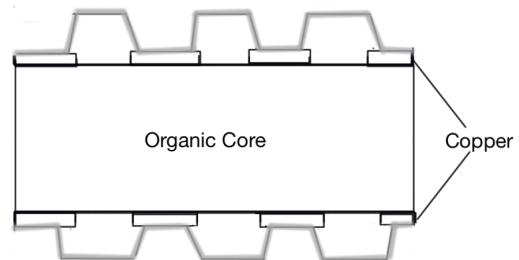


Figure 9. Image depicting the substrate after desmearing and depositing copper seed layer.

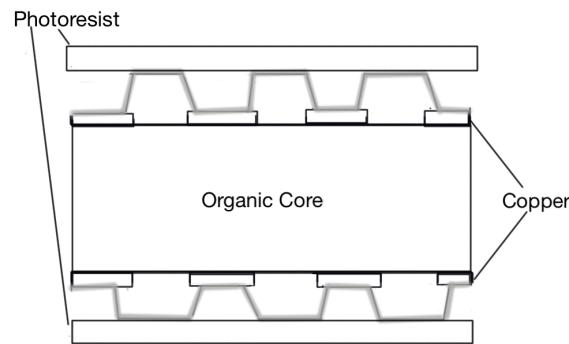


Figure 10. Image depicting the substrate after lamination.

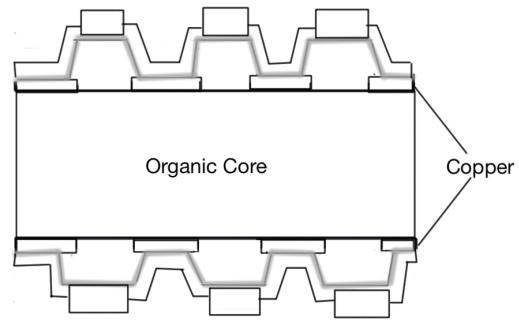


Figure 13. Image depicting the substrate after electrolytic copper plating.

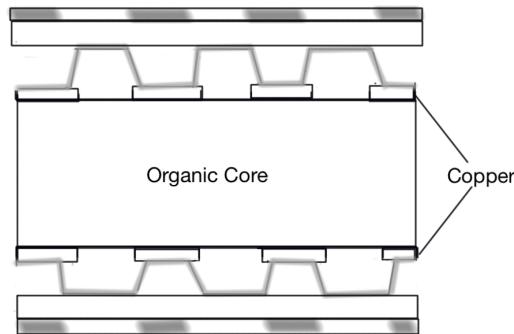


Figure 11. Image depicting the substrate after placing a positive, dry-film mask.

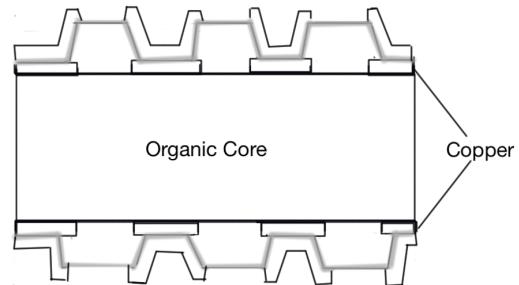


Figure 14. Image depicting the substrate after stripping photoresist.

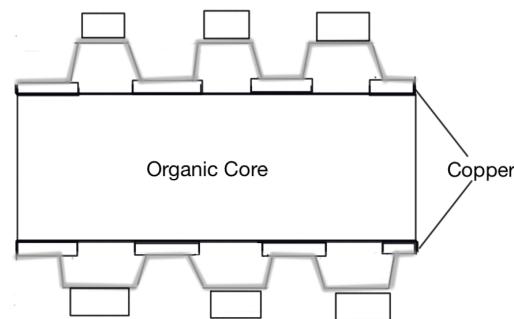


Figure 12. Image depicting the substrate after photoresist development.

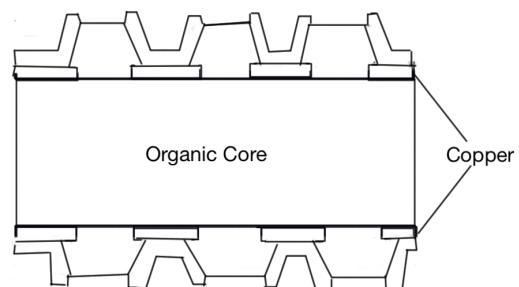


Figure 15. Image depicting the substrate after stripping copper seed layer.

TABLE 1
AFTER WHICH STEP TO PERFORM AN INSPECTION OR MEASUREMENT

Step	Test
Develop Photoresist	Verify completion under microscope
Strip Photoresist	Test for conductivity, take pictures
Drill Vias	Verify vias under microscope
Electroless Copper Plating	Measure copper seed layer
Strip Copper Seed Layer	Measure RLC components and line structures on board, take pictures, cross section

3. Materials, Tools, and Configuration

TABLE 2
MATERIALS, TOOLS, AND CONFIGURATION NEEDED FOR EACH STEP

Step	Device	Configuration	Buttons Enabled	Materials
Laminate (Layer 1)	Roller Laminator	Pressure: 1 mm Temperature: 110 °C Speed: 2 in/min	N/A	Dry Film Negative Photoresist
Laminate (Layer 2)	Roller Laminator	Pressure: 1 mm Temperature: 110 °C Speed: 2 in/min	N/A	Dry Film Positive Photoresist
UV Exposure (Layer 1)	Tamarack Photolithographic Device	Time: 6 s	Mask Hold Contact Mode Substrate Hold Expose Gap	M-1 Mask
UV Exposure (Layer 2)	Tamarack Photolithographic Device	Time: 6 s Align [+] on mask with that on board	Mask Hold Contact Mode Substrate Hold Expose Gap	M-2 Mask
Develop Photoresist	ChemCut Spray Developer	Temperature: 80 °F Speed: 43 in/min	Process Pump Heat Rinse Pump	N/A
Etch Copper	ChemCut Spray Etcher	Temperature: 115 °F Speed: 55 in/min	Process Pump Heat Rinse Pump	N/A
Conductivity Test	4 Point Probe	N/A	N/A	N/A
Strip Photoresist	Heat Plate	Temperature: 40 °C	N/A	3.6 mL de-ionized water .4 mL Photoresist stripper
Novabond Process Treatment		See table below		
Vacuum Laminate	Vacuum Laminator	Temperature: 200 °F Time (Vacuum): 90 s Time (Pressure): 30 s	N/A	ABF Film

Hot Press Laminate	Hot Press	Temperature: 238 °F Time: 90 s Pressure: 4 tons	N/A	ABF Film
Cure Film	Conventional Oven	Temperature: 180 °C Time: 30 min	N/A	N/A
Remove Organic Residue	Plasma Chamber	Time: 5 mins/side Temperature: 100 °C	N/A	N/A
Etch Anti-Tarnish	Acid Bath	Time: 5 min	N/A	N/A
Copper Plating	Electrolytic Plating Bath	Current (back): 6.1 A Current (front): 6.8 A Temperature: 22 °C	N/A	N/A
Strip Photoresist	Beaker	Temperature: 40 °C Time: 4 min	N/A	N/A
Strip Copper Seed Layer	Spray Etcher	Speed: 35.1 in/min	N/A	N/A
Cross Section	Polisher	Pads: Varies Speed: Varies	N/A	Solution of 2 parts powder, 1 part liquid acrylic
Measure R Components	Multimeter	Mode: Ohms	N/A	N/A
Measure LC Components	Precision LCR Meter	Frequency: 1MHz	N/A	N/A

TABLE 3
STEPS IN NOVABOND PROCESS TREATMENT

Step	Temperature (°C)	Time (s)
Soft-Clean Process	30	30
De-Ionized Water Rinse	N/A	120
Novabond Conditioner	50	60
Novabond Coating Solution	70	360
De-Ionized Water Rinse	N/A	240
Novabond Reducer	35	60
De-Ionized Water Rinse	N/A	120
Novabond Protector	33	60
De-Ionized Water Rinse	N/A	240

4. Results

TABLE 4
MEASUREMENTS OF COPPER SEED LAYER
AFTER ELECTROLESS COPPER PLATING

Side	Height (nm)
Front	229
Back	305

TABLE 5
CONDITION OF DOUBLE COMB STRUCTURES IN
COLUMN-MAJOR ORDER

Comb Structure	Condition
1	Short
2	Short
3	Okay
4	Okay
5	Okay
6	Short
7	Okay
8	Okay
9	Okay
10	Okay
11	Short

TABLE 6
MEASURED RESISTANCE OF DAISY CHAINS IN
COLUMN-MAJOR ORDER

Daisy Chain	Via Size (mil)	Resistance (ohm)
1	4	.646
2	4	.658
3	4	.704
4	4	.726
5	6	.527
6	6	.531
7	6	.556
8	6	.560
9	8	.421
10	8	.418
11	8	.445
12	8	.441

TABLE 7
MEASURED INDUCTANCE AND QUALITY
FACTOR OF INDUCTORS IN COLUMN-MAJOR
ORDER

Inductor	Quality Factor	Inductance (nH)
1	.11	103
2	.31	402
3	.11	103
4	.4	572

TABLE 8
MEASURED RESISTANCE OF RESISTORS IN
COLUMN-MAJOR ORDER

Resistor	Resistance (ohms)
1	3.195
2	2.936
3	3.247
4	8.635

TABLE 9
MEASURED CAPACITANCE OF CIRCULAR
CAPACITORS IN COLUMN-MAJOR ORDER

Capacitor	Capacitance
1	154.354
2	Short
3	204.4
4	Short
5	Short
6	Short

TABLE 10
MEASURED CAPACITANCE OF SQUARE
CAPACITORS IN COLUMN-MAJOR ORDER

Capacitor	Capacitance
1	72.7
2	57.5
3	Short
4	55.8
5	Short
6	249.5
7	Short
8	Short

5. Analysis

5A. Comb Structure

Of the eleven double comb structures, four were shorted and seven were okay. Upon inspection, the cause of the short was that part of one comb structure had a very thin connection to its corresponding comb structure, as shown in the figure below. This defect was likely caused by dust on the mask that appeared as an opaque feature during UV exposure. Furthermore, because contact printing was used, debris may have caught between the mask and resist, causing damage to the mask. The risk of dust particles affecting photolithography can be reduced in the following ways: using a higher-class clean room, performing step-and-repeat projection printing (which would still allow for high resolution printing, but eliminate the risk of mask damage) instead of contact printing, and frequently replacing the mask.

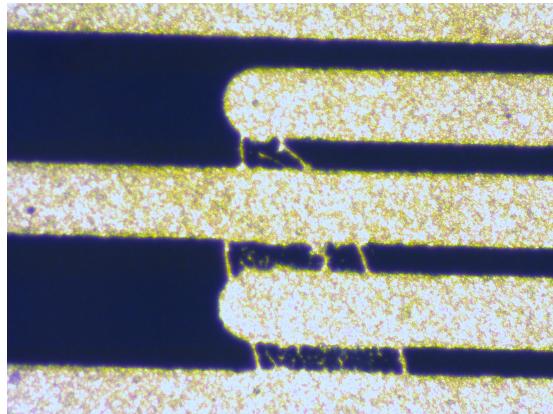


Figure 16. Image depicting thin connection between comb structures causing short.

5B. Capacitors

Of the fourteen total capacitors, eight were shorted and six worked. The capacitor would short if the plates touched, even if at only one point. The part of the experiment responsible for embedding the capacitor. However, it is also possible that a surface scratch on the thin connection where the probe was placed during capacitance readings would cause the capacitor to appear shorted.

TABLE 11

THEORETICAL CAPACITANCE OF CIRCULAR CAPACITORS IN COLUMN-MAJOR ORDER¹

Capacitor	Area (m^2)	Theoretical Capacitance (F)	Error (%)
1	6.56E-5	3.25E-5	52.48
3	8.31E-5	4.11E-10	50.27

TABLE 12

THEORETICAL CAPACITANCE OF SQUARE CAPACITORS IN COLUMN-MAJOR ORDER

Capacitor	Area (m^2)	Theoretical Capacitance (F)	Error (%)
1	2.09E-5	1.03E-10	29.69
2	2.09E-5	1.03E-10	44.39
4	2.09E-5	1.03E-10	46.03
6	8.36E-5	4.14E-10	39.67

In the capacitors that worked, the measured capacitance ranged from 30% to 50% less than the theoretical capacitance. Some of this error can be explained because it was assumed when calculating the theoretical capacitance that the distance between layers is universal across the board.

5C. Inductors

The four inductors are identical on the mask, so they were intended to have identical inductance, which was not the case. Furthermore, the inductors have low quality factors (ranging from .11 to .4), which means that the inductors created do not have the attributes of ideal, lossless inductors.

5D. Daisy Chains

When comparing the average measured resistance of the daisy chains with via size, the plot has an R^2 value almost equal to 1, which indicates a linear relationship. This means that for every additional unit of copper in the via, the resistance increases by a constant factor, which is an intended characteristic. In addition, the

¹ Capacitance calculated using equation $C=k \cdot e_0 \cdot A/d$, where $k = 3.71$, and $d = 6.64\mu m$ (see Figure 20 in Appendix)

slope of the best-fit equation can be used to estimate the internal resistance of the material.

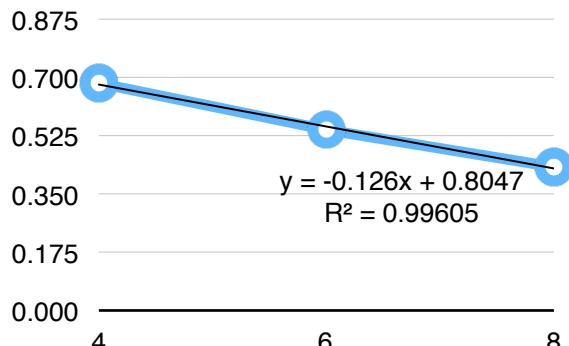


Figure 17. Plot comparing average measured resistance (ohms) of daisy chains with via size (mil).

5E. Blind Vias

The resultant blind vias from this process had two major errors: undercut and roughness, as shown below. The surface was roughened in order to increase the bonding strength between the laminate and copper. As a result, the roughness was passed onto the vias during line etching. Roughness is a problem because it can cause reflection that inhibits the signal. One way to reduce roughness would be to use a film that better adheres to copper; both wet films and other materials could be explored.

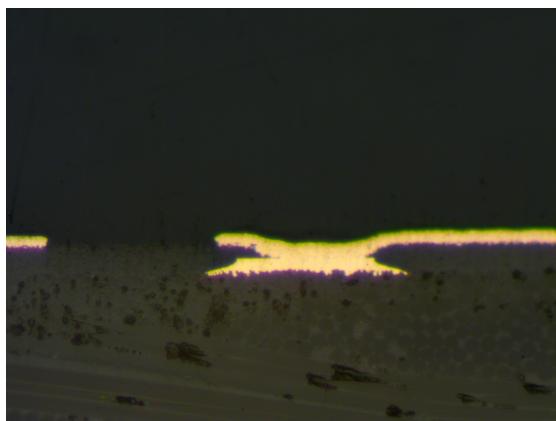


Figure 18. Image depicting roughness and undercut in connection between via levels.

Isotropic undercut occurs during etching. Undercut is a problem because it can cause feature instability and connectivity issues. It

could be prevented by only using additive processes or reduced by ion sputtering².

5F. Alignment

The vias are not perfectly aligned on the board, as shown in the figure below. This would present a large problem if the vias were not aligned on a conductive surface, or aligned onto the wrong surface. To improve alignment, a photolithographic tool with more auto-alignment accuracy could be used.

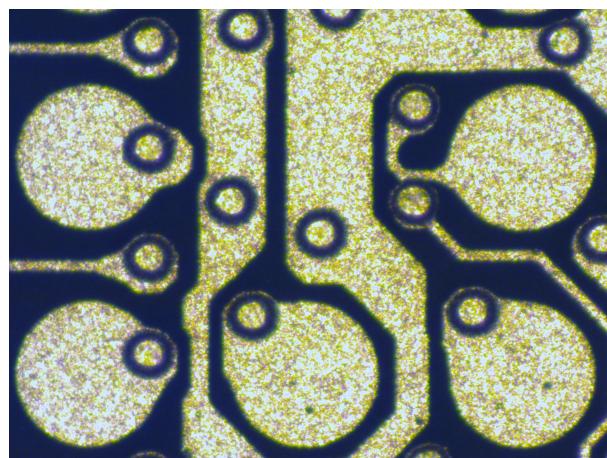


Figure 19. Image depicting via misalignment in BGA on backside of board.

6. Conclusion

As previously mentioned, the objective of this experiment was to manufacture a substrate with a variety of embedded components that had certain characteristics using standard techniques in industry. To that end, the resulting substrate did not have many of those characteristics. Of the measured components, over a third of the double comb structures and over half of the capacitors were shorted. Among the working capacitors, the error between theoretical and measured capacitances ranged from 30% to 50%. In addition, there were alignment issues, undercut, and roughness in the vias.

Overall, this board has plenty of errors that would cause it to get scrapped for commercial purposes. These errors stemmed from implementation, not design.

² Valbusa, U., C. Boragno, and F. Bautier De Mongeot. "Nanostructuring Surfaces by Ion Sputtering."

References

Valbusa, U., C. Boragno, and F. Bautier De Mongeot. "Nanostructuring Surfaces by Ion Sputtering." *Journal of Physics: Condensed Matter* (2002): n. pag. *Research Gate*. Research Gate, 22 Aug. 2002. Web. 9 Dec. 2015.

Appendix

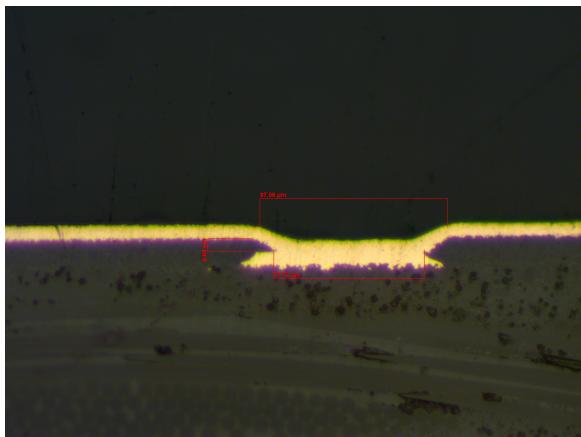


Figure 20. Image depicting measurement of 6.64 um distance between via layers, assumed to be universal across board.

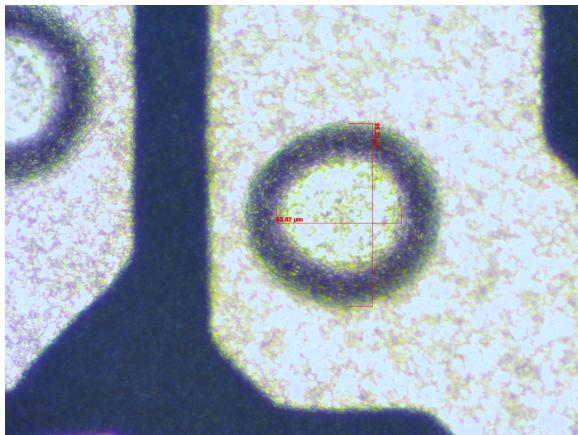


Figure 21. Image depicting measurement of via size on BGA.

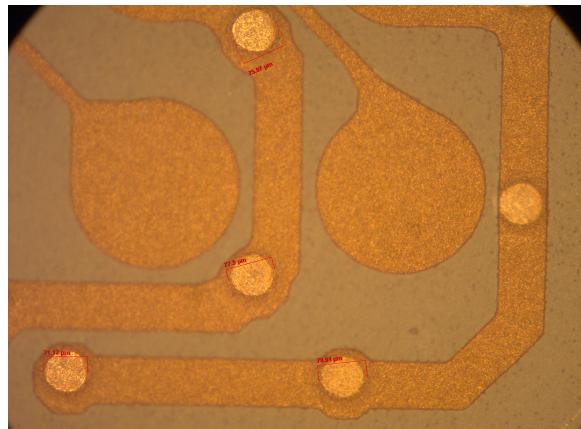


Figure 21. Image depicting via alignment in BGA on front of board.

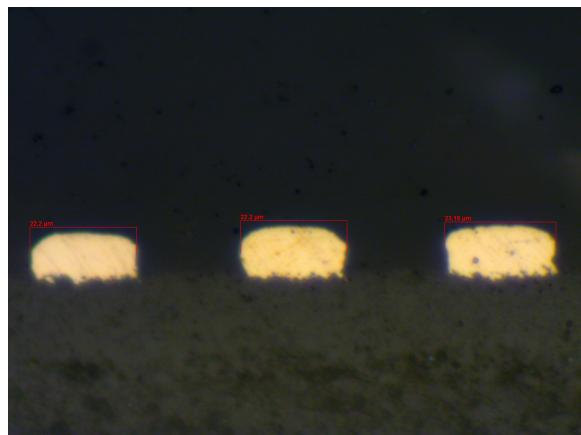


Figure 22. Image depicting cross section measurement of traces on board.