**2.0 RESISTIVE NETWORKS**

**a.** intro to KVL and KCL

**b.** Use KVL and KCL to solve circuit

**2.1 TERMINOLOGY**

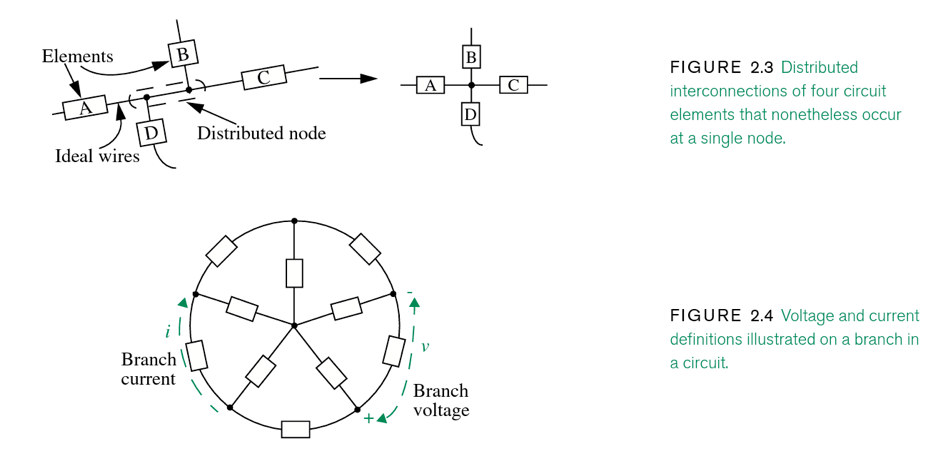
**a.** Junction where 2 + elements are connected = node

**b.** 2 + nodes connected= branch (aka edge)

**c.** Element = branch for only 2 elements

**d.** Since elements and branches are the same for circuits formed of two-terminal

elements, the **branch voltages and currents are the same as the corresponding terminal variables for the elements forming the branches.**

**e. **

**2.2 KIRCHHOFF’S LAWS**

**a.** KVL and KCL derive from Maxwell’s equation.

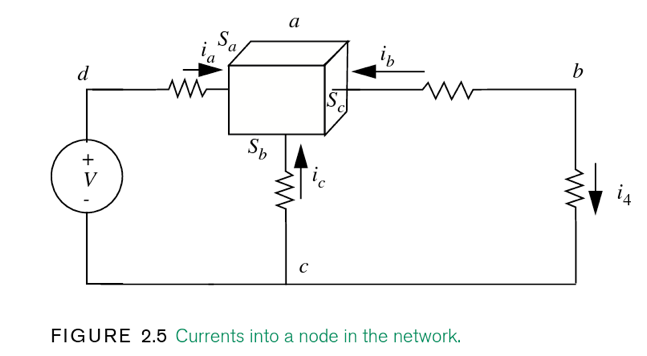
**b.** They are lumped-parameter simplifications into a circuit

**2.2.1 KCL**

**a. What is KCL?** The current flowing out of any node in a circuit must equal the current flowing in. That is, the algebraic sum of all branch currents flowing into any node must be zero.

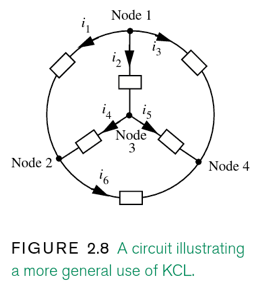
**b.** Current coming in through some branches = current going out through the other branches.

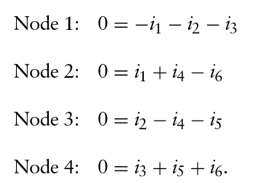
**c.** ia + ib + ic = 0

**d.** 

**in node a:** ia + ib + ic = 0

**in node b:** -ib – ic =0

**e.** 

**f.** 

net current in = net current out. KCL analysis on this closed circuit. As such, adding all those equations sum to 0. A circuit with N node will have N-1 independent statements of KCL.

**2.2.2 KVL**

**a. What is KVL?** The algebraic sum of the branch voltages around any closed path in a network must be zero.

**i.** Voltage between two nodes is independent of the path along which it is accumulated.

**ii.** Like KCL, KVL is an expression of energy conservation.

**b. Look at the chpt book problems**

**2.3 CIRCUIT ANALYSIS: BASIC METHOD**

**a. Basics of circuit analysis:**

**i.** Define the branch and current voltage in the circuit in a CONSISTENT MANNER. IE. + VOLTAGE is CW flow into a + end of voltage.

**ii.** Assemble the element laws for the elements.

**iii.** Apply Kirchhoff’s current and voltage laws

**iv.** Jointly solve the equation sassembled in Steps 2 and 3 for the branch

**2.3.1 SINGLE-RESISTOR CIRCUITS**

**a.**