Targets

Group 306

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Introduction

This document analyses the targets for each of the lowest level blocks developed in the functional decomposition. The "Targets" section focuses on defining these targets for the functions. The section is ordered with all of the analog components (microphone, analog to digital converter, I^2C module, and speaker), then the digital components in the ASIC (I^2C module, memory module, Fast Fourier Transform module, and the control module), and ends with 3 extra targets that need to be hit for a successful system (real world application, microprocessor memory, LCD display) that are not in the functional decomposition. For each of the targets, a justification, method of validation, and tools needed are discussed.

The targets were arrived by thinking about the inputs and outputs, and the relationship between all functions. With this information, research was done on each function, and the important targets were selected. For example, for the microphone, the input is an audio sound and the output is an electrical signal corresponding to the sound. Since the microphone is analog, timing concerns were not looked at. However, since the whole system anticipates the most accurate sound signal input, the target for the microphone was chosen to be a frequency response target. This allows for low errors with the dual tone frequencies of interest. Then the justification for the numbers, the method of validation, and the tools needed were all researched. This plan was done for the rest of the functions.

The mission critical targets are talked about after the targets. If these targets are not met, they have impacts on other functions and the system might not perform as intended. These targets were chosen to be the sampling frequency of the analog to digital converter and FFT detection bandwidth and timing constraints. These are the major targets for the system to work. In a high level, if an analog signal can be converted to a digital signal with enough precision and speed (analog to digital converter) and if the frequency response of the digital signal can be analyzed (FFT), then a dual tone can easily be identified.

Targets

Microphone

- Target: The microphone needs to have a 0 +/- 5 dB frequency response between 170Hz-6500Hz
    - Justification: the lowest frequency of a dual tone is 697Hz and the highest is 1633Hz. This means the Nyquist frequency is Nf = 1633Hz*2= 3266Hz. The Nyquist frequency was multiplied by 2 to obtain 6532Hz and simplified to 6500Hz.The 6500Hz is nearly 4 times the maximum frequency of 1633Hz, so in order to keep symmetry, the lower frequency of 697 was divided by 4 to obtain 174Hz, simplified to 170Hz.

- Method of Validation: measure the voltage response of a 170Hz cosine wave with an oscilloscope and use the sensitivity rating of the microphone to determine the quality of the reproduction (frequency response). Perform the same test with a 6500Hz cosine wave and determine the frequency response by viewing the voltage with an oscilloscope.
- Tools needed: oscilloscope and sound frequency generator. The oscilloscope is needed to analyses the voltage output of a microphone after a cosine sound is made with the frequency generator.

Analog to Digital Converter

- Target: The analog to digital converter needs to be able to sample a signal with a sampling rate of at least 5kHz
  - Justification: The Nyquist frequency of the highest frequency of a dual tone is 3266Hz. It is always a good idea to oversample the Nyquist rate. The 5KHz frequency was obtained by oversampling the Nyquist rate by 50% (4899Hz) and rounding up.
  - Method of Validation: Inject a constant voltage into the analog to digital converter and see how many outputs (samples) are received by the analog to digital converter each second with a logic analyzer.
  - Tools needed: logic analyzer and power supply. The logic analyzer measures the sampling frequency of the analog to digital converter that converts a constant voltage given by a power supply

Inter-Integrated Circuit (I^2C) on the Microprocessor

- Target: The I^2C module has to be able to do 400Khz transmission speeds
  - Justification: The 400Khz transmission speeds is an I^2C standard fast mode transmission speed
  - Method of Validation: connect the I^2C module to a slave device and treat the module as the master. Transmit a junk address to the slave and observe the frequency of the transmission with a logic analyzer.
  - Tools needed: logic analyzer and slave device. The logic analyzer measures the transmit speed of the I^2C module that is sending junk data to a slave.

Speaker

- Target: The microphone needs to have a 0 +/- 5 dB frequency response between 170Hz-6500Hz
  - Justification: the speaker mimics the inverse of the microphone. In theory, if a constant voltage is sent to the speaker, it should convert the voltage to a sound frequency. If this sound is fed to the microphone, the output of the microphone should be the same voltage sent to the speaker.

- Method of validation: measure the audio frequency response of a voltage that corresponds to a 170Hz sound signal given in the sensitivity parameter of the datasheet. Measure the frequency of the output and obtain the frequency response. Replicate this for the 6500Hz frequency response.
- Tools needed: sound level meter and power supply. The sound level (most likely a phone) will record the sound frequency of the speaker that is fed a voltage from a power supply.

Inter-Integrated Circuit (I^2C) on the ASIC

- Target: similar to the microprocessor, the ASIC I^2C module has to be able to do 400Khz transmission and receive speeds
  - Justification: The 400Khz transmission speeds is an I^2C standard fast mode transmission speed
  - Method of Validation: connect the ASIC I^2C module to a slave device and treat the module as the master. Transmit a junk address to the slave and observe the frequency of the transmission with a logic analyzer.
  - Tools needed: logic analyzer and slave device. The logic analyzer measures the transmit speed of the I^2C module that is sending junk data to a slave.

Memory on the ASIC

- Target: The memory should be able to store 6.5 Kbits
  - Justification: Assuming the analog to digital converter's bit per sample is 10 bits/sample, and a dual tone is analyzed for a length of at most 65ms (ETSI Standard), this means there are 325 samples for each dual tone length according to the calculation 65 ms * 5000 samples/s. The 5000 samples/s is obtained from the sampling rate of the analog to digital converter of the microprocessor. Since each sample is 10 bits, it turns out that for each dual tone length, 3250 bits are needed. Moreover, Fast Fourier information needs to be stored, so the 3250 bits are multiplied by 2 to obtain 6500 bits. This number is an overestimation because both digital signal of the dual tone and its Fourier output would not be stored at the same time.
  - Method of validation: try to store bits in all memory locations and could how many bits the memory module can fit
  - Tools needed: environment to store and read memory. The environment is needed to store information through software; this environment will most likely be an FPGA IDE.
- Target: The memory access time should be 10 us or less
  - Justification: the worst-case scenario form memory speed is that 6100 bits need to be read in 65 ms. So, it means each bit needs to be read in 10 us. This is the worst-case scenario because it assumes both the digital audio data and the Fast

Fourier data need to be extracted from memory in the length of the max dual tone time.
    - Method of validation: read all the memory off the memory submodule and determine how long it takes to read.
    - Tools needed: environment to store and read memory. The environment is needed to store information through software; this environment will most likely be an FPGA IDE.

Fast Fourier Transform Module on the ASIC

- Target: The detection bandwidth should be within +-1.5% of the design center frequency, and the rejection bandwidth should be beyond +-3.5% the center frequency.
    - Justification: The FFT module should be efficient enough to run in real time. There is a tradeoff between the number of points that must be taken to get an accurate spectrum compared with the time to evaluate the points. There is a standard for the detection and rejection bandwidths.
    - Method of validation: Vary the detection window of the digital FFT module. Feed some DTMF signals and measure the time that it takes to produce outputs.
    - Tools needed: FPGA prototype of the FFT module, and logic analyzer.

- Target: Each specific signal frequency should be detected if they are present at a power level of 9dB greater than the other frequencies of the same group (low/rows or high/columns). Also, the difference in power level between the low and high signal frequencies should be between 4dB to -8dB
    - Justification: The FFT module should accurately determine the DTMF signals that are present. The power level of the signals is generated by the FFT module, and it is the main data used to detect the DTMF frequencies present in a signal. There is a standard for desired power level of a DTMF signal.
    - Method of validation: Perform different tests with signals having different power level ratios, also introduce noise in some tests.
    - Tools needed: FPGA prototype of the FFT module, and logic analyzer.

- Target: The duration of a valid signal should be greater than 23ms, the interdigit time (time between end of one signal and beginning of the next) should be at least 40ms, and the cycle time (time between start of a signal and start of the next) should be at least 93ms.
    - Justification: The FFT module should be able to filter noise and speech audio signals. The FFT should be programmed to detect some timing constraints based on the DTMF standards.

- Method of validation: Perform different tests with non-DTMF signals vs DTMF standard compliant signals, also introduce random noise and speech in some tests.
- Tools needed: FPGA prototype of the FFT module, and logic analyzer.

Control Module on the ASIC

- Target: The process speed of the control module should not exceed 65ms.
  - Justification: The control module must be able to send commands to different modules and perform logic operations in a shot amount of time that does not affect the real-time operation of the system.
  - Method of validation: Perform timing simulations using ModelSim Altera.
  - Tools needed: Verilog code of the Control module, ModelSim Altera program.

Real World Application

- Target: be able to decode 3 dual tones in a row in 195 ms
  - Justification: 3 dual tones in a row creates 1728 different combinations of dual tones. This allows a real-world application to be built that takes in a special combination of 3 dual tones and creates a real-life event (ex. Locking a door). 195 ms is needed because each dual tone has a max length of 65 ms; therefore, 3*65 ms = 195 ms.
  - Method of validation: create a program that generates 3 dual tones in a 195ms window and see if the system detects the combination
  - Tools needed: MATLAB script creating 3 sequential dual tones in 195 ms

Microprocessor Memory

- Target: The memory should be able to store 6.5 Kbits of memory
  - Justification: the microprocessor should have the same memory as the ASIC memory in order for the ASIC to transmit what is in its memory to the microprocessor such that the values can easily be analyzed through a microprocessor IDE. This will most likely be used for testing and initial prototyping.
  - Method of validation: use the microprocessor IDE to determine how much free space is available in the microprocessor.
  - Tools needed: microprocessor IDE to check memory locations.

LCD Display

- Target: The LCD should have a refresh rate of at least 65 ms

- Justification: If the system decodes the entire DTMF signal in 65 ms, the only way to display the resultant decoded DTMF is if the LCD also has a refresh rate equal to or less than 65 ms.
- Method of validation: send a series of different image to the LCD and calculate how many refreshes take place in a span of 1 minute. Take the number of refreshes per minute and calculate how many seconds it takes for 1 refresh.
- Tools needed: LCD display and timer. The number of patterns programmed images are counted for the LCD display with a timer.

Mission Critical Targets

The first mission critical target is the analog to digital converter's 5KHz sampling rate. The changing of the 5KHz sampling rate determines if there is enough resolution to properly sample a dual tone, but it also limits the speed of the analog to digital converter. Speed is important because there is a 65 ms time window that a dual tone needs to be sampled in order to make the system real time. The balance between resolution and speed was roughly done in this document, but with experimental adjustments, it might change. This is due to noise considerations, inaccuracies with the analog to digital converters, and limits of the converters that are unknown (more research will be looked at in concept generation).

The second mission critical target is the Fast Fourier Transform module's detection bandwidth. This is a very important quantity in that if the FFT module is given an error bound for its bandwidth. This allows the FFT to quickly and accurately convert a time domain digital dual tone signal to the frequency domain to decide what dual tone was sent. Since this mathematical approach is the main way of analyzing dual tones, it is a mission critical target.

Summary

In summary, there are certain targets that need to be met for the system to function as planned. These targets are present for the analog design (microcontroller) of the system and the digital design (ASIC). Very important targets were later classified as mission critical targets. These include the sampling rate of the analog to digital converter and the Fast Fourier Transform's detection bandwidth. Since the majority of the design depends on the speed and accuracy of these 2 items, they are classified as mission critical. If all targets are met according to the table seen below, then the system should function as intended. The target nominal values, or their errors, might be changed as prototypes are created and tested. See the table below. Also, see the appendix for a more detailed summary.

Target Part	Summary
Microprocessor	ADC has a 5KHz sampling frequency, 400KHz I^2C, and microphone and speaker have 0 dB frequency response over 170-6500 Hz
ASIC	400KHz I^2C, 6.5 Kbit total memory with 10 us delay, +/- 1.5% detection bandwidth FFT with all timing targets, 65 ms control speed
System Level	Real world application response time less than 65 ms, 6.5 Kbit of microprocessor memory, 65 ms refresh rate of LCD display

Appendix

The target catalog can be seen below.

Metric Number	Need	Metric	Imp	Units	Marginal Value	Ideal Value
1	3, 7	Microphone Frequency Response	3	dB, Hz	+/- 5 dB	0 dB
2	1, 3, 6, 7	ADC Sampling Rate	5	kHz	+/- .5 kHz	5 kHz
3	1, 3	I2C Transmission Speed (analog)	3	kHz	400 kHz or 1 MHz	400 kHz
4	3	Speaker Frequency Response	1	kHz	+/- 5 dB	0 dB
5	1,3	I2C Transmission Speed (digital)	3	kHz	400 kHz or 1 MHz	400 kHz
6	1, 2, 4, 6	Total Memory Storage	3	Kbits	+/- .5 kBits	6.5 Kbits
7	1, 2, 4, 6	Memory Speed	3	us	+/- 1 us	10 us
8	1, 2, 4, 6, 8	FFT detection bandwidth	5	%	+/- 1.5%	0%
9	1, 2, 4, 6, 8	FFT power detection	4	dB	greater than 9dB	greater than 9dB
10	1, 2, 4, 6, 8	FFT valid signal duration	3	ms	greater than 23ms	greater than 23ms
11	1, 2, 4, 6, 8	Control module speed	4	ms	less than 65ms	65ms
12	5	Application decode time	2	ms	less than 195ms	195ms
13	3	Total microprocessor memory	2	Kbits	+/- .5 kBits	6.5 Kbits
14	3, 7	LCD refresh rate	1	ms	less than 65ms	65ms