RDMA with PCIe and Ethernet IP

1. Introduction

The RDMA with PCIe and Ethernet IP is an implementation over Converged (RoCE v2) NIC functionality. This IP core can work with a wide variety of Xilinx hard and soft MAC IPs. it provides a high throughput, low latency, and reliable data transfer solution over standard ethernet.
This IP allows simultaneous connections to multiple remote hosts running RoCE v2 traffic.

Below is the diagram showing module internal modules and connectivity.

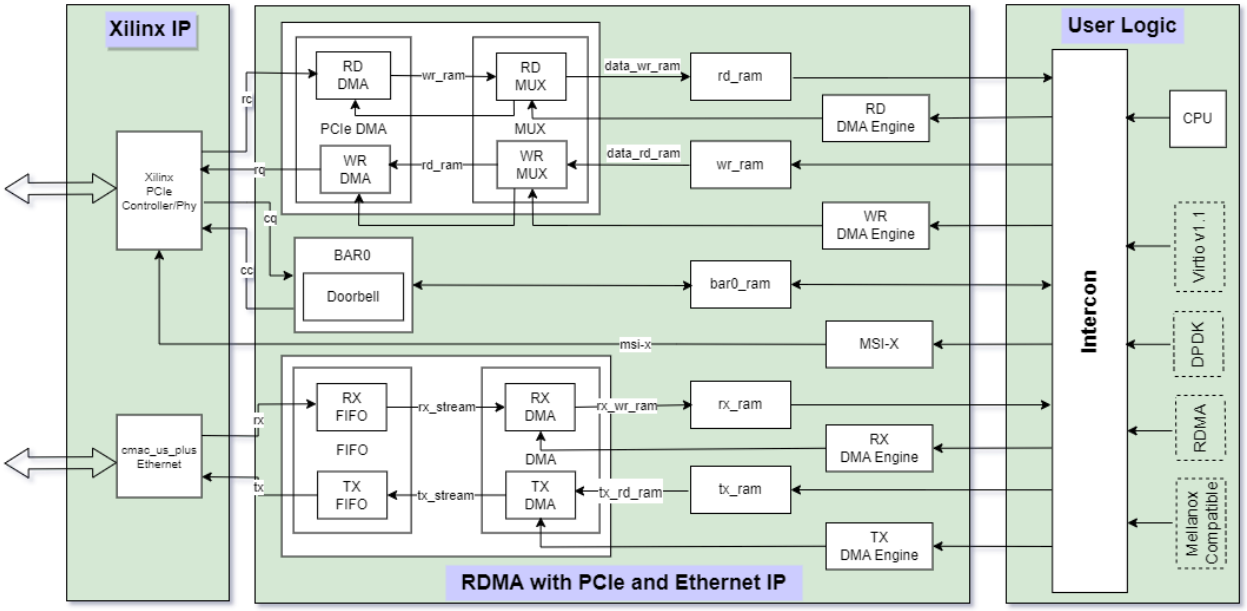

Figure 1: RDMA with PCIe and Ethernet IP

2. Overview

The PCIe-Ethernet QDMA subsystem is a PCIe based multi-channel queue DMA ideal for Infrastructure Processing Unit (IPU).
Data processing Unit (DPU) to offload CPU data movement. The DMA subsystem can be configured by interface types allowing it to function in many different modes based on the DMA descriptor depending on user logic via AXI interface.

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3. Features

Here are the features of the RDMA with PCIe and Ethernet IP:

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1. Ideal to replace Xilinx® LogiCORE™ for PCI Express® (PCIe)
2. Remote Direct Memory Access (RDMA)
3. DPDK driver support
4. Virtual I/O Device (VIRTIO) Version 1.1
5. PCIe to Ethernet FPGA Design
6. Ethernet: 100/200 Gigabit
7. PCIe: Gen3 x16/Gen4 x 8
8. FGPA: Xilinx
9. Support user-define descriptor format
10. Support user-define packet payload size to optimize performance
11. Support for both the AXI4-Memory Mapped and AXI4-Stream interfaces per queue
12. Multi-queue sets host to controller/controller to host descriptor rings
13. Support polling mode (Status Descriptor Write Back)
14. Controller to host stream interrupt moderation
15. 2k MSI-X vectors
16. Performance: 90Gbps+ PCIe-Ethernet transfer with Xilinx FPGA - with PCIe Gen3x16
17. Demo available using poll mode driver and a Network Interface Card (NIC) bind to the poll mode driver
18. Demo: Bypassing the kernel using user space