RDMA over Converged Ethernet (RoCE v2) system

Enables RNIC use-cases with FPGA based Smart NIC

The GROVF RDMA IP core and host drivers provide RDMA over Converged Ethernet (RoCE v2) system implementation and integration with standard Verbs API.

RDMA IP is delivered with reference design which includes the IP subsystem itself the 100G MAC IP subsystem, DMA subsystem, host drivers and example application on software. The system drivers are integrated with OFED standard Verbs API and is compatible with well known RNIC cards and software. Additionally, it provides low latency FPGA implementation of RoCE v2 at 100 Gbps throughput.

IP Features

- Fully compatible with known RNIC products and soft RoCE implementations (RoCE v2)
- **100 Gb/s** Throughput, under **2 usec** latency (roundtrip)
- Configurable RDMA Queue pairs. 1023 or more
- Hardware retransmission and reordering
- Customizable IP

GROVF RDMA supports:

- Hardware operated RC, XRC, RD, UC, UD services
- Incoming and outgoing SEND, RDMA READ, RDMA WRITE
- Memory protection domains implemented in FPGA and ECN
- 3rd party MAC and DMA IPs
- Standard Verbs API on Host Machine
- Dynamic configuration using Verbs API

GROVF Architecture

The solution is a soft IP implementing RDMA over Converged Ethernet protocol. It consists of FPGA IP integrated with MAC and DMA, plus the host CPU drivers. The solution complies with Channel Adapter and RoCE v2 requirements as stated in the IB specification. Below is the simplistic architectural overview of the system. The data plane and reliable communication is hardware offloaded and the implementation does not include CPU cores in FPGA.