FPGAConfigurationSubsystem

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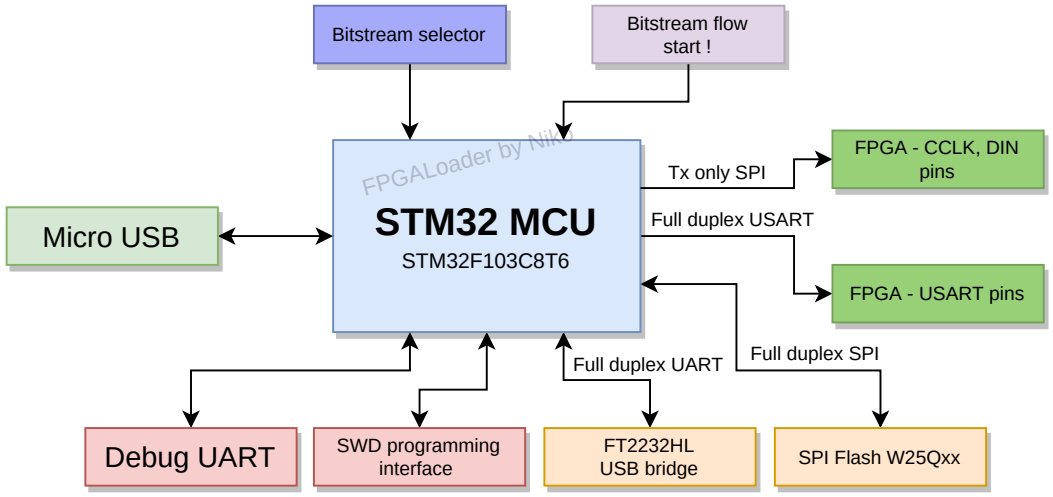
On-board FPGA bitstream loader

block diagram:



Soldered connectors	Button	Other chip
Pinout on PCB - no connector	DIP Switch	FPGA

How it works?

- Device waits for user action
- User can communicate with STM32 using USB-CDC or UART
- User can select a bitstream(by UART, USB command, or button)
- When user starts bitstream flow(by UART, USB command, or button) - data is sent to FPGA
- User can write a new bitstream(s) to SPI Flash
  using an USB or UART, with a special PC application which
  interacts with STM32 on-chip firmware
- User also can send/receive an arbitrary data in USART to/from FPGA (only when bitstream was loaded)

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