Total Items	39
Pass Items	38
Fail Items	1
NY Items	0

Section Main Title  1. Wat for reset and clock stable  2. Road value of 4 register  1. Road default value  2. Water annothing with default value mention in RTL  spec.  1. Water for reset and clock stable  2. Write random value of 4 register  3. Road and Write value check.  3. Road value of 1 register  4. Road value of 1 register  4. Water for reset and clock stable  2. Write random value of 1 register  3. Road value of 1 register  4. Water for reset and clock stable  2. Write data Road to 10 Extreptor  Person condition. Check value mention in RTL  spec.  1. Water for reset and clock stable  2. Write data Road to 10 Extreptor  3. White facts are for a clock stable  3. White data Road to 10 Extreptor  4. Water interrupt in TSR register  4. Water facts and clock stable  5. Write data Road to 15 Extreptor  9. Write data Road to 15 Extreptor  1. Write data Road to 15 Extreptor  2. Write data Road to 15 Extreptor  1. Write data Road to 15 Extreptor  1. Write data Road to 15 Extreptor  2. Road value of 15 Extreptor  2. Road value of 15 Extreptor  2. Road value of 15 Extreptor  2. Count from 0, no divide 19 2  2. Write data Road to 11 Extreptor  2. Write data Road to 11 Extreptor  2. Write data Road to 11 Extreptor  1. Water for reset and clock stable  2. Write data Road to 11 Extreptor  2. Write data Road to 11 Extreptor  3. Write data Road to 11 Extreptor  4. Water for reset and clock stable  2. Write data Road to 11 Extreptor  2. Write data Road to 11 Extreptor  3. Write data Road to 11 Extreptor  4. Water for reset and clock stable  2. Write data Road to 11 Extreptor  3. Write data Road to 11 Extreptor  4. Water for r	18/9 18/9 18/9	Remark
1. Walt for reset and clock stable 2. Read value of register Plass condition: Check value mention in RTL plant for reset and clock stable 1. Read and Write value check 1. Walter random value of a register Plass condition: Check value mention in RTL Plant for reset and clock stable 1. Walter random value of a register Plass condition: Check value matching 1. Walter random value of a register Plass condition: Check value matching 1. Walter random value of a register Plass condition: Check value matching with default value mention in RTL 1. Check reserved register 1. Walter reset and clock stable 2. Writer random value of a register 4. Read value of register 4. Read value of register 4. Read value of reserved register 7. Writer creat and clock stable 2. Writer random value of reserved register 8. Read value of reserved register 9. Secondition: Check value equal is 0 1. Walter creat and clock stable 2. Writer random value of reserved register Plass condition: Check value equal is 0 1. Walter creat and clock stable 2. Write random value of reserved register Plass condition: Check value equal is 0 1. Walter creat and clock stable 2. Write data 8 Poll to 15 Register 4. Walter interrupt is 15 Register 6. Read value of 15 Register 7. Write data 8 Poll to 15 Register 9. Write data 8 Poll to 15 Register 1. Second value of 15 Register 1. Walter provided value of 15 Register 1. Walter provided value of 15 Register 1. Read value of 15 Register 1. Read value of 15 Register 1. Read value of 15 Register 1. Walter provided value of 15 Register 1. Walter	18/9	
2. Read value of a register Pass condition. Check value matching with default value mention in RTL spec.  1. Wall for reset and clock stable 2. Write random value of 4 register 3. Read and Write value check 3. Read value of 1 register 4. Read value of Register Pass condition. Check value matching of the special value of the register Pass condition. Check value matching with default value mention in RTL spec.  1. Wall for reset and clock stable 2. Write random value of 4 register 3. Read value of 4 register Pass condition. Check value matching with default value mention in RTL spec.  1. Wall for reset and clock stable 2. Write random value of 4 register Pass condition. Check value matching with default value mention in RTL spec.  1. Wall for reset and clock stable 2. Write class Bit of 1 register Pass condition. Check value read register reg., reserved_test High Directed Ngayên Vy PASSED  1. Wall for reset and clock stable 2. Write class Bit of 1 to Title register Pass condition. Check value register reg., reserved_test High Directed Ngayên Vy PASSED  1. Wall for reset and clock stable 2. Write class Bit of 1 to Title register 4. Wall interrupt is asserted 5. Write class Bit of 1 to Title register 4. Wall interrupt is asserted 5. Write class Bit of 1 to Title register 9. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 2. Write class Bit of 1 to Title register 3. Write class Bit of 1 to Title register 1. Write class Bit of 1 to Title register 2. Write class Bit of 1 to Title register 3. Write class Bit of 1 to Title register 3. Write class Bit of 1 to Title register 4. Wall interrupt is asserted 4. Wall interrupt is asserted 4. Wall interrupt is asserted 5. Write class Bit of 1 to Title register 2. Write class Bit of 1 to Title register 3. Write class Bit of 1 to Title register 3. Write class Bit of 1 to Title regis	18/9	
Pass condition: Check white matching with default value mention in RTL spec  1. Walf for reset and clock stable 2. Writer andom value of 4 register 3. Reset on the fly check 2. Writer andom value of 4 register 4. Reset and with for reset and clock stable 2. Writer andom value of 4 register 3. Reset on the fly check 4. Reset on the fly check 4. Reset on the fly check 4. Reset on the fly check 5. Reset on the fly check 6. Reset on the fly check 6. Reset of value of 4 register 7. Walf for reset and clock stable 2. Writer andom value of 8 register 8. Reset on the fly check 9. Reset of value of 4 register 9. Reset on the fly check 9. Writer andom value of 8 register 9. Reset on the fly check 1. Walf for reset and clock stable 2. Writer andom value of reserved register 7. Reset value of 8 register 9. Reset value of 8 register 9. Reset value of 8 register 9. Write data 8 Roll to 10 register 1. Walf for reset and clock stable 1. Walf for reset and clock stable 2. Write data 8 Roll to 10 register 9. Write data 8 Roll to 10 register 1. Write data 8 Roll to 10 register 9. Write data 8 Roll to 10 register 1. Write data 8 Roll to 10 register 9. Write data 8 Roll to 10 register 1. Write data 8 Roll to 10 register	18/9	
PASSED  1.2 Read and Write value check  1.2 Read and Write value check  1.3 Read value of a register  1.3 Read value of a register  1.3 Read value of a register  1.4 Check reserved register  1.4 Check reserved register  1.5 Check interrupt in TSR register  1.5 Check interrupt in TSR register  1.5 Check interrupt in TSR register  1.6 Read value of 15 register  1.7 Write data 8 Pol to 15 register  1.8 Read value of 15 register  1.9 Write data 8 Pol to 10 TSR register  1.9 Write data 8 Pol to 10 TSR register  1.1 Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall interrupt is asserted  1.1 Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall interrupt is asserted  1.1 Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  4. Wall interrupt is asserted  5. Write data 8 Pol to 10 TSR register  7. Write data 8 Pol to 10 TSR register  1.5 Check interrupt in TSR register  1.5 Check interrupt in TSR register  2. Count from 0, no divide  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall interrupt is asserted  1. Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall interrupt is asserted  5. Write data 8 Pol to 10 TSR register  9. Write data 8 Pol to 10 TSR register  1. Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  1. Wall for reset and clock stable  2. Write data 8 Pol to 10 TSR register  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall 8 Write Program of the Write Write data 8 Pol to 10 TSR register  2. Write data 8 Pol to 10 TSR register  3. Write data 8 Pol to 10 TSR register  4. Wall 8 Write Program of the Write Write data 8 Pol to 10 TSR register  4. Wall 8 Write Wr	18/9	
1.2 Read and Write value check 2. Write random value of 4 register 3. Read value of 4 register 1.3 Reset on the fly check 2. Write random value of 4 register 3. Reset on the fly check 4. Read value of 4 register 3. Reset on the fly check 4. Read value of 4 register 3. Reset on the fly check 4. Read value of 4 register 5. Reset value of 8 register 6. Read value of 8 register 6. Read value of 1 register 7. I valid for reset and clock stable 2. Write random value of 4 register 7. Read value of 1 reserved register 8. Read value of reserved register 8. Read value of reserved register 9. Reset value equal is 0 1. Valid for reset and clock stable 2. Write data 8 bit 1 to 1 Register 3. Write data 8 bit 1 to 1 Register 4. Wall interrupt to assertice 6. Read value of 158 register 7. Write data 8 bit 1 to 1 Register 8. Read value of 158 register 9. Write data 8 bit 1 to 1 Register 1. Wall for reset of 158 register 1. Wall for reset of 158 register 1. With data 8 bit 1 to 1 Register 1. Wall for reset of 158 register 1. Write data 8 bit 1 to 1 Register 1.	18/9	
1.2 Read and Wirite value check 2. Write random value of a register Pess condition. Check value matching 1.3 Revisit on the fly check 3. Reset value of a register A. Read value of a register A. Wall interrupt in SR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Read value of TSR register A. Wall interrupt is asserted A. Read value of TSR register A. Wall interrupt is asserted as	18/9	
1. Zeroal and Write value Check  1. Read value of 4 register Plass condition. Check value matching  1. Wait for reset and clock stable 2. Write random value of 4 register Plass condition. Check value matching with default value mention in RTL spec.  1. Wait for reset and clock stable 2. Write random value of 1 register Plass condition. Check value matching with default value mention in RTL spec.  1. Wait for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register 4. Read value of reserved register 7. Read value of reserved register 8. Read value of reserved register 9. Wait interrupt in Check value well as 0 to 10 Tis register 9. Write data 8 Dot 10 Tis register 9. Write data 8 Dot 10 Tis register 1. Some search and the search of t	18/9	
1. Zeroal and Write value Check  1. Read value of 4 register Plass condition. Check value matching  1. Wait for reset and clock stable 2. Write random value of 4 register Plass condition. Check value matching with default value mention in RTL spec.  1. Wait for reset and clock stable 2. Write random value of 1 register Plass condition. Check value matching with default value mention in RTL spec.  1. Wait for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register 4. Read value of reserved register 7. Read value of reserved register 8. Read value of reserved register 9. Wait interrupt in Check value well as 0 to 10 Tis register 9. Write data 8 Dot 10 Tis register 9. Write data 8 Dot 10 Tis register 1. Some search and the search of t	18/9	
Pass condition: Check value matching  1. Write reset and clock stable 2. Write random value of 4 register 3. Reset systyme 4. Read value of 14 register Pass condition: Check value matching with default value mention in RTL spec 1. Write random value of reserved register Pass condition: Check value matching with default value mention in RTL spec 1. Write or set and clock stable 2. Write random value of reserved register Pass condition: Check value equal is 0 1. Write for reset and clock stable 2. Write data 8 7b 10 To Tis reset and clock stable 2. Write data 8 7b 10 To Tis register A Wall interrupt is asserted 3. Write data 8 7b 10 To Tis register 4. Wall interrupt is asserted 5. Write data 8 7b 10 To Tis register 6. Read value of Tis register 7. Write data 8 7b 10 To Tis register 1. Wall interrupt is asserted 1. Write fortal a 7b 10 To Tis register 1. Write fortal a 7b 10 To Tis register 1. Write fortal a 7b 10 To Tis register 1. Write fortal a 7b 10 To Tis register 1. Write fortal a 7b 10 To Tis register 1. Write fortal a 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 1. Write data 8 7b 10 To Tis register 2. Count from 0, no divide 1. Write fortal a To Tis register 2. Write data 8 7b 10 To Tis register 2. Write data 8 7b 10 To Tis register 2. Write data 8 7b 10 To Tis register 2. Write data 8 7b 10 To Tis register 2. Write data 8 7b 10 To Tis register 3. Write data 8 7b 10 To Tis register 4. Write data 8 7b 10 To Tis register 4. Write data 8 7b 10 To Tis register 5. Write data 8 7b 10 To Tis register 6. Read valu	18/9	
1. Wait for reset and clock stable 2. Write random value of 4 register 3. Reset system 4. Read value of 1 register 1.4. Check reserved register 1.4. Check reserved register 1.4. Check reserved register 1.4. Check reserved register 1.5. Check interrupt in TSR register 1.5. Check interrupt in TSR register 1.5. Check interrupt in TSR register 1.6. Read value of 1 register 1.7. Write data 8 bb1 to 17 Register 1.8. Read value of 1 register 1.9. Write data 8 bb1 to 18 Register	18/9	
2. Write random value of 4 register 3. Reset on the fly check 3. Reset system 4. Read value of 4 register Pass condition. Check value matching with default value mention in RTL spec 1. Wall for reset and clock stable 2. Write random value of reserved register Pass condition. Check value of reserved register 3. Read value of reserved register Pass condition. Check value of register 1. Wall for reset and clock stable 2. Write data 8 brit to 10 Fire register 3. Write data 8 brit to 10 Fire register 3. Write data 8 brit to 10 Fire register 4. Wall interrupt is asserted 5. Write data 8 brit to 10 Fire register 6. Read value of 15 Register 6. Read value of 15 Register 7. Write data 8 brit to 10 Fire register 10. Wall interrupt is asserted 11. Write data 8 brit to 10 Fire register 12. Read value of 15 Register 13. Write data 8 brit to 10 Fire register 14. Read value of 15 Register 15. Check interrupt in TSR register 16. Wall interrupt is asserted 17. Write data 8 brit to 10 Fire register 18. Read value of 15 Register 19. Write data 8 brit to 10 Fire register 10. Wall interrupt is asserted 11. Write data 8 brit to 10 Fire register 12. Read value of 15 Register 13. Write data 8 brit to 10 Fire register 14. Read value of 15 Register 15. Write data 8 brit to 10 Fire register 16. Write data 8 brit to 10 Fire register 17. Write data 8 brit to 10 Fire register 18. Write data 8 brit to 10 Fire register 19. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 2. Write data 8 brit to 10 Fire register 3. Write data 8 brit to 10 Fire register 4. Wall 300 posedge ker_cik 5. Read value of 15 Register 5. Write data 8 brit to 10 Fire register 6. Read value of 15 Register 7. Write data 8 brit to 10 Fire register 7. Write data 8 brit to 10 Fire register 8. Write data 8 brit do 10 Fire register 9. Write data 8 brit do 10 Fire register 9. Write data 8	18/9	
3. Reset on the fly check 4. Read value of 1 register Pass condition: Check value matching with default value mention in RTL spec 1. Wall for reset and clock stable 2. Write radion value of reserved register 3. Read value of reserved register 1. Wall for reset and clock stable 2. Write value equal is 0 1. Wall for reset and clock stable 2. Write data 8011 to TR register 3. Write data 8010 to TSR register 4. Wall interrupt is asserted 5. Write data 8010 to TSR register 6. Read value of TSR register 7. Write data 8010 to TSR register 8. Read value of TSR register 1. Write data 8010 to TSR register 9. Write data 8010 to TSR register 1. Wall for reset and clock stable 2. Write data 8010 to TSR register 2. Write data 8010 to TSR register 2. Write data 8010 to TSR register 3. Write data 8010 to TSR register 4. Wall 300 posedege ker_dik 5. Read value of TSR register 5. Register 6. Reg	18/9	
4. Read value of 14 register Pass condition: Check value matching with default value mention in RTL spec. 1. Wall for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register 3. Read value of reserved register 4. Wall in reset and clock stable 2. Write data 8 Phol to TSR register 3. Write data 8 Phol to TSR register 4. Wall interrupt is asserted 5. Write data 8 Phol to TSR register 7. Write data 8 Phol to TSR register 9. Write data 8 Phol to TSR register 10. Wall interrupt is asserted 11. Write data 8 Phol to TSR register 12. Read value of TSR register 13. Write data 8 Phol to TSR register 14. Wall interrupt is asserted 15. Check interrupt in TSR register 16. Read value of TSR register 17. Write data 8 Phol to TSR register 18. Read value of TSR register 19. Write data 8 Phol to TSR register 10. Wall interrupt is asserted 11. Write data 8 Phol to TSR register 12. Read value of TSR register 13. Write data 8 Phol to TSR register 14. Read value of TSR register 15. Check interrupt in TSR register is a Phologometric interrupt in TSR register 16. Count up 17. Write data 8 Phol to TSR register 18. Write data 8 Phol to TSR register 19. Wall for reset and clock stable 2. Write data 8 Phol to TSR register 2. Write data 8 Phol to TSR register 3. Write data 8 Phol to TSR register 4. Wall 300 posedege ker, clik 5. Read value of TSR register 7. Write data 8 Phol to TSR register 8. Read value of TSR register 9. Wall of TSR register 9. Wall of TSR register 19. Wall for reset and clock stable 2. Write data 8 Phol to TSR register 9. Wall of TSR register 9. Wall o	18/9	
1.4 Check reserved register  1.4 Check reserved register  1. Wait for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register 4. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 3. Read value of reserved register 4. Wait interrupt in Check value equals to 4. Wait interrupt in Sax register 4. Wait interrupt in Sax register 5. Write data 8 bit 10 filt register 6. Read value of TSR register 7. Write data 8 bit 10 filt register 9. Write data 8 bit 10 filt register 10. Wait interrupt in TSR register 10. Wait interrupt in TSR register 11. Wait interrupt in TSR register 12. Read value of TSR register 13. Write data 8 bit 10 filt register 14. Read value of TSR register 15. Check interrupt in TSR register 16. Read value of TSR register 17. Write data 8 bit 10 filt register 18. Read value of TSR register 19. Read value of TSR register 19. Read value of TSR register 10. Wait interrupt in TSR register 11. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 13. Write data 8 bit 10 filt register 14. Read value of TSR register 15. Count from 0, no divide 16. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 3. Write data 8 bit 10 filt register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 7. Write data 8 bit 10 filt register 8. Sead value of TSR register 9. Write data 8 bit 10 filt register 9. Write data 8 bit 10 filt register 10. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 3. Write data 8 bit 10 filt register 9. Seas condition: Check interrupt is asserted and read value is 8 hot 11. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 9. Seas condition: Check interrupt is asserted and read value is 8 hot 10. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 9. Seas condition: Check interrupt is asserted and read value is 8 hot 11. Wait for reset and clock stable 2. Write data 8 bit 10 filt register 19. Write data 8 bit 10 filt register 19. Wait double 9.	18/9	
Pass condition: Check value metathing with default value mention in RTL spec  1. Walf for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register 4. Walf for reset and clock stable 2. Write data 8 Phot 10 TE register 3. Write data 8 Phot 10 TE register 4. Walf interrupt is asserted 5. Write data 8 Phot 10 TE register 6. Read value of TSR register 7. Write data 8 Phot 10 TSR register 8. Read value of TSR register 9. Write data 8 Phot 10 TSR register 1. Walf for reset and clock stable 2. Write data 8 Phot 10 TSR register 2. Counter combine with divisor test 2. Count up  1. Walf for reset and clock stable 2. Write data 8 Phot 10 TSR register 3. Write data 8 Phot 10 TSR register 4. Walf 300 posedege ker_clk 5. Read value of TSR register 1. Walf for reset and clock stable 2. Write data 8 Phot 10 TSR register 3. Write data 8 Phot 10 TSR register 4. Walf 300 posedege ker_clk 5. Read value of TSR register 7. Write data 8 Phot 10 TSR register 8. Read value of TSR register 9. Ses condition: Check interrupt is asserted and read value is 8 Phot 1. Walf for reset and clock stable 2. Write data 8 Phot 10 TSR register 8. Sead value of TSR register 9. Sead value of TSR register 1. Walf for reset and clock stable 2. Write data 8 Phot 10 TSR register 1. Walf of opposedege ker_clk 5. Read value of TSR register 1. Walf do posedege ker_clk 5. Read value of TSR register 1. Walf do posedege ker_clk 5. Read value of TSR register 1. Walf do posedege ker_clk 5. Read value of TSR register 1. Walf do posedege ker_clk 5. Re		
Spec   1.4   Check reserved register   1.4   Write reset and clock stable   2. Write random value of reserved register   1.4   Check reserved register   2. Write random value of reserved register   1.4   Check reserved register   2. Write data 8 hot of the Check value equal is 0   1. Walf for reset and clock stable   2. Write data 8 hot of the Check and the Check reserved register   2. Write data 8 hot of the Check reserved register   2. Write data 8 hot of the Check reserved register   3. Write data 8 hot of the Check reserved register   3. Write data 8 hot of the Check reserved register   3. Write data 8 hot of the Check reserved register   4. Walt interrupt is asserted   5. Write data 8 hot of the Check register   6. Read value of TSK register   7. Write data 8 hot of the Check register   7. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Write data 8 hot of the Check register   1. Walt for reset and clock stable   2. Write data 8 hot of the Check register   2. Write data 8 hot of the Check register   2. Write data 8 hot of the Check register   3. Write data 8 hot of the Check register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   2. Write data 8 hot of the Check register   3. Write data 8 hot of the Check register   3. Write data 8 hot of the Check register   3. Write data 8 hot of the Check register   4. Walt 300 posedege ker_clk   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk   5. Read value of TSK register   4. Walt 300 posedege ker_clk		
1. Wait for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register Pass condition: Check value equal is 0  1. Wait for reset and clock stable 2. Write data 8 bit 1 to 11E register 3. Write data 8 bit 1 to 11E register 4. Wait interrupt is asserted 5. Write data 8 bit 1 to 11E register 7. Write data 8 bit 1 to 11E register 1.5. Check interrupt in TSR register 1.5. Check interrupt in TSR register 1.5. Check interrupt in TSR register 1.6. Read value of TSR register 1.7. Write data 8 bit 1 to 11E register 1.8. Read value of TSR register 1.9. Wait interrupt is asserted 1.1. Write data 8 bit 1 to 11E register 1.1. Write data 8 bit 1 to 11		
2. Write random value of reserved register 3. Read value of reserved register Pass condition: Check value equal is 0  1. Wait for reset and clock stable 2. Write data 8 'D1 to Tix register 3. Write data 8 'D1 to Tix register 4. Walt interrupt is asserted 5. Write data 8 'D1 to Tix register 7. Write data 8 'D1 to Tix register 7. Write data 8 'D1 to Tix register 7. Write data 8 'D1 to Tix register 9. Write data 8 'D1 to Tix register 10. Walt interrupt is asserted 11. Write data 8 'D00 to Tix register 12. Read value of Tix register 13. Write data 8 'D00 to Tix register 14. Read value of Tix register 15. Check interrupt in Tix register 16. Check interrupt in Tix register 17. Write data 8 'D00 to Tix register 18. Read value of Tix register 19. Write data 8 'D00 to Tix register 19. Write data 8 'D00 to Tix register 11. Write data 8 'D00 to Tix register 12. Read value of Tix register 13. Write data 8 'D00 to Tix register 14. Read value of Tix register 15. Count from 0, no divide 10. Walt interrupt is asserted of the value of tix register 19. Write data 8 'D00 to Tix register 10. Walt for reset and clock stable 10. Write data 8 'D00 to Tix register 10. Write dat		
1. See a value of reserved register    See a value of reserved register   Pass condition. Check value equal is 0		
S. Read value of reserved register Pass condition. Check value equals to 0  1. Wali for reset and clock stable 2. Write data 8 thol to TCR register 3. Write data 8 thol to TCR register 6. Read value of TSR register 7. Write data 8 thol to TSR register 1. S. Check interrupt in TSR register 8. Read value of TSR register 9. Write data 8 thol to TSR register 10. Wali interrupt is asserted 11. Write data 8 thol to TSR register 12. Read value of TSR register 13. Write data 8 thol to TSR register 14. Read value of TSR register 15. Check interrupt in TSR register 16. Wali interrupt is asserted in Wali interrupt is a serted in Wali interrupt in TSR register 17. Write data 8 thol to TSR register 18. Write data 8 thol to TSR register 19. Write data 8 thol to TSR register 19. Write data 8 thol to TSR register 11. Write data 8 thol to TSR register 12. Read value of TSR register 13. Write data 8 thol to TSR register 14. Read value of TSR register 15. Write data 8 thol to TSR register 16. Write data 8 thol to TSR register 17. Write data 8 thol to TSR register 18. Write data 8 thol to TSR register 19. Write data 8 thol to TSR regist		
1. Walt for reset and clock stable 2. Write data 8 hot to TCR register 3. Write data 8 hot to TCR register 4. Walt interrupt is asserted 5. Write data 8 hot to TSR register 6. Read value of TSR register 7. Write data 8 hot to TSR register 8. Read value of TSR register 9. Write data 8 hot to TSR register 10. Walt interrupt is asserted 11. Write data 8 hot to TSR register 12. Read value of TSR register 13. Write data 8 hot to TSR register 13. Write data 8 hot to TSR register 13. Write data 8 hot to TSR register 14. Read value of TSR register 15. Write data 8 hot to TSR register 16. Write data 8 hot to TSR register 17. Write data 8 hot to TSR register 18. Write data 8 hot to TSR register 19. Write data 8 hot to TSR register 19. Write data 8 hot to TSR register 20. Count up  10. Walt for reset and clock stable 20. Write data 8 hot to TCR register 21. Write data 8 hot to TCR register 22. Count from 0, no divide 23. Write data 8 hot to TCR register 24. Walt 300 posedege ker_clk 25. Read value of TSR register 26. Write data 8 hot to TCR register 27. White data 8 hot to TCR register 28. Write data 8 hot to TCR register 29. Write data 8 hot to TCR register 29. Write data 8 hot to TCR register 29. Write data 8 hot to TCR register 20. Write data 8 hot to TCR register 21. Walt for reset and clock stable 22. Write data 8 hot to TCR register 23. Write data 8 hot to TCR register 24. Walt 300 posedege ker_clk 25. Read value of TSR register 26. Count from 0, divide by 2 27. Count from 0, divide by 2 28. Count from 0, divide by 2 39. Write data 8 hot to TCR register 40. Walt 600 posedege ker_clk 50. Read value of TSR register 50. Write data 8 hot of TSR register 60. Register 60. Read value of TSR register 6	18/9	
2. Write data 8*D1 to TE register 3. Write data 8*D1 to TCR register 4. Walt interrupt is asserted 5. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 8. Read value of TSR register 9. Write data 8*D0 to TSR register 10. Walt interrupt is asserted 11. Write data 8*D0 to TSR register 12. Read value of TSR register 13. Write data 8*D0 to TSR register 14. Read value of TSR register 15. Walt for reset and clock stable 2. Count from 0, no divide 1 Write data 8*D0 to TE register 3. Write data 8*D0 to TE register 4. Walt 100 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*D0 to TER register 1. Walt for reset and clock stable 2. Write data 8*D0 to TER register 9. Write data 8*D0 to TER register 1. Walt for reset and clock stable 2. Write data 8*D0 to TER register 9. Write data 8*D0 to TER register 1. Walt for reset and clock stable 2. Write data 8*D0 to TER register 9. Write data 8*D0 to TER register 9. Write data 8*D0 to TER register 1. Walt for reset and clock stable 2. Write data 8*D0 to TER register 9. Walt 6*D0 posedege ker_clk 9. Walt 6*D0 posedeg	18/9	
2. Write data 8*D1 to TE register 3. Write data 8*D1 to TCR register 4. Wait interrupt is asserted 5. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 7. Write data 8*D0 to TSR register 8. Read value of TSR register 9. Write data 8*D0 to TSR register 10. Wait interrupt is asserted 11. Write data 8*D0 to TSR register 12. Read value of TSR register 13. Write data 8*D0 to TSR register 14. Read value of TSR register 15. Wait for reset and clock stable 2.11 Count up  1. Wait for reset and clock stable 2. Write data 8*D0 to TGR register 3. Write data 8*D0 to TGR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*D0 to TGR register 2. Count from 0, no divide by 2  2. Count from 0, divide by 2  2. Count from 0, divide by 2  Directed Nguyễn Vy PASSED	18/9	
3. Write data 8*D01 to TCR register 4. Walt interrupt is asserted 5. Write data 8*D01 to TSR register 6. Read value of TSR register 7. Write data 8*D01 to TSR register 8. Read value of TSR register 10. Walt interrupt is asserted 11. Write data 8*D01 to TSR register 12. Read value of TSR register 13. Write data 8*D01 to TSR register 14. Read value of TSR register 15. Write data 8*D01 to TSR register 16. Walt interrupt is asserted 17. Write data 8*D01 to TSR register 18. Write data 8*D01 to TSR register 19. Asserted value of TSR register 19. Asserted value of TSR register 19. Write data 8*D01 to TSR register 19. Write data 8*D01 to TSR register 19. Write data 8*D01 to TSR register 2.1 Count up  1 Walt for reset and clock stable 2. Write data 8*D01 to TGR register 3. Write data 8*D01 to TGR register 4. Walt 300 possedege ker_Clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*D01 1. Walt for reset and clock stable 2. Write data 8*D01 to TGR register 4. Walt 300 possedege ker_Clk 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8*D01 to TGR register 8. Read value of TSR register 9. Souther combine with divisor test 6. Read value of TSR register 7. Write data 8*D01 to TGR register 8. Read value of TSR register 8. Read value of TSR register 9. Write data 8*D01 to TGR register	18/9	
4. Wait interrupt is asserted 5. Write data 8*h00 to TSR register 6. Read value of TSR register 7. Write data 8*h01 to TSR register 8. Read value of TSR register 9. Write data 8*h01 to TSR register 10. Wait interrupt is asserted 11. Write data 8*b01 to TSR register 12. Read value of TSR register 13. Write data 8*b10 to TSR register 14. Read value of TSR register 15. Write data 8*b10 to TSR register 16. Wait interrupt is asserted 17. Write data 8*b10 to TSR register 18. Read value of TSR register 19. Write data 8*b10 to TSR register 19. Write data 8*b10 to TSR register 2.1 Count from 0, no divide 11. Wait for reset and clock stable 2. Write data 8*b10 to TSR register 3. Write data 8*b10 to TSR register 4. Wait 300 posedege ker_cik 5. Read value of TSR register 4. Write data 8*b10 to TSR register 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8*b10 to TSR register 7. Write data 8*b10 to TSR register 8. Write data 8*b10 to TSR register 9. Write data 8*b10 to TSR register 10. Wait for reset and clock stable 11. Wait for reset and clock stable 12. Write data 8*b10 to TSR register 13. Write data 8*b10 to TSR register 14. Wait 600 posedege ker_cik 15. Read value of TSR register 16. Read value of TSR register 17. Write data 8*b10 to TSR register 18. Write data 8*b10 to TSR register 19. Write data 8*b10 to TSR registe	18/9	
5. Write data 8'h00 to TSR register 6. Read value of TSR register 7. Write data 8'b10 to TSR register 8. Read value of TSR register 9. Write data 8'b10 to TSR register 10. Walt interrupt in TSR register 11. Write data 8'b10 to TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register 15. Count up  1. Walt for reset and clock stable 2. Write data 8'b10 to TIR register 3. Write data 8'b10 to TSR register 4. Walt 300 posedege ker_clk 5. Read value of TSR register 2.1.2 Count from 0, no divide by 2  2.1.2 Count from 0, divide by 2  1. Walt for reset and clock stable 2. Write data 8'b10 to TSR register 3. Write data 8'b10 to TSR register 4. Walt 300 posedege ker_clk 5. Read value of TSR register 3. Write data 8'b10 to TSR register 4. Walt 300 posedege ker_clk 5. Read value of TSR register 4. Walt 500 posedege ker_clk 5. Read value of TSR register 4. Walt for reset and clock stable 2. Write data 8'b10 to TSR register 3. Write data 8'b10 to TSR register 4. Walt 500 posedege ker_clk 5. Read value of TSR register 6. Read value of TSR register 6. Read value of TSR register 7. Write data 8'b10 to TSR register 8. Read value of TSR register 9. PASSED 8. Read value of TSR register 9. PASSED	18/9	
6. Read value of TSR register 7. Write data 8'b01 to TSR register 9. Write data 8'b01 to TSR register 10. Walt interrupt is asserted 11. Write data 8'b01 to TSR register 12. Read value of TSR register 13. Write data 8'b01 to TSR register 14. Read value of TSR register 14. Read value of TSR register 15. Write data 8'b01 to TSR register 16. Read value of TSR register 17. Write data 8'b01 to TSR register 18. Write data 8'b01 to TSR register 19. Count up 11. Walt for reset and clock stable 2. Write data 8'b01 to TSR register 2. Write data 8'b01 to TSR register 3. Write data 8'b01 to TSR register 4. Walt 300 posedege ker_clk 5. Read value of TSR register 4. Walt 300 posedege ker_clk 5. Read value of TSR register 4. Walt data 8'b01 to TSR register 4. Walt data 8'b01 to TSR register 6. Read value of TSR register 7. Write data 8'b01 to TSR register 8. Read value of TSR register 9. Write data 8'b01 to TSR register 9. Write data 8'b01 to TSR register 19. Write data 8'b01 to TSR register 19. Walt for reset and clock stable 2. Write data 8'b01 to TSR register 19. Walt for reset and clock stable 20. Write data 8'b01 to TSR register 20. Walt data 8'b01 to TSR register 21. Count from 0, divide by 2 3. Write data 8'b01 to TSR register 4. Walt data 8'b01 to TSR register 21. Walt for reset and clock stable 22. Write data 8'b01 to TSR register 3. Write data 8'b01 to TSR register 4. Walt data 8'b01 to TSR register 4. Walt data 8'b01 to TSR register 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8'b01 to TSR register 8. Read value of TSR register 8. Read value of TSR register 8. Read value of TSR register 9. Write data 8'b01 to TSR register 9. Walt data 8'b01	18/9	
7. Write data 8'b01 to TSR register reg_tsr_test Directed Nguyễn Vy PASSED  1.5 Check interrupt in TSR register 8. Read value of TSR register 10. Wait interrupt is asserted 11. Write data 8'b01 to TSR register 12. Read value of TSR register 13. Write data 8'b01 to TSR register 13. Write data 8'b01 to TSR register 14. Read value of TSR register 14. Read value of TSR register 15. Wait for reset and clock stable 2. Write data 8'b01 to TSR register 3. Write data 8'b01 to TSR register 3. Write data 8'b01 to TSR register 3. Write data 8'b01 to TSR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b01 to TSR register 7. Write data 8'b01 to TSR register 8. Write data 8'b01 to TSR register 9. Write data 8'	18/9	
1.5 Check interrupt in TSR register  8. Read value of TSR register 9. Write data 8'b11 to TCR register 10. Wait interrupt is asserted 11. Write data 8'b00 to TSR register 12. Read value of TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register 14. Read value of TSR register 15. Write data 8'b10 to TSR register 16. Wait interrupt is asserted 17. Write data 8'b10 to TSR register 18. Write data 8'b10 to TSR register 19. Write data 8'b10 to TSR register 2. Count up  1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 4. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 5. Read value of TSR register 4. Write data 8'b10 to TCR register 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8'b10 to TCR register 7. Write data 8'b10 to T	18/9	
1.5 Check interrupt in TSR register  8. Read value of TSR register 9. Write data 8'b11 to TCR register 10. Wait interrupt is asserted 11. Write data 8'b00 to TSR register 12. Read value of TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register 14. Read value of TSR register 15. Write data 8'b10 to TSR register 16. Wait interrupt is asserted 17. Write data 8'b10 to TSR register 18. Write data 8'b10 to TSR register 19. Write data 8'b10 to TSR register 2. Count up  1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Wait 300 poseders we're.lk 5. Read value of TSR register 4. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 5. Read value of TSR register 4. Write data 8'b10 to TCR register 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8'b10 to TCR register 7. Write data 8'b10 to T	18/9	
9. Write data 8°b1 to TCR register 10. Wait interrupt is asserted 11. Write data 8°b0 to TSR register 12. Read value of TSR register 13. Write data 8°b0 to TSR register 14. Read value of TSR register 14. Read value of TSR register 15. Write data 8°b0 to TSR register 16. Read value of TSR register 17. Count up  1. Wait for reset and clock stable 2. Write data 8°b0 to TER register 3. Write data 8°b0 to TER register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 2. Write data 8°b0 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register 2. Write data 8°b0 to TCR register 4. Wait 500 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register		
10. Walt interrupt is asserted 11. Write data 8'b00 to TSR register 12. Read value of TSR register 13. Write data 8'b01 to TSR register 14. Read value of TSR register 14. Read value of TSR register Pass condition: Check underflow bit and overflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register Association: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Read value of TSR register 7. PASSED 8. PASSED 8. PASSED 9. PASSED		
11. Write data 8'b00 to TSR register 12. Read value of TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register Pass condition: Check underflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8'b01 to TIC register 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register Pass condition: Check interrupt is asserted and read value is 8'h01  2.1.2 Count from 0, divide by 2  Count from 0, divide by 2  Count from 0, divide by 2  Directed Nguyễn Vy PASSED		
12. Read value of TSR register 13. Write data 8'b10 to TSR register 2 Counter combine with divisor test 2.1 Count up  1. Wait for reset and clock stable 2.1.1 Count from 0, no divide 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check underflow bit is matching  1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  2.1.2 Count from 0, divide by 2  2.1.3 Count from 0, divide by 2  3. Write data 8'b1001 to TCR register 4. Wait for reset and clock stable 2. Write data 8'b1001 to TCR register 3. Write data 8'b1001 to TCR register 4. Wait for reset and clock stable 2. Write data 8'b1001 to TCR register 4. Wait for reset and clock stable 2. Write data 8'b1001 to TCR register 4. Wait for reset and clock stable 2. Write data 8'b1001 to TCR register 4. Wait for reset and clock stable 5. Read value (obs stable on the properties of the properties		
13. Write data 8'b10 to TSR register 14. Read value of TSR register 14. Read value of TSR register Pass condition: Check underflow bit and overflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 300 posedege ker_clk 5. Read value of TSR register register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register A Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 4. Write data 8'b01 to TIE register 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Read value of TSR register 7. Count from 0, divide by 2 7. PASSED 8. PASSED 8. PASSED 9. PASSED 9. PASSED 9. PASSED 9. PASSED 9. PASSED 9. PASSED		
14. Read value of TSR register Pass condition: Check underflow bit and overflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*b01  2.1.2 Count from 0, divide by 2  1. Wait for reset and clock stable 2. Write data 8*b01 to TCR register Pass condition: Check interrupt is asserted and read value is 8*b01  2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TIC register 4. Wait for reset and clock stable 2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TIC register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register		
14. Read value of TSR register Pass condition: Check underflow bit and overflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*b01  2.1.2 Count from 0, divide by 2  1. Wait for reset and clock stable 2. Write data 8*b01 to TCR register Pass condition: Check interrupt is asserted and read value is 8*b01  2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TIC register 4. Wait for reset and clock stable 2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TIC register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register		
Pass condition: Check underflow bit and overflow bit is matching  2 Counter combine with divisor test  2.1 Count up  1. Wait for reset and clock stable 2. Write data 8'b01 to TIC register 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  2.1.2 Count from 0, divide by 2  Count from 0, divide by 2  Pass condition: Check interrupt is asserted and read value is 8'h01  Directed Nguyễn Vy PASSED  A Nguyễn Vy PASSED  Out from 0, divide by 2  A Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register		
2.1. Count up  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 30' posedege ker_clk 5. Read value of TSR register 4. Wait for reset and clock stable can be register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Sead value of TSR register 7. Count from 0, divide by 2 7. Directed Nguyễn Vy 8. PASSED 8. Read value of TSR register 9. PASSED		
2.1.1 Count rom 0, no divide  2.1.1 Count from 0, no divide  3. Write data 8*b01 to TCR register 4. Wait 300 posedege ker_cik 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*h01  1. Wait for reset and clock stable 2. Write data 8*b01 to TIC register 3. Write data 8*b01 to TIC register 4. Wait 600 posedege ker_cik 5. Read value of TSR register 4. Wait 600 posedege ker_cik 5. Read value of TSR register 4. Wait 600 posedege ker_cik 5. Read value of TSR register  4. Wait 600 posedege ker_cik 5. Read value of TSR register		
2.1.1 Count from 0, no divide  2. Write data 8'b01 to TCR register 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register Pass condition: Check interrupt is asserted and read value is 8'h01  2.1.2 Count from 0, divide by 2  Count from 0, divide by 2  Count from 0, divide by 2  I. Wait 600 posedege ker_clk 5. Read value of TSR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Read value of TSR register 7. Wait 600 posedege ker_clk 7. Read value of TSR register 8. Wait 600 posedege ker_clk 9. Read value of TSR register		
2.1.1 Count from 0, no divide  2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b101 to TIE register 7. Write data 8'b101 to TIE register 8. Write data 8'b101 to TIE register 9. Write data 8'b101 to TIE register		
2.1.1 Count from 0, no divide  3. Write data 8'b01 to TCR register 4. Wait 300 posedage ker_lik 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 3. Write data 8'b1001 to TCR register 4. Wait 600 posedage ker_lik 5. Read value of TSR register 2.1.2 Count from 0, divide by 2  Directed Nguyễn Vy PASSED  Nguyễn Vy PASSED  Nguyễn Vy PASSED  S. Read value of TSR register		
2.1.1 Count from 0, no divide  4. Wait 300 posedege ker_clk  5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 600 posedege ker_clk 5. Read value of TSR register 6. Read value of TSR register 7. Write data 8'b01 to TIE register 7. Wait 600 posedege ker_clk 7. Read value of TSR register 8. Wait 400 posedege ker_clk 9. PASSED		
4. Wait 30U posedege ker_cik 5. Read value (cok Interrupt is asserted and read value is 8'h01  1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TIE register 4. Wait 600 posedege ker_cik 5. Read value of TSR register 6. Read value of TSR register	20/9	
Pass condition: Check interrupt is asserted and read value is 8*h01  1. Wait for reset and clock stable 2. Write data 8*b01 to TIE register 3. Write data 8*b1001 to TIE register 4. Wait 600 posedege ker_cik 5. Read value of TSR register  5. Read value of TSR register	20//	
1. Wait for reset and clock stable 2. Write data 8"b01 to TIE register 3. Write data 8"b1001 to TIC register 4. Wait 600 posedege ker_clk 5. Read value of TSR register  5. Read value of TSR register		
1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b1001 to TCR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register		
2. Write data 8'b01 to TIE register 2.1.2 Count from 0, divide by 2  2.1.2 Count from 0, divide by 2  2.1.2 Count from 0, divide by 2  3. Write data 8'b010 to TIE register 4. Wait 600 posedege ker_clk 5. Read value of TSR register  5. Read value of TSR register		
2.1.2 Count from 0, divide by 2 3. Write data 8'b1001 to TQR register 4. Wait 600 posedege ker_cik 5. Read value of TSR register  Directed Nguyễn Vy PASSED		
4. Wait 600 posedege ker_clk  5. Read value of TSR register		
4. Wait out posedegs ker_ak  5. Read value 75R register	20/9	
Pass condition: Check interrupt is asserted and read value is 8'h01		
Mait for reset and clock stable		
2. Write data 8'b01 to TIE register		
3 Write data 9/h10001 to TCP register	L	
2.1.3 Count from 0, divide by 4 S. Wine data of blood to Richestyles and the Capital Count from 0, divide by 4 S. Wait 1040 posedege ker_clk Directed Nguyễn Vy PASSED	20/9 The :	s_ovf signal is NOT LOW after being asserted
5. Read value of TSR register		
Pass condition: Check interrupt is asserted and read value is 8'h01		
1. Wait for reset and clock stable		
2. Write data 8'b01 to TIE register		
3. Write data 8'b11001 to TCR register	20.70	a sufaignal is NOT LOW off b- b
2.1.4 Count from 0, divide by 8 S. Winte data of I from 1 to Reference   Cit   Count from 0, divide by 8   Directed   Nguyễn Vy   PASSED	20/9 The :	s_ovf signal is NOT LOW after being asserted
5. Read value of TDR register		
Pass condition: Check interrupt is asserted and read value is 8'h01		
	+	
Wait for reset and clock stable		
2. Write data 8'b100 to TCR register		
3. Write random value of TDR register		
4 Write data 9'h01 to TIE register	1	
2.1.5 Count from random, no divide 4. Write data a bid 1 to TCR register cnt_up_rd_div1_test Random Nguyễn Vy PASSED	100 10	
6. Wait 300 - (random value) posedege ker_cik	22/9	
	22/9	
	22/9	
7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	22/9	

		Wait for reset and clock stable			1			1	
		2. Write data 8'b100 to TCR register							
		Write random value of TDR register			1				
		Write data 8'b01 to TIE register		Medium					
2.1.6	Count from random, divide by 2	5. Write data 8'b1001 to TCR register	cnt_up_rd_div2_test		Random	Nguyễn Vy	PASSED	22/9	
		6. Wait 600 - (random value) posedege ker_clk							The s_ovf signal is NOT LOW after being asserted  The s_ovf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'h01							
		Wait for reset and clock stable							The s_ovf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted
		Write data 8'b100 to TCR register							
		3. Write random value of TDR register							
		4. Write data 8'b01 to TIE register				_			
2.1.7	Count from random, divide by 4	5. Write data 8'b10001 to TCR register	cnt_up_rd_div4_test		Random	Nguyễn Vy	PASSED	22/9	The s_ovf signal is NOT LOW after being asserted
		Wait 1100 - (random value) posedege ker_clk							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'h01							
		Wait for reset and clock stable		-					
		Wait for reset and clock stable     Write data 8'b100 to TCR register							
		3. Write random value of TDR register							
2.1.8	Count from random, divide by 8	4. Write data 8'b01 to TIE register	cnt_up_rd_div8_test		Random	Nguyễn Vy	DASSED	22/0	The story signal is NOT LOW after being asserted
1.0	Count from random, divide by 6	5. Write data 8'b11001 to TCR register	crit_up_ru_uivo_test		Kandom	ivguyen vy	I ASSED	22/7	The 3_0VI signal is NOT LOW after being asserted
		<ol><li>Wait 2100 - (random value) posedege ker_clk</li></ol>							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'h01	1		1				
		Wait for reset and clock stable							
		Write data 8'b11 to TIE register	1		1				
					1				
		3. Write data 8'b10001 to TCR register							
2.1.9	Count up from 0 with divide by 4, then change the counter at middle	Wait 520 posedege ker_clk     Weite date 0/k10011 to TCP register	cnt_up_change_test		Directed	Nguyễn Vy	PASSED	22/9	The s_udf signal is NOT LOW after being asserted
	, , , , , , , , , , , , , , , , , , , ,	5. Write data 8'b10011 to TCR register				, ,			3
		6. Wait 600 posedege ker_clk	1		1				
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b10						<u></u>	
2.	2 Count down								
		Wait for reset and clock stable							
		2. Write data 8'b10 to TIE register						SED 22/9 The s_ovf signal is NOT LOW at The s_ovf signal is NOT LOW at The s_udf signal is NOT LOW at SED 24/9  SED 24/9 The s_udf signal is NOT LOW at The	
		3. Write data 8'b11 to TCR register					yển Vy PASSED 22/9 The s_ovf signal is NOT LO yển Vy PASSED 22/9 The s_ovf signal is NOT LO yển Vy PASSED 24/9  yển Vy PASSED 24/9  yển Vy PASSED 24/9  The s_udf signal is NOT LO		
		Wait 2 posedege ker_clk							
2.2.1	Count from 0, no divide	5. Write data 8'b11 to TSR register	cnt_dw_div1_test	High	Directed	Nguyễn Vy	PASSED	24/9	
		6. Wait 300 posedege ker_clk							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b10							
		Wait for reset and clock stable							
		2. Write data 8'b10 to TIE register							
		3. Write data 8'b1011 to TCR register							
	Occupation of Alberta has O	Wait 2 posedege ker_clk	and the discount of		Discrete	N	DACCED	0.470	
2.2.2	Count from 0, divide by 2	5. Write data 8'b11 to TSR register	cnt_dw_div2_test		Directed	ivguyen vy	PASSED	24/9	
		6. Wait 600 posedege ker_clk	1		1				
		7. Read value of TSR register	1		1				
		Pass condition: Check interrupt is asserted and read value is 8'b10	1		1				
		Wait for reset and clock stable	<del>-  </del>	-	-	+		1	
			1		1				
		2. Write data 8'b10 to TIE register	1		1				
		3. Write data 8'b10011 to TCR register	1		1				
2.2.3	Count from 0, divide by 4	Wait 2 posedege ker_clk	cnt_dw_div4_test		Directed	Nguyễn Vy	DACCED	24/9	The soudf signal is NOT LOW after being asserted
2.3	Count nome, adde by 4	5. Write data 8'b11 to TSR register	cnt_uw_uiv4_test		Directed	ivguyeri vy	LWOOLD	24/7	The s_dar signal is NOT LOW after being asserted
		6. Wait 1100 posedege ker_clk							
		7. Read value of TSR register	1		1				The s_udf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted  The s_udf signal is NOT LOW after being asserted
		Pass condition: Check interrupt is asserted and read value is 8'h10							
			+	-	-	+		1	
		Wait for reset and clock stable     Write date 9/h10 to T/F register	1		1				
		2. Write data 8'b10 to TIE register	1		1				
		3. Write data 8'b11011 to TCR register							
2.2.4	Count from 0, divide by 8	Wait 2 posedege ker_clk	cnt_dw_div8_test		Directed	Nauvão Vv	DACCED	24/9	The studf signal is NOT LOW after being asserted
2.4	oount normo, divide by o	5. Write data 8'b11 to TSR register	cit_uw_uivo_test		Directed	rvguyeri vy	LUDSED	24/7	The 3_dui signal is NOT LOW after being asserted
		6. Wait 2100 posedege ker_clk	1		1				
		7. Read value of TDR register	1		1				
		Pass condition: Check interrupt is asserted and read value is 8'h10							
		Wait for reset and clock stable	<del>-  </del>	-	-			<b>†</b>	
			1		1				
		2. Write data 8'b100 to TCR register	1		1				
		3. Write random value of TDR register	1		1				
2.2.5	Count from random, no divide	4. Write data 8'b10 to TIE register	cnt_dw_rd_div1_test		Random	Nguyễn Vy	PASSED	26/9	
2.3	Count normaliuom, no uivide	5. Write data 8'b11 to TCR register	cit_uw_ru_uiv1_test		NandOIII	rvguyeri vy	LUDSED	20/7	
		6. Wait [(random value) + 30] posedege ker_clk	1		1				
		7. Read value of TSR register							
								1	Ti control of the con
		Pass condition: Check interrupt is asserted and read value is 8'b10							

				<del></del>					
		Wait for reset and clock stable		Medium					
		2. Write data 8'b100 to TCR register							
		Write random value of TDR register							
		4. Write data 8'b10 to TIE register							
2.2.6	Count from random, divide by 2	5. Write data 8'b1011 to TCR register	cnt_dw_rd_div2_test		Random	Nguyễn Vy	PASSED	26/9	
		6. Wait [(random value)*2 + 30] posedege ker_clk							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b10							
		Wait for reset and clock stable							
		2. Write data 8'b100 to TCR register							
		Write random value of TDR register							
		4. Write data 8'b10 to TIE register							
2.2.7	Count from random, divide by 4		cnt_dw_rd_div4_test		Random	Nguyễn Vy	PASSED	26/9	The s_udf signal is NOT LOW after being asserted
		5. Write data 8'b10011 to TCR register				0 , ,			_
		<ol><li>Wait [(random value)*4 + 30] posedege ker_clk</li></ol>							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b10							
		Wait for reset and clock stable							
		2. Write data 8'b100 to TCR register							
		Write random value of TDR register							
2.2.8	Count from random, divide by 8	4. Write data 8'b10 to TIE register	cnt_dw_rd_div8_test		Random	Nguyễn Vy	PASSED	26/9	The s_udf signal is NOT LOW after being asserted
L.L.O	odan nominandom, amao by o	5. Write data 8'b11011 to TCR register	unt_un_ru_uno_test		nanaom	rigarier 17	TAGGED	20,,	The S_dat Signal is No.1 2011 dites being asserted
		<ol><li>Wait [(random value)*8 + 30] posedege ker_clk</li></ol>							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b10							
<b>—</b>		Wait for reset and clock stable			1		1	-	
					1		1		
		2. Write data 8'b11 to TIE register			1		1		
		3. Write data 8'b10011 to TCR register			1		1		Clear data from TSR register, but underflow bit from TSR
		Wait 520 posedege ker_clk							
2.2.9	Count down from 0 with divide by 4, then change the counter at middle	5. Write data 8'b11 to TSR register	cnt_dw_change_test		Directed	Nguyễn Vy	FAILED	26/9	register is still value because the s_udf signal is NOT LOW
	, , , , , , , , , , , , , , , , , , ,	6. Write data 8'b10001 to TCR register				3.3.			after being asserted. The s_ovf signal is NOT LOW after
		7. Wait 600 posedege ker_clk							being asserted
		8. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b01							
2.3	Cross count up and count down								
		Wait for reset and clock stable							
		Write data 8'b11 to TIE register							
		3. Write data 8'b01 to TCR register							
		4. Wait 130 posedege ker_clk							
2.3.1	Count up from 0, then changes to count down		cnt_up_dw_test		Directed	Nguyễn Vy	PASSED	28/9	
		5. Write data 8'b11 to TCR register				0 , ,			
		Wait 300 posedege ker_clk							
		7. Read value of TSR register							
		Pass condition: Check interrupt is asserted and read value is 8'b01							
		Wait for reset and clock stable		_					
		Write data 8'b100 to TCR register							
		Write random value of TDR register							
		Write data 8'b11 to TIE register							
2 2 2	Count in from random than above to see the see		and up about the		Donel	Nama Z - M	DACCEC	20/0	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_Clk 7. Write data 8'b11 to TCR register	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8"b11 to TIE register 5. Write data 8"b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8"b11 to TCR register 8. Wait 300 posedege ker_clk	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIC register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_dw_rd_test	Medium		Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable	cnt_up_dw_rd_test	Medium		Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIC register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_dw_rd_test	Medium		Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register	cnt_up_dw_rd_test	Medium		Nguyễn Vy	PASSED	28/9	
		4. Write data 8°b11 to TIE register 5. Write data 8°b11 to TIC register 6. Wait 130 posedege ker_clk 7. Write data 8°b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8°b01 1. Wait for reset and clock stable 2. Write data 8°b11 to TIE register 3. Write data 8°b11 to TIE register		Medium					
2.3.2	Count up from random, then changes to count down  Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk	cnt_up_dw_rd_test	Medium		Nguyễn Vy Nguyễn Vy	PASSED PASSED	28/9	
		4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b101 to TCR register 5. Write data 8'b101 to TCR register		Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIC register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIC register 3. Write data 8'b11 to TIC register 4. Wait 130 posedege ker_clk 5. Write data 8'b01 to TCR register 6. Wait 300 posedege ker_clk		Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_cik 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_cik 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_cik 5. Write data 8'b01 to TCR register 6. Wait 300 posedege ker_cik 7. Read value of TSR register		Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIC register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIC register 3. Write data 8'b11 to TIC register 4. Wait 130 posedege ker_clk 5. Write data 8'b01 to TCR register 6. Wait 300 posedege ker_clk		Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01		Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIE register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable							
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b01 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register		— Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b101 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write raset and clock stable 2. Write data 8'b10 to TCR register 3. Write random value of TDR register 3. Write random value of TDR register		— Medium					
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Read value of TSR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 1. Write data 8'b10 to TCR register 1. Write data 8'b110 to TCR register 1. Write data 8'b110 to TCR register 1. Write data 8'b110 to TCR register		— Medium					
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 5. Write data 8'b11 to TCR register 5. Write data 8'b11 to TCR register	cnt_dw_up_test	— Medium	Directed	Nguyễn Vy	PASSED	28/9	
		4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Read value of TSR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 4. Write data 8'b10 to TCR register 1. Write data 8'b10 to TCR register 1. Write data 8'b110 to TCR register 1. Write data 8'b110 to TCR register 1. Write data 8'b110 to TCR register		— Medium					
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b101 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Write data 8'b10 to TCR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TCR register 5. Write data 8'b10 to TCR register 6. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 5. Write data 8'b10 to TCR register 6. Wait 130 posedege ker_clk	cnt_dw_up_test	— Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIE register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TIE register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 6. Write data 8'b11 to TCR register 7. Write data 8'b11 to TCR register 8. Write data 8'b11 to TCR register 9. Write data 8'b11 to TCR register 1. Write data 8'b11 to TCR register	cnt_dw_up_test	— Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for rest and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 4. Write random value of TDR register 5. Write data 8'b10 to TCR register 4. Write data 8'b11 to TIER register 5. Write data 8'b11 to TIER register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 130 posedege ker_clk 9. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 300 posedege ker_clk 9. Write data 8'b10 to TCR register 8. Wait 300 posedege ker_clk 9. Write data 8'b10 to TCR register	cnt_dw_up_test	Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 7. Write data 8'b101 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Write data 8'b10 to TCR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TCR register 5. Write data 8'b10 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TICR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b10 to TCR register 8. Write data 8'b10 to TCR register 9. Write data 8'b10 to TCR register	cnt_dw_up_test	— Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up  Count down from random, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for rest and clock stable 2. Write data 8'b11 to TCR register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b10 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 4. Write random value of TDR register 5. Write data 8'b10 to TCR register 4. Write data 8'b11 to TIER register 5. Write data 8'b11 to TIER register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 130 posedege ker_clk 9. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 130 posedege ker_clk 1. Write data 8'b10 to TCR register 8. Wait 300 posedege ker_clk 9. Write data 8'b10 to TCR register 8. Wait 300 posedege ker_clk 9. Write data 8'b10 to TCR register	cnt_dw_up_test	Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up	4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01 1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 7. Write data 8'b101 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register 9. Write data 8'b10 to TCR register 1. Wait for reset and clock stable 2. Write data 8'b10 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TCR register 5. Write data 8'b10 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TICR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b10 to TCR register 8. Write data 8'b10 to TCR register 9. Write data 8'b10 to TCR register	cnt_dw_up_test	— Medium	Directed	Nguyễn Vy	PASSED	28/9	

2.4.1	Count up with no divide, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TE register 3. Write data 8'h01 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'h11001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_1_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.2	Count up with divide by 2, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'h1101 to TIE register 3. Write data 8'h1001 to TCR register 4. Wait 300 posedege ker_clk 5. Write data 8'h11001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_2_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.3	Count up with divide by 4, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8 'h1 10 TIE register 3. Write data 8 'h1 1001 to TCR register 4. Wait 600 posedege ker_clk 5. Write data 8 'h1 1001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_4_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.4	Count down with divide by no divide, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8*b11 to TIE register 3. Write data 8*b11 to TCR register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8*b11 to TSR register 7. Wait 130 posedege ker_clk 8. Write data 8*b11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8*b10	cnt_dw_div_1_8_test	Medium	Directed	Nguyễn Vy	PASSED	30/9	
2.4.5	Count down with divide by 2, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TE register 3. Write data 8'h1011 to TCR register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b11 to TSR register 7. Wait 300 posedege ker_clk 8. Write data 8'h11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register Psss condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div_2_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.6	Count down with divide by 4, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TE register 3. Write data 8'b11 to TE register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b11 to TSR register 7. Wait 600 posedege ker_clk 8. Write data 8'h11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register 9. Wait 100 rosedege ker_clk 10. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div_4_8_test		Directed	Nguyễn Vy	PASSED	30/9	
	Interrupt test								
3.7	Check underflow forward input	1. Walt for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b11 to TCR register 4. Walt 255 posedge clk, in Pass condition: Check interrupt is asserted 1. Walt for reset and clock stable	underflow_en_test		Directed	Nguyễn Vy	PASSED	03/10	
3.2	Check underflow not forward input	Write data 32'b11 to TCR register     Wait 255 posedge clk_in     Pass condition: Check interrupt is not asserted	underflow_dis_test	High	Directed	Nguyễn Vy	PASSED	03/10	
3.3	Check overflow forward input	Write data 8'b01 to TIE register     Write data 8'b01 to TCR register     Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	overflow_en_test		Directed	Nguyễn Vy	PASSED	03/10	

3.4		Wait for reset and clock stable     White data 8'b01 to TCR register     Wait 255 posedge clk_in     Pass condition: Check interrupt is not asserted	overflow_dis_test		Directed	Nguyễn Vy	PASSED	03/10	l
3.5	Check underflow and overflow forward input	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 255 posedge clk_in 5. Write 8'b11 to TSR register 6. Write data 8'b11 to TCR register 7. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	ud_over_en_test	Medium	Directed	Nguyễn Vy	PASSED	03/10	l
3.6	Check underflow and overflow not forward input	1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 3. Wait 255 posedge clk_in 4. Write 8'b11 to TSR register 4. Write data 8'b11 to TCR register 5. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	ud_over_dis_test		Directed	Nguyễn Vy	PASSED	03/10	
4	Check APB protocol				Assertion				