Total Items	39
Pass Items	38
Fail Items	1
NY Items	0

Section	Main Title	Description	Testname	Priority	Method	Owner	Status	Milestone	Remark
1	Register test								
1.1	Read default value	1. Wait for reset and clock stable 2. Read value of 4 register Pass condition: Check value matching with default value mention in RTL spec	reg_def_test		Directed	Nguyễn Vy	PASSED	18/9	
1.2	Read and Write value check	1. Wait for reset and clock stable 2. Write random value of 4 register 3. Read value of 4 register Pass condition: Check value matching	reg_rw_test		Directed	Nguyễn Vy	PASSED	18/9	
1.3	Reset on the fly check	1. Wait for reset and clock stable 2. Write random value of 4 register 3. Reset system 4. Read value of 4 register Pass condition: Check value matching with default value mention in RTL spec	reg_rs_test		Directed	Nguyễn Vy	PASSED	18/9	
1.4	Check reserved register	1. Wait for reset and clock stable 2. Write random value of reserved register 3. Read value of reserved register Pass condition: Check value equal is 0	reg_reserved_test	High	Directed	Nguyễn Vy	PASSED	18/9	
1.5	Check interrupt in TSR register	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h01 to TCR register 4. Wait interrupt is asserted 5. Write data 8'h00 to TSR register 6. Read value of TSR register 7. Write data 8'b01 to TSR register 8. Read value of TSR register 9. Write data 8'b11 to TCR register 10. Wait interrupt is asserted 11. Write data 8'b00 to TSR register 12. Read value of TSR register 13. Write data 8'b10 to TSR register 14. Read value of TSR register Pass condition: Check underflow bit and overflow bit is matching	reg_tsr_test		Directed	Nguyễn Vy	PASSED	18/9	
2	Counter combine with divisor test								
2.1	Count up					Nguyễn Vy			
2.1.1	Count from 0, no divide	1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 300 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_div1_test	High	Directed	Nguyễn Vy	PASSED	20/9	
2.1.2	Count from 0, divide by 2	1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b1001 to TCR register 4. Wait 600 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_div2_test		Directed	Nguyễn Vy	PASSED	20/9	
2.1.3	Count from 0, divide by 4	1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b10001 to TCR register 4. Wait 1040 posedege ker_clk 5. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_div4_test		Directed	Nguyễn Vy	PASSED	20/9	The s_ovf signal is NOT LOW after being asserted
2.1.4	Count from 0, divide by 8	1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b11001 to TCR register 4. Wait 2100 posedege ker_clk 5. Read value of TDR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_div8_test		Directed	Nguyễn Vy	PASSED	20/9	The s_ovf signal is NOT LOW after being asserted
2.1.5	Count from random, no divide	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b01 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 300 - (random value) posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_rd_div1_test		Random	Nguyễn Vy	PASSED	22/9	

2.1.6	Count from random, divide by 2	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b01 to TIE register 5. Write data 8'b1001 to TCR register 6. Wait 600 - (random value) posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_rd_div2_test	Medium	Random	Nguyễn Vy	PASSED	22/9	
2.1.7	Count from random, divide by 4	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b01 to TIE register 5. Write data 8'b10001 to TCR register 6. Wait 1100 - (random value) posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_rd_div4_test		Random	Nguyễn Vy	PASSED	22/9	The s_ovf signal is NOT LOW after being asserted
2.1.8	Count from random, divide by 8	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b01 to TIE register 5. Write data 8'b11001 to TCR register 6. Wait 2100 - (random value) posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h01	cnt_up_rd_div8_test		Random	Nguyễn Vy	PASSED	22/9	The s_ovf signal is NOT LOW after being asserted
2.1.9	Count up from 0 with divide by 4, then change the counter at middle	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b10001 to TCR register 4. Wait 520 posedege ker_clk 5. Write data 8'b10011 to TCR register 6. Wait 600 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_up_change_test		Directed	Nguyễn Vy	PASSED	22/9	The s_udf signal is NOT LOW after being asserted
2.2	Count down								
2.2.1	Count from 0, no divide	1. Wait for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 2 posedege ker_clk 5. Write data 8'b11 to TSR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div1_test	High	Directed	Nguyễn Vy	PASSED	24/9	
2.2.2	Count from 0, divide by 2	1. Wait for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b1011 to TCR register 4. Wait 2 posedege ker_clk 5. Write data 8'b11 to TSR register 6. Wait 600 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div2_test		Directed	Nguyễn Vy	PASSED	24/9	
2.2.3	Count from 0, divide by 4	1. Wait for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b10011 to TCR register 4. Wait 2 posedege ker_clk 5. Write data 8'b11 to TSR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'h10	cnt_dw_div4_test		Directed	Nguyễn Vy	PASSED	24/9	The s_udf signal is NOT LOW after being asserted
2.2.4	Count from 0, divide by 8	1. Wait for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b11011 to TCR register 4. Wait 2 posedege ker_clk 5. Write data 8'b11 to TSR register 6. Wait 2100 posedege ker_clk 7. Read value of TDR register Pass condition: Check interrupt is asserted and read value is 8'h10	cnt_dw_div8_test		Directed	Nguyễn Vy	PASSED	24/9	The s_udf signal is NOT LOW after being asserted
2.2.5	Count from random, no divide	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TIE register 5. Write data 8'b11 to TCR register 6. Wait [(random value) + 30] posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_rd_div1_test		Random	Nguyễn Vy	PASSED	26/9	

2.2.6	Count from random, divide by 2	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TIE register 5. Write data 8'b1011 to TCR register 6. Wait [(random value)*2 + 30] posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_rd_div2_test	Medium	Random	Nguyễn Vy	PASSED	26/9	
2.2.7	Count from random, divide by 4	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TIE register 5. Write data 8'b10011 to TCR register 6. Wait [(random value)*4 + 30] posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_rd_div4_test		Random	Nguyễn Vy	PASSED	26/9	The s_udf signal is NOT LOW after being asserted
2.2.8	Count from random, divide by 8	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b10 to TIE register 5. Write data 8'b11011 to TCR register 6. Wait [(random value)*8 + 30] posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_rd_div8_test		Random	Nguyễn Vy	PASSED	26/9	The s_udf signal is NOT LOW after being asserted
2.2.9	Count down from 0 with divide by 4, then change the counter at middle	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b10011 to TCR register 4. Wait 520 posedege ker_clk 5. Write data 8'b11 to TSR register 6. Write data 8'b10001 to TCR register 7. Wait 600 posedege ker_clk 8. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_dw_change_test		Directed	Nguyễn Vy	FAILED	26/9	Clear data from TSR register, but underflow bit from TSR register is still value because the s_udf signal is NOT LOW after being asserted. The s_ovf signal is NOT LOW after being asserted
2.3	Cross count up and count down								
2.3.1	Count up from 0, then changes to count down	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b11 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_dw_test	Medium	Directed	Nguyễn Vy	PASSED	28/9	
2.3.2	Count up from random, then changes to count down	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b11 to TIE register 5. Write data 8'b01 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b11 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_dw_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.3.3	Count down from 0, then changes to count up	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'b01 to TCR register 6. Wait 300 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_dw_up_test		Directed	Nguyễn Vy	PASSED	28/9	
2.3.4	Count down from random, then changes to count up	1. Wait for reset and clock stable 2. Write data 8'b100 to TCR register 3. Write random value of TDR register 4. Write data 8'b11 to TIE register 5. Write data 8'b11 to TCR register 6. Wait 130 posedege ker_clk 7. Write data 8'b01 to TCR register 8. Wait 300 posedege ker_clk 9. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b11	cnt_dw_up_rd_test		Random	Nguyễn Vy	PASSED	28/9	
2.4	Changes divide mode at middle								

2.4.1	Count up with no divide, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h01 to TCR register 4. Wait 130 posedege ker_clk 5. Write data 8'h11001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_1_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.2	Count up with divide by 2, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h1001 to TCR register 4. Wait 300 posedege ker_clk 5. Write data 8'h11001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_2_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.3	Count up with divide by 4, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h10001 to TCR register 4. Wait 600 posedege ker_clk 5. Write data 8'h11001 to TCR register 6. Wait 1100 posedege ker_clk 7. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b01	cnt_up_div_4_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.4	Count down with divide by no divide, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h11 to TCR register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b11 to TSR register 7. Wait 130 posedege ker_clk 8. Write data 8'h11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div_1_8_test	Medium	Directed	Nguyễn Vy	PASSED	30/9	
2.4.5	Count down with divide by 2, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h1011 to TCR register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b11 to TSR register 7. Wait 300 posedege ker_clk 8. Write data 8'h11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div_2_8_test		Directed	Nguyễn Vy	PASSED	30/9	
2.4.6	Count down with divide by 4, then changes to divide by 8	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'h10011 to TCR register 4. Wait 10 posedege ker_clk 5. Read value of TSR register 6. Write data 8'b11 to TSR register 7. Wait 600 posedege ker_clk 8. Write data 8'h11011 to TCR register 9. Wait 1100 posedege ker_clk 10. Read value of TSR register Pass condition: Check interrupt is asserted and read value is 8'b10	cnt_dw_div_4_8_test		Directed	Nguyễn Vy	PASSED	30/9	
3	Interrupt test								
3.1	Check underflow forward input	1. Wait for reset and clock stable 2. Write data 8'b10 to TIE register 3. Write data 8'b11 to TCR register 4. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	underflow_en_test	High	Directed	Nguyễn Vy	PASSED	03/10	
3.2	Check underflow not forward input	1. Wait for reset and clock stable 2. Write data 32'b11 to TCR register 3. Wait 255 posedge clk_in Pass condition: Check interrupt is not asserted	underflow_dis_test		Directed	Nguyễn Vy	PASSED	03/10	
3.3	Check overflow forward input	1. Wait for reset and clock stable 2. Write data 8'b01 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	overflow_en_test		Directed	Nguyễn Vy	PASSED	03/10	

3.4	Check overflow not forward input	1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 3. Wait 255 posedge clk_in Pass condition: Check interrupt is not asserted	overflow_dis_test		Directed	Nguyễn Vy	PASSED	03/10	
3.5	Check underflow and overflow forward input	1. Wait for reset and clock stable 2. Write data 8'b11 to TIE register 3. Write data 8'b01 to TCR register 4. Wait 255 posedge clk_in 5. Write 8'b11 to TSR register 6. Write data 8'b11 to TCR register 7. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	ud_over_en_test	Medium	Directed	Nguyễn Vy	PASSED	03/10	
3.6	Check underflow and overflow not forward input	1. Wait for reset and clock stable 2. Write data 8'b01 to TCR register 3. Wait 255 posedge clk_in 4. Write 8'b11 to TSR register 4. Write data 8'b11 to TCR register 5. Wait 255 posedge clk_in Pass condition: Check interrupt is asserted	ud_over_dis_test		Directed	Nguyễn Vy	PASSED	03/10	
4	Check APB protocol				Assertion				