

# JOHN BELL ENGINEERING **CRT CONTROLLER**

### BASIC CONFIGURATION

AS SHOWN IN THE SCHEMATIC THE HEART OF THE CONTROLLER IS AN 8085A 8-BIT MICROPROCESSOR OPERATING AT 3MHZ AND SUPPORTED BY TWO 8185 1K X 8 STATIC RAM MEMORIES AND A 2716 CONTROL SOFTWARE PROM. AN 8251A PROGRAMMABLE COMMUNICATION INTERFACE PROVIDES SYNCHRONOUS OR ASYNCHRONOUS SERIAL COMMUNICATIONS. BAUD RATES ARE SELECTED BY MEANS OF SWITCHES CONTAINED ON THE BOARD AND THE BAUD RATE CLOCK IS GENERATED BY THE 8253 PROGRAMMABLE INTERVAL TIMER UNDER SOFT-WARE CONTROL. AN 8255A PROVIDES THREE 8-BIT PARALLEL I/O PURTS, TWO OF WHICH ARE UTILIZED FOR KEYBOARD SCANNING. THE THIRD PORT IS USED TO SENSE OPTION SWITCH SETTINGS AND TO SENSE THE VERTICAL RETRACE SIGNAL FROM THE 8275 FOR CRT SYNCHRONIZATION.

THE CRT INTERFACE IS CONTROLLED BY AN 8275 PROGRAMMABLE CRT CON-TROLLER. THE CRT DOT AND CHARACTER TIMING IS GENERATED BY AN 8224 CLOCK GENERATOR. A SECOND CHANNEL OF THE 8253 TIMER PROVIDES THE APPROPRIATE HORIZONTAL RETRACE TIMING FOR THE CRT MONITOR. A 2716 EPROM IS UTILIZED TO PROVIDE A USER-PROGRAMMABLE CHARACTER GENERA-TOR, AND A SHIFT REGISTER TRANSFORMS THE DATA FROM THE CHARACTER EPROM INTO A SERIAL BIT STREAM TO ILLUMINATE DOTS ON THE CRT SCREEN. THE 2716 CHARACTER GENERATOR MAKES IT POSSIBLE TO DISPLAY SPECIAL SYMBOLS FOR WORD PROCESSING OR INDUSTRIAL CONTROL APPLICATIONS OR TO DISPLAY CHARACTERS AND WORDS IN A FOREIGN LANGUAGE.

### SYSTEM ARCHITECTURE

THE CONTROLLER HARDWARE IS DIVIDED INTO THREE SECTIONS: PROCESSOR AND SUPPORT, SERIAL AND PARALLEL I/O, AND CRT CONTROL. THE PRO-CESSOR AND SUPPORT SECTION CONSISTS OF AN 8085A MICROPORCESSOR, TWO 8185 1K X 8 STATIC RAM DEVICES, AND A 2716 EPROM (CONTAINING 2K BYTES OF CONTROL FIRMWARE). THE 8085A USES A 6 MHZ CRYSTAL IN ORDER TO OPERATE AT A 3MHZ CLOCK RATE. THE 8185 MEMORIES ATTACH DIRECTLY TO THE 8085A MULTIPLEXED BUS. AN 8282 IS USED TO LATCH EIGHT ADDRESS LINES (A0-A7) FROM THE MULTIPLEXED BUS FOR 2716 PROGRAM MEMORY ACCESS (AS SHOWN IN FIGURE 3).

THE 8253 CONTAINS THREE INDEPENDENT TIMERS AND GENERATES TWO TIMING SIGNALS FOR THE CONTROLLER. THE FIRST TIMER IS OPERATED IN A PRO-GRAMMABLE ONE SHOT MODE, GENERATING A 32 MICROSECOND HORIZONTAL RE-TRACE PULSE FOR THE BALL BROTHERS TV-12 CRT MONITOR USED IN THIS DESIGN. A SIMPLE SOFTWARE CHANGE ALLOWS THE USER TO MODIFY THIS DE-LAY TIME FOR DIFFERENT CRT MONITORS.

A SECOND TIMER IS USED TO GENERATE 8251A BAUD RATE. THREE SWITCHES ARE MONITORED BY THE 8085A TO DETERMINE THE DESIRED BAUD RATE. WHEN THE CPU DETECTS A CHANGE IN THE SWITCH POSITIONS, THE 8253 IS LOADED WITH THE APPROPRIATE COUNT FOR THE NEW BAUD RATE. THE THIRD TIMER IS AVAILABLE FOR CUSTOMER USE.

ALL I/O OPERATIONS OF THE CONTROLLER ARE MEMORY MAPPED.

\*\* PLEASE NOTE THE OUTPUT IS NOT NTSC STANDARD.

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PARTS LIST
                                                                                                               IC, 1489 (75189)
IC, 1488 (75188)
IC, 74LS166
IC, 74LS175
IC, 74LS00
IC, 8251
IC, 2716
IC, 8275
IC. 8275
A1
A2
A3
A4
A5
A6
                                                                                                             IC, 2716
IC, 8275
IC, 8275
IC, 8275
IC, 8285
IC, 74LS139
IC, 3085A
IC, 74LS163
IC, 3135
IC, 8282
IC, 8224
IC, 74LS74
IC, 8255A
CRYSTAL, 6.144 MHZ
CRYSTAL, 11.34 MHZ
SWITCH PACK, 8 SWITCHES, 16 PIN CIP
DIODE, IN4001
RESISTOR PACK, 10K, 10 PIN SIP
RESISTOR, 1K, W
CAPACITOR, 530PF
CAPACITOR, 530PF
CAPACITOR, 5UF, 15V
CAPACITOR, 5UF, 15V
CAPACITOR, 01UF
HEADER, 40 PIN (2X201), I" CENTERS
HEADER, 4 PIN, 1" CENTERS
IC SOCKET, 14 PIN
IC SOCKET, 18 PIN
IC SOCKET, 18 PIN
IC SOCKET, 20 PIN
IC SOCKET, 24 PIN
IC SOCKET, 28 PIN
IC SOCKET, 40 PIN
 A7, A12
 Α8
 Α9
A10
 A11
 A13
 A14, A18
 A15
A16
A17
 A19
XTAL1
XTAL2
Sl
 CR1
RP1, RP2
R1, R2, R3
C5
C23
C1-C4
C6-C22, C24
J2
RXD, CTS
RTS- CTS
A1-A2, A5, A17
A3-A4, A10, A13, A16
A14, A18
A15
A7, A9, A12
A6
A8, A11, A19
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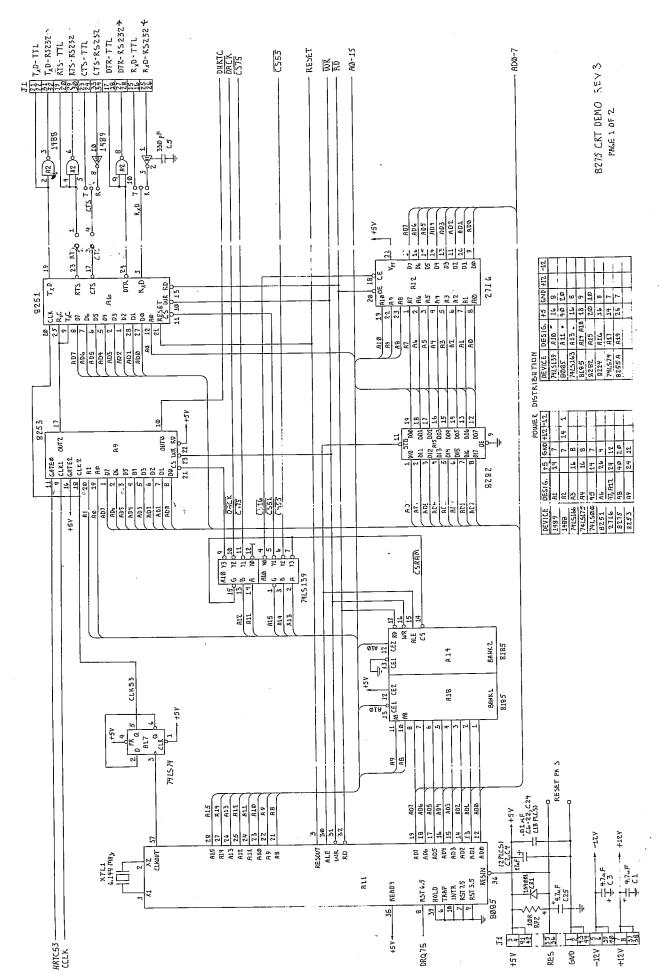
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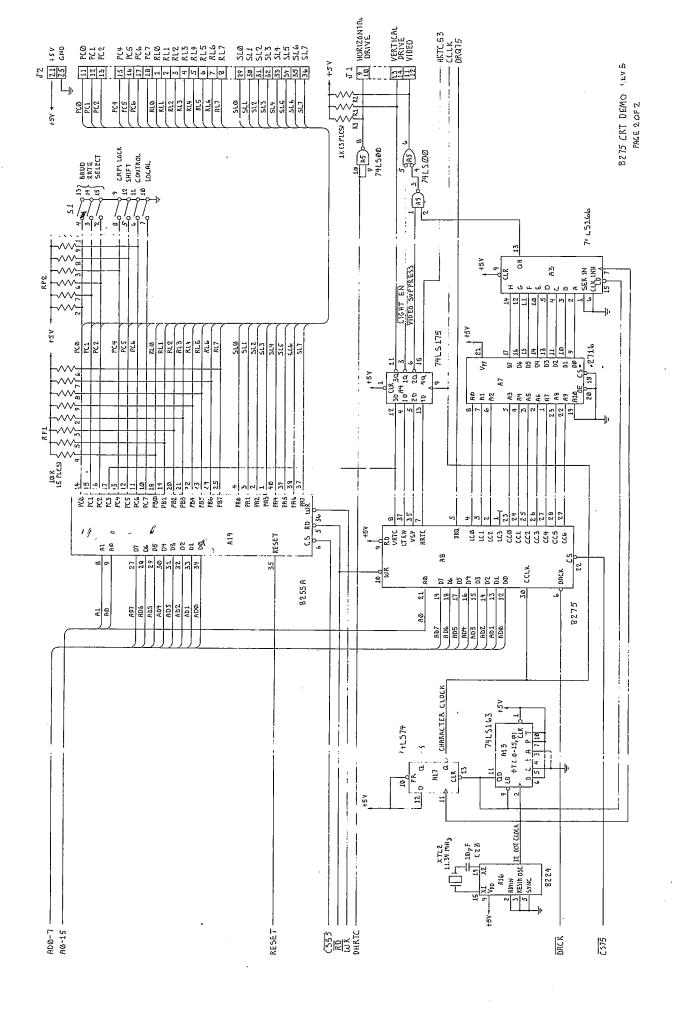
J1 PIN LIST

PINS   DESCRIPTION			•		
5 6   1/2	PIN	S		 DESCRIPTION	
43 44 GND	3 7 113 15 17 121 225 27 231 335 57 341	4681121146812022246233346833340	14,	+5 12 12 HORIZONTAL PRIVE VIDEO OUTPUT VERTICAL DRIVE RXD (TTL) DTR (TTL) RTS (TTL) TXD (TTL) CTS (TTL) RXS (RS-232C) DTR (RS-232C) TXD (RS-232C) CTS (RS-232C) RTS (RS-232C)	TO MONITOR

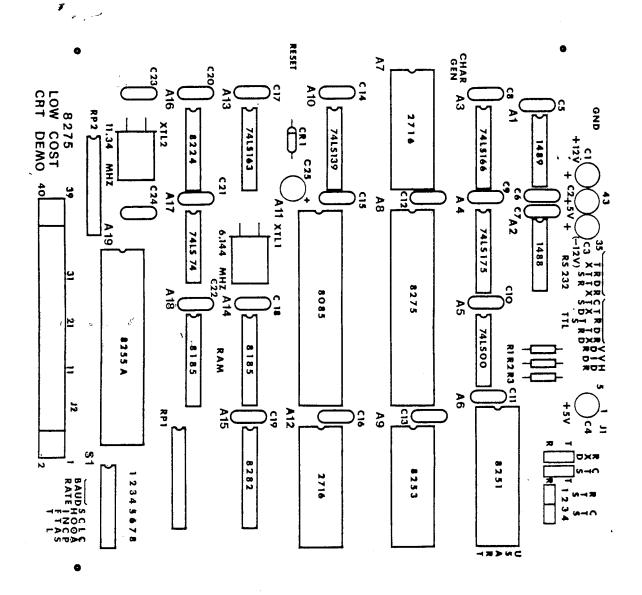
J2 PIN LIST

PIN	DESCR	IPTION	PIN	DESCRIPTIN
1	RĻÓ		2	RL1
3	RL2		4	RL3
5	RL4		6	RL5
3 5 7	RL6		8	KL7
9			10	
11	PCO		12	PC1
13	PC2	BAUD RATE	14	
15	PC4		16	PC5
17	PC6		18	PC7
19			20	
21	Vcc		22	
23			24	
25	GROUN	D	26	
27			28	
29	SLO		30	SLl
31	SL2		32	\$L3
33	SL4		34	SL5
35	SL6		36	SL7
37			38	
39			40	2











### SERIAL AND PARALLEL I/O

THE CRT CONTROLLER BOARD COMMUNICATES TO COMPUTER SYSTEMS AND OTHER CRT UNITS THROUGH A SERIAL INTERFACE. BOTH RS-232C AND TTL COMPATIBLE INTERFACES ARE AVAILABLE AT THE J1 CONNECTOR. THE UNIT'S STANDARD SOFTWARE SUPPORTS DATA TRANSMISSION RATES OF 9600, 4800, 2400, 1200, 600, 300, 150, AND 110 BAUD. THESE RATES ARE SWITCH SELECTABLE ON THE BOARD. SINCE THE BAUD RATE CLOCK IS GENERATED BY AN 8253, THESE RATES MAY BE EASILY MODIFIED IN SOFTWARE.

KEYBOARD SCANNING IS SUPPORTED THROUGH THE A AND B PORTS OF THE 8255A PROGRAMMABLE PERIPHERAL INTERFACE. THE EIGHT SCAN LINES (PORT B) AND EIGHT RETURN LINES (PORT A) SUPPORT A 64 CONTACT CLOSURE KEY MATRIX. THREE SWITCHES ARE ATTACHED TO PORT C TO PERMIT BAUD RATE SELECTION. FOUR ADDITIONAL GENERAL PURPOSE INPUTS ON PORT C PERMIT THE SOFTWARE TO SENSE DEPRESSION OF THE CAPS LOCK KEY, THE CONTROL KEY, AND THE SHIFT KEY AS WELL AS THE POSITION OF THE LINE/LOCAL SWITCH. THE LAST INPUT ON PORT C IS USED TO SENSE THE STATUS OF THE VRTC (VERTICAL RETRACE) OUTPUT OF THE 8275 SO THAT THE CONTROLLER CAN SYNC HRONIZE WITH THE CRT DISPLAY ON POWER UP OR AFTER A HARD-WARE RESET.

ALL KEYBOARD I/O IS CONNECTED TO THE CONTROLLER BY MEANS OF A 40 PIN HEADER ON THE EDGE OF THE BOARD. ALL SEVEN OPTION SWITCH INPUTS ARE ALSO BROUGHT TO THE CONNECTOR SO THAT OPTION SWITCHES MAY BE INSTALLED ON THE KEYBOARD IF DESIRED.

### CRT CONTROL

THE CRT DISPLAY IS CONTROLLED BY AN 8275 PROGRAMMABLE CRT CONTROLLER. THIS DEVICE PERMITS SOFTWARE SPECIFICATION OF MOST CRT SCREEN FOR-MAT CHARACTERISTICS SUCH AS THE CURSOR POSITION, THE NUMBER OF CHARACTERS PER ROW, AND THE NUMBER OF ROWS PER FRAME (SCREEN). THE 8275 HANDLES ALL DISPLAY TIMING INCLUDING RETRACE TIME DELAYS.

IN THE CURRENT DESIGN, 2000 CHARACTERS ARE DISPLAYED ON THE CRT SCREEN (25 ROWS OF 80 CHARACTERS). EACH CHARACTER IS FORMED AS A 5 BY 7 DOT MATRIX WITHIN A LARGER 7 BY 10 MATRIX (FIGURE 4). OTHER SCREEN FORMATS (E.G., THE POPULAR 16 ROWS OF 64 CHARACTERS) CAN BE EASILY IMPLEMENTED WITH MINIMAL SOFTWARE CHANGES.

### SCREEN REFRESH

THE 8275 CONTAINS TWO 80 CHARACTER ROW BUFFERS. WHILE ONE BUFFER IS USED TO DISPLAY THE CURRENT CHARACTER LINE ON THE SCREEN, THE 8275 FILLS THE OTHER ROW BUFFER FROM MEMORY. THIS DATA TRASFER BEGINS WHEN THE 8275 ISSUES A DATA REQUEST (BY MEANS OF THE DRQ PIN), CAUSING AN INTERRUPT TO THE CPU. IN RESPONSE TO THIS INTERRUPT, THE CPU ACTIVATES THE RAM'S CS AND RD INPUTS WHILE SIMULTANEOUSLY ACTIVATING THE 8275'S DACK AND WR INPUTS. WITH THIS TECHNIQUE, A SINGLE BUS CYCLE IS USED TO TRANSFER EACH BYTE FROM THE RAM INTO THE CRT ROW BUFFER. AFTER THE ROW BUFFER IS FILLED, THE CPU EXITS THE INTERRUPT SERVICE ROUTINE.

### ATTRIBUTES

THE 8275 CAN DO MUCH MORE THAN SIMPLY PAINT CHARATERS ON A CRT SCREEN. IN THIS IMPLEMENTATION, THE END OF ROW-STOP DMA COMMAND CODE ALLOWS THE CONTROL SOFTWARE TO EASILY BLANK INDIVIDUAL DISPLAY LINES OR TO PERFORM AN ERASE TO END OF SCREEN FUNCTION.

THE 8275 SUPPORTS SOFTWARE SELECTION OF CHARACTER ATTRIBUTES. COMMAND CODES TO TURN THESE ATTRIBUTES ON AND OFF MAY BE EMBEDDED IN THE DISPLAY LINE BUFFER. ATTRIBUTES ARE USED TO BLINK, UNDERLINE, OR HIGHLIGHT (INTENSIFY) CHARACTERS ON THE SCREEN. ATTRIBUTES ALSO CONTROL THE REVERSE VIDEO DISPLAY (BLACK LETTERS ON A WHITE BACKGROUND) CAPABILITY. TWO GENERAL PURPOSE ATTRIBUTES ARE ALSO PROVIDED TO CONTROL UNIQUE USER-DESIGNED DISPLAY CAPABILITIES.

### DISPLAY TIMING AND SUPPORT

THE 8275 IS SUPPORTED BY THREE HARDWARE FUNCTIONS (FIGURE 4): A DOT /CHARACTER CLOCK OSCILLATOR, A PROM/ROM CHARACTER GENERATOR, AND A CHARACTER SHIFT REGISTER. THE DOT/CHARACTER CLOCK OSCILLATOR CONSISTS OF AN 8224 OPERATING AT 11.34 MHZ AND PROVIDING AN 87.5 NANOSECOND DOT CLOCK. A 74LS163 DIVIDES THIS CLOCK BY 7 TO GENERATE A 1.63 MHZ (612 NANOSECOND) CHARACTER CLOCK. THE 8275 IS PROGRAMMED TO DISPLAY ONE RASTER LINE EVERY 61.2 MICROSECONDS - A COMPLETE CHARACTER LINE EVERY 612 MICROSECONDS (10 RASTER LINES). THE 8275 IS ALSO PROGRAMMED TO REFRESH THE SCREEN EVERY 16.5 MILLISECONDS (60.5 HZ).

EACH CHARACTER ROW CONSISTS OF TEN RASTER LINES. SEVEN LINES ARE USED TO DISPLAY THE 5 X 7 MATRIX CHARACTERS, TWO LINES ARE BLANKED FOR ROW SPACING, AND ONE LINE DISPLAYS THE CURSOR AND UNDERLINE.

THE 8275 USES THE LCO-LC3 OUTPUTS TO INDICATE THE CURRENT RASTER LINE DURING THE DISPLAY OF EACH CHARACTER. THESE OUTPUTS, COMBINED WITH THE CHARACTER CODE OUTPUTS (CC0-CC6), ARE INPUT TO THE 2716 IN ORDER TO GENERATE THE DOT PATTERN FOR DISPLAY. THIS DOT PATTERN IS LOADED INTO THE SHIFT REGISTER AND IS SERIALLY CLOCKED FOR DISPLAY BY THE 11.34 MHZ DOT CLOCK.

DURING THE VERTICAL RETRACE INTERVAL, THE ROW BUFFER FOR THE FIRST LINE OF THE NEXT FRAME IS LOADED BY THE 8085A. WHEN THE FRAME STARTS, THE 8275 OUTPUTS THE FIRST CHARACTER ON ITS CCO-CC6 PINS; THE LC OUTPUTS ARE ALL ZERO. 612 NANOSECONDS LATER, THE NEXT CHARACTER CODE IS EMITTED BY THE 8275. THIS PROCESS IS REPEATED UNTIL ALL 80 CHARACTERS HAVE BEEN OUTPUT. AT THIS TIME, THE 8275 GENERATES A HORI-ZONTAL RETRACE PULSE. THE 8253 CONVERTS THE HRTC PULSE INTO THE APPROPRIATE PULSE WIDTH FOR THE CRT MONITOR.

AT THE END OF THE FIRST RASTER LINE, THE 8275 INCREMENTS THE LC OUT-PUTS. THE NEXT NINE RASTER LINES ARE SIMILAR TO THE FIRST - THE 8275 OUTPUTS THE SAME 80 CHARACTER CODES ON THE CCU-CC6 PINS FOR EACH OF THE RASTER LINES, AND THE LC OUTPUTS ARE INCREMENTED AFTER EACH RASTER.

WHILE THE TEN RASTER LINES ARE BEING DISPLAYED, THE 8275 IS ALSO FILLING THE NEXT ROW BUFFER. AFTER THE TENTH RASTER LINE IS COMPLETED, THE 8275 RESETS THE LC COUNT, AND OUTPUTS CHARACTER CODES FOR THE SECOND ROW ON THE CCO-CC6 PINS. AS THIS ROW IS DISPLAYED, THE FIRST ROW BUFFER IS FILLED WITH INFORMATION FOR THE THIRD ROW. THE 8275 ALTERNATES ROW BUFFERS UNTIL ALL 25 ROWS ARE DISPLAYED. AT THIS TIME, THE VRTC SIGNAL IS ACTIVATED, AND THE COMPLETE PROCESS IS REPEATED FOR THE NEXT FRAME.

DURING THE DISPLAY, THE 8275 AUTOMATICALLY ACTIVATES THE VSP AND LTEN OUTPUTS'AS APPROPRIATE TO CONTROL RETRACE BLANKING, TO GENERATE THE CURSOR, OR TO UNDERLINE CHARACTERS.

### FOREGROUND AND BACKGROUND SOFTWARE

THE SOFTWARE FOR THE CRT CONTROLLER IS DIVIDED INTO TWO SECTIONS. THE FIRST SECTION CONTROLS HIGH PRIORITY FOREGROUND TASKS. THIS FOREGROUND SOFTWARE IS ACTIVATED EACH TIME THE 8275 REQUESTS AN 80 CHARACTER DISPLAY LINE BUFFER (THROUGH THE 8085A RST6.5 INTERRUPT). THE CRT LINE BUFFER IS FILLED BY PERFORMING 80 SEQUENTIAL MEMORY READS. AS EACH READ IS PERFORMED, THE HARDWARE AUTOMATICALLY SENDS A WRITE/DMA ACKNOWLEDGE TO THE 8275. THE PRESENCE OF SIMULTANEOUS MEMORY READ AND 8275 WRITE COMMANDS EFFECTS THE TRASFER OF A CHARACTER FROM THE 8185 RAM TO THE 8275 IN A SINGLE MEMORY CYCLE (WITHOUT A DMA CONTROLLER). IN THE INTEREST OF MINIMUM EXECUTION TIME, THE 80 READS ARE ACTUALLY PERFORMED USING THE CPU STACK POINTER AND 40 POP INSTRUCTIONS. THE COMPLETE REFRESH SEQUENCE FOR ONE LINE REQUIRES APPROXIMATELY 210 MICROSECONDS. THIS SEQUENCE IS REPEATED EVERY 612 MICROSECONDS. PROCESSOR OVERHEAD FOR REFRESH OPERATIONS IS APPROXIMATELY 35%.

KEYBOARD SCANNING IS ALSO INCLUDED IN THE FOREGROUND SOFTWARE. HOW-EVER, THIS SCANNING IS PERFORMED ONLY AT THE END OF EACH DISPLAY FRAME (AFTER 25 LINES/16.5 MILLISECONDS). IF A KEY DEPRESSION IS NOTED DURING ONE OF THESE SCANS, THE INFORMATION IS STORED FOR FURTHER BACKGROUND PROCESSING.

THE SECOND SOFTWARE SECTION HANDLES BACKGROUND PROCESSING. TASKS TO BE PERFORMED IN THE BACKGROUND INCLUDE MONITORING THE 8251A SERIAL I/O PORT, DEBOUNCING THE KEYBOARD, AND PROCESSING CHARACTERS ENTERED BY MEANS OF EITHER THE KEYBOARD OR THE SERIAL INTERFACE. THIS BACKGROUND SOFTWARE EXECUTES CONTINUOUSLY EXCEPT WHEN INTERRUPTED FOR THE HIGHER-PRIORITY FOREGROUND PROCESSING.

### REFRESH BUFFER MANAGEMENT

THE 2000 CHARACTERS TO BE DISPLAYED ON THE CRT SCREEN ARE STORED IN A MEMORY AREA COMMONLY CALLED THE REFRESH BUFFER. THE FOREGROUND SOFTWARE TRANSFERS ONE LINE (OF 80 CHARACTERS) AT A TIME TO THE 8275. TWO POINTERS ARE USED DURING NORMAL OPERATION. THE CURRENT LINE POINTER CONTAINS THE ADDRESS OF THE NEXT LINE TO BE DISPLAYED, AND THE BUFFER POINTER CONTAINS THE ADDRESS OF THE NEXT CRT BUFFER LOCATION TO BE WRITTEN INTO (FROM EITHER THE KEYBOARD OR THE SERIAL PORT). THE FOREGROUND PROCESSING SOFTWARE CONTROLS THE CURRENT LINE POINTER. THIS POINTER MUST ALWAYS BE CORRECT SO THAT A LINE CAN BE TRANSFERRED TO THE 8275 WHEN REQUESTED. THE BUFFER POINTER, ON THE

OTHER HAND, NORMALLY INDICATES THE CURRENT CURSOR LOCATION.

THE SIMPLEST REFRESH BUFFER ORGANIZATION ASSOCIATES THE FIRST MEMORY ADDRESS WITH THE UPPER LEFT POSITION ON THE CRT SCREEN. ALL OTHER CHARACTERS ARE STORED SEQUENTIALLY AS SHOWN IN FIGURE 5. THE MAJOR DISADVANTAGE OF THIS METHOD IS THE DIFFICULTY OF SCROLLING. SCROLLING A CRT SCREEN REQUIRES THAT EACH DISPLAY LINE BE MOVED UP ONE ROW (THE TOP LINE OF THE CRT IS LOST). THE BOTTOM LINE IS BLANKED AND THE CURSOR IS PLACED AT THE BEGINNING OF THIS LINE. IN ORDER TO SCROLL THE SCREEN WITH THIS FIXED SEQUENTIAL ORGANIZATION, ALL CHARACTERS IN THE REFRESH BUFFER MUST BE MOVED FORWARD BY 80 CHARACTERS (MEMORY LOCATIONS). THIS ACTION MOVES EACH LINE UP ONE ROW ON THE CRT. THE LAST 80 CHARACTERS IN THE BUFFER ARE THEN BLANKED. MOVING 1840 CHARACTERS EACH TIME THE SCREEN SCROLLS A SINGLE LINE IS A VERY SLOW AND COMBERSOME SCROLLING TECHNIQUE.

THIS LOW COST CRT CONTROLLER USES A SLIGHT MODIFICATION OF THE PRE-VIOUSY DESCRIBED TECHNIQUE THAT KEEPS THE SEQUENTIAL MEMORY URIENTA-TION WHILE AT THE SAME TIME ELIMINATING THE NEED TO MOVE CHARACTERS IN MEMORY. THIS TECHNIQUE REQUIRES AN ADDITIONAL DISPLAY START POINTER THAT POINTS TO THE MEMORY LOCATION OF THE FIRST CHARACTER TO BE DISPLAYED ON THE SCREEN. AT SYSTEM INITIALIZATION, THE DISPLAY START POINTER IS SET TO 6000H. DURING EACH VERTICAL RETRACE INTER-VAL, THE CURRENT LINE POINTER IS INITIALIZED FROM THE DISPLAY START POINTER. SCROLLING IS PERFORMED BY MERELY CHANGING THE DISPLAY START POINTER AND BLANKING THE OLD FIRST LINE (WHICH BECOMES THE NEW FINAL LINE) ON THE CRT SCREEN.

TO PERFORM A SINGLE LINE SCROLL, THE DISPLAY START POINTER IS MOVED AHEAD 80/ CHARACTERS TO LOCATION 6050H AND THE FIRST 80 CHARACTERS IN THE BUFFER ARE BL'ANKED. DURING THE NEXT VERTICAL RETRACE, THE FOREGROUND SOFTWARE SETS THE CURRENT LINE POINTER TO THE DISPLAY START LOCATION (6050H), AND BEGINS TRANSFERRING CHARACTERS TO THE 8275 FROM THIS ADDRESS. THE CHARACTER IN MEMORY LOCATION 6050H (PREVIOUSLY THE FIRST CHARACTER IN THE SECOND ROW) NOW OCCUPIES THE FIRST DISPLAY POSITION ON THE CRT SCREEN (FIRST CHARACTER OF THE FIRST ROW). WHEN THE FOREGROUND SOFTWARE REACHES THE END OF THE DISPLAY BUFFER, THE NEXT LINE IS READ FROM THE BEGINNING OF THE BUFFER (LOCATION 6000H). THIS ACTION CAUSES THE FIRST 80 CHARACTERS IN THE BUFFER TO APPEAR ON THE LASTDISPLAY LINE (FIGURE 6). EACH SUBSEQUENT SCROLL MOVES THE DISPLAY START POINTER FORWARD BY 80 CHARACTERS, AND ALL BUFFER OPERATIONS AUTOMATICALLY ROLL OVER TO THE PHYSICAL BEGINNING OF THE BUFFER AFTER PASSING THE LAST BUFFER LOCATION.

SINCE THE LINE-BY-LINE DISPLAY OF CHARACTERS IS CONTROLLED BY THE 8085A SOFTWARE, OTHER DISPLAY TECHNIQUES MAY BE USED. IN PARTICULAR, A LINKED LIST STRUCTURE IS EXTREMELY ADAPTABLE TO WORD PROCESSING AND TEXT EDITING FUNCTIONS. THIS METHOD ALLOWS EACH LINE (WITHIN A FILE) TO BE CHANGED INDEPENDENTLY OF OTHER LINES. THE LINES ARE LINKED OR CHAINED TOGETHER BY POINTERS. LINES MAY BE EASILY INSERTED OR DELETED BY SIMPLY CHANGING POINTERS. TO DISPLAY A CRT FRAME, THE PROCESSOR FOLLOWS THE POINTER CHAIN FROM ONE LINE TO THE NEXT.

### KEYBOARD INTERFACE

THE KEYBOARD USED IN THIS DESIGN WAS A SIMPLE UNENCODED ASCII KEY-BOARD. IN ORDER TO KEEP THE COST TO A MINIMUM A SIMPLE SCAN MATRIX TECHNIQUE WAS IMPLEMENTED BY USING TWO PORTS OF AN 8255 PARALLEL I/O DEVICE.

WHEN THE SYSTEM IS INITIALIZED THE CONTENTS OF THE EIGHT KEYBOARD RAM LOCATIONS ARE SET TO ZERO. ONCE EVERY FRAME, WHICH IS 16.67 MILLI-SECONDS, THE CONTENTS OF THE KEYBOARD RAM IS READ AND THEN REWKITTEN WITH THE CONTENTS OF THE CURRENT SWITCH MATRIX. IF A NONZERO VALUE OF ONE OF THE KEYBOARD RAM LOCATIONS IS FOUND TO BE THE SAME AS THE CORRESPONDING CURRENT SWITCH MATRIX, A VALID KEY PUSH IS REGISTERED AND ACTION IS TAKEN. BY OPERATING THE KEYBOARD SCAN IN THIS MANNER AN AUTOMATIC DEBOUNCE TIME OF 16.67 MILLISECONDS IS PROVIDED.

THE FIGURE BELOW SHOWS THE ACTUAL PHYSICAL LAYOUT OF THE KEYBOARD AND FIGURE 28 SHOWS HOW THE INDIVIDUAL KEYS WERE ENCODED. ON FIGURE 28 THE SCAN LINES ARE THE NUMBERS ON THE BOTTOM OF EACH KEY POSITION AND THE RETURN LINES ARE THE NUMBERS AT THE TOP OF EACH KEY POSITION. THE SHIFT, CONTROL AND CAPS LOCK KEY WERE BROUGHT IN THROUGH SEPARATE LINES OF PORT C OF THE 8255.

IN ORDER TO GUARANTEE THAT TWO SCAN LINES COULD NOT BE SHORTED TOGETHER IF TWO OR MORE KEYS ARE PUSHED SIMULTANEOUSLY, ISOLATION DIODES COULD BE ADDED.

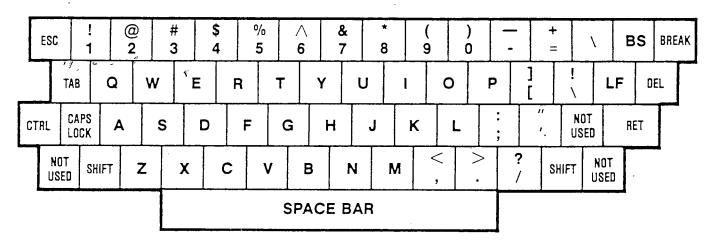
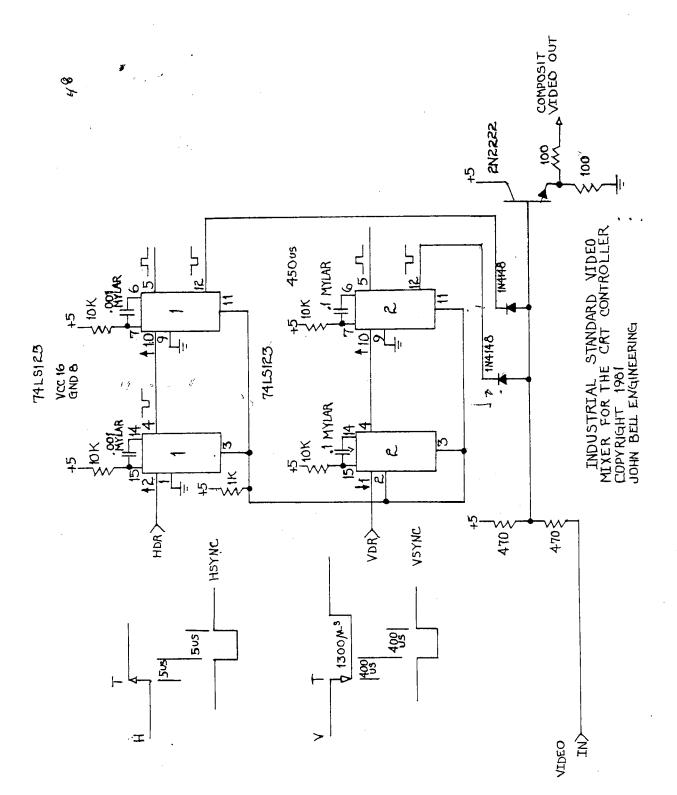


FIGURE 2A - KEYBOARD LAYOUT

7 C		7 1	7 2	2	7	7	7	7 5	7 6		2 7	0		0	0 2	- 1	0	0		0 5	0	0 7	- 1
	6 0		6 1	6 2		6 4	6 5	- 1	6 6	5 0	1		1	1 2		1 3	1		1 5	1 6		1	
PORT C	PO PO	RT	4	1	6 3	5 4	5	- 1	5 6	5 7		2	2		2 2	2 3		2 4	3 5		2		
	4 0	POF POF	IT	4 2	3	·	4	4 5	1	4 6	4 7	1	3	3 1	ł	3 2	3		ĀT C	3 6			
		5 3																					

TOP NUMBER = RETURN LINE BOTTOM NUMBER = SCAN LINE



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## JOHN BELL ENGINEERING, INC.

CRT BOARD DIP SWITCH SETTING

### DIP SWITCH SETTINGS

THE BAUD RATE SWITCHES ARE SET AS FOLLOWS

BAUD	S 0	S1	S 2
	(PIN 4-13)	(PIN 3-14)	(PIN 2-15)
			•
110	ON	ON	ON
150	OFF	ON	ON
300	ON	OFF	ON
600	OFF	OFF	ON
1200	ON	ON	OFF
2400	OFF	ON	OFF
4800	ON	OFF	OFF
9600	OFF	OFF	OFF
1.6			

THE LOCAL SWITCH (PIN 7-10)

SHOULD BE ON FOR FULL DUPLEX OPERATION. IN THIS MODE THE TERMINAL WILL GET A CHARACTER FORM THE KEYBORAD, SEND IT OUT THE USART TO A SYSTEM VIA RS232 AND EXPECT THE EXTERNAL SYSTEM (USUALLY A COMPUTER) TO "ECHO" THE CHARACTER BACK TO THE CRT BOARD AND ONLY THEN IS IT PRINTED ON THE SCREEN.

WHEN THE LOCAL SWITCH IS OFF, THE TERMINAL IS IN A SORT OF STAND ALONE, OR LOCAL MODE WHERE CHARACTERS COMING FROM THE RS232 INPUT TO THE CPU BOARD ARE NOT PRINTED BUT ANY CHARACTER TYPED ON THE KEYBOARD IS PRINTED BY THE CRT BOARD.

NO CHARACTERS ARE SENT TO THE CPU IN THIS MODE.

### THE CAPITAL LOCK SWITCH (PIN 8-9)

WHEN THIS SWITCH IS CLOSED, ALL LETTERS COMING FROM THE KEYBOARD ARE TYPED ON THE SCREEN IN CAPITAL LETTERS. WHEN THE SWITCH IS OFF, THE SHIFT KEY MUST BE USED TO GET THE CAPITAL LETTERS.

# JOHN BELL ENGINEERING, INC.

### USART JUMPERS

FOR R\$232 OPERATION, NO HANDSHAKE

1. PUT JUMPERS IN CTS PIN 3 TO 4, AND ALSO IN CTS CENTER TO POSITION "T"

THEN GROUND PIN 23,24 OF J1, THIS ENABLES USART TO SEND CHARACTERS.

PLACE JUMPER FOR WHAT TYPE OF RS232 SIGNAL LEVEL WILL BE RECEIVED AS FOLLOWS:

TTL LEVEL SIGNAL JUMPER R X D FROM "T" TO CENTER AND HOOK UP RS232 SIGNAL FROM COMPUTER TO PIN 15, 16 OR JI

RS232 LEVELS( 10V) JUMPER R X D FROM "R" TO CENTER AND HOOK UP RS232 DATA LINE FROM THE EXTERNAL COMPUTER (MOST COMMON) TO PIN 25, 26 JI

JUMPER FOR WHAT LEVEL SIGNAL TO USE ON RS232 OUTPUT TO THE EXTERNAL COMPUTER

> TTL LEVEL SIGNAL TIE PIN 21, 22 ON JI TO DATA TO SEND LINE ON RS232 LINK TO COMPUTER

RS232 STANDARD LEVEL TIE PIN 31, 32 ON JI TO DATA LINE ON RS232 LINK TO EXTERNAL COMPUTER OUTPUT (MOST COMMON)

### NOTE:

- IF TTL LEVEL SIGNALS ARE GOING TO BE USED FOR THE 1. COMMUNICATION TO THE CPU, A1, AND A2 CAN BE DELETED AND NO - 12 VOLT SUPPLY WILL BE NEEDED
- CLEAR TO SEND CTS, AND READY TO SEND RTS SIGNALS ARE 2. AVAILABLE IN BOTH RS232 LEVELS (+ 10 V) AND TTL LEVELS ON JI, THESE SIGNALS CAN BE USED FOR HANDSHAKING DATA TRANSFERS OVER THE RS232 LINK.



# JOHN BELL ENGINEERING, INC.

### SHIFT & CONTROL

THE SHIFT AND CONTROL KEYS ARE NOT USED FOR (PIN 5-12) (PIN 6-11)ON S1 ON SI

THE ASCII ENCODED KEYBOARD SOFTWARE

### ESCAPE CODES - SPECIAL FUNCTIONS

LETTER AFTER ESCAPE CHARACTER	FUNCTION
B E J K A	MOVE CURSER DOWN CLEAR SCREEN CLEAR REST OF SCREEN BELOW CURSER CLEARS LINE CURSER IS ON MOVE CURSER UP ONE LINE MOVE CURSER RIGHT ONE CHARACTER MOVE CURSER LEFT ONE CHARACTER
Н	HOME CURSER TO UPPER LEFT SCREEN

### CONTROL KEYS

THE BOARD RECOGNIZES CONTROL CHARACTERS THAT ARE KEYED IN FROM THE ASCII ENCODED KEYBOARD OR SENT VIA THE USART.

### FIELD ATTRIBUTES

SEE ATTACHMENT

PIN 36 OF J2 MUST BE TIED LOW

TO DISABLE THE INTERPRETATION OF ASCII CHARACTERS AS FIELD ATTRIBUTES OR SPECIAL CODES.

THIS PIN MAY BE USED AS AN INPUT WHEN FIELD ATTRIBUTES ARE USED BUT MUST REMAIN LOW WHEN ASCII IS INPUT VIA THE KEYBOARD.

### intel

#### Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

### Special Control Character

s s	FUNCTION
0 0	End of Row
0 1	End of Row-Stop DMA
1 0	End of Screen
1 1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.  $\cdot$ 

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

### Field Attributes

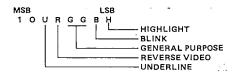
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the

character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

#### There are six field attributes:

- Blink Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
- Highlight Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
- Reverse Video Characters following the code are caused to appear with reverse video by, activating the Reverse Video output (RVV).
- Underline Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).
- 5,6. General Purpose There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. GPA<sub>0-1</sub> are active high outputs.

#### Field Attribute Code



H = 1 FOR HIGHLIGHTING B = 1 FOR BLINKING

R = 1 FOR REVERSE VIDEO

U = 1 FOR UNDERLINE

 $GG = GPA_1, GPA_0$ 

\*More than one attribute can be enabled at the same time.

If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

CRT A12 ASCII VERSION

THIS EXPLAINS THE HARDWARE INTERFACE TO BE USED WITH THE NEW SOFTWARE UPDATED 11/81 BY MJ IN THE JOHN BELL CRT DEMO.

THE KEYBOARD SHOULD BE A 7 BIT ASCII DECODED KEYBOARD WITH POSITIVE TRUE OUTPUTS AND A POSITIVE GOING STROBE. THE STROBE SHOULD LAST A MINIMUM OF ABOUT 2 FRAMES (35 MS). THE DEBOUNCING OPTION THAT WAS IN THE ORIGIONAL SOFTWARE IS STILL IMPLEMENTED IN THIS SOFTWARE. IF THE CRT BOARD DOES NOT GET THE SAME DATA AFTER A FRAME, THE DEBOUNCE IS NOT COMPLETE AND THE CHARACTER IS REJECTED.

THE STROBE FOR THE KEYBOARD SHOULD BE GOING TO PORT B OF THE 8255, ON THE LEAST SIGNIFICANT BIT, PIN 1 ON J2. ...

THE ASCII DATA SHOULD BE GOING TO PORT A WITHTHE FOLLOWING CONNECTIONS:

ASCII E	3 I T	PIN	ON	J2	BIT	ΟF	PORT	Α
. В1			29			PAC	)	
B2			30			PA]	l	
В3			31			PA2	2	
В4			32			PA	3	
19 B.5	€.		33			PAL	+	
19 B.5 B.6		1 2	34			PAS	5	
В7	(MSB)		35			PAG	5	

NOTE: PIN 36 OF J2 SHOULD BE GROUNDED.

Please specify when ordering

\* . . . . . .

21F8- 38 44 04 08 10 10 00 10

\* . . .

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2000- F3 31 00 68 21 00 60 22
2008- D6 67 22 D4 67 21 DA 67
2010- OE 0B 36 00 23 0D C2 12
2018- 00 36 19 01 D0 67 21 00
2020- 60 1E 20 73 23 7D B9 C2
2020- 60 1E 20 73 23 7D B9 C2
2028- 23 00 7C B8 C2 23 00 C3
2030- AD 00 00 00 F5 D5 E5 21
2038- 00 03 9 EB 2A D4 67 31
2040- 00 10 39 FB 2A D4 67 31
2040- 00 10 39 FB 1E 1E 1E 1E 1E 12
2050- E1 21
2050- E1 21
2050- E1 21
2068- E1 21
2068- E1 21
2077- EB F9 21 30 98 19 EB D2
2078- 7D 00 21 00 60 C2 D4 67
2078- 7D 00 21 00 60 C2 D4 67
2079- BA C2 40 E6 07 21 DF 67
2099- BA C2 40 E6 07 21 DF 67
2099- BB C4 B9 04 3A DD 67 E6
2099- BB C4 B9 04 3A DD 67 E6
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 D1 F1 FB C9 SE 9B 32
2008- E1 C4 B9 04 TA DD 67
E1 BB C4 B9 04
E1 B 2000- F3 31 00 68 21 00 60 22

\*

2200- C3 06 01 3A E1 67 E6 04 2300- FE 4F C2 1C 03 3A DA 67 2208- C2 13 02 3E 00 32 E1 67 2308- FE 18 CA 11 03 3C 32 DA 2210- C3 06 01 3A DC 67 D6 20 2310- 67 3E 00 32 DB 67 CD 70 2218- 32 DB 67 3A E4 67 32 DA 2318- 03 C3 06 01 3C 32 DB 67 CD 70 2320- CD 70 03 C3 06 01 3C 32 DB 67 CD 70 2320- CD 70 03 C3 06 01 3C 32 DB 67 CD 70 2320- CD 70 03 C3 06 01 3C 3A DB 62 CD 70 2330- 40 45 00 C5 10 CD 40 C1 2330- 67 FE 00 CA 06 01 3D 32 238- 04 E1 CD C1 80 A5 CD 40 2338- DA 67 3E AF 32 DB 67 CD 2240- 3B 3A DC 67 E5 CD 65 TD CD 40 C1 2330- 67 FE 00 CA 06 01 3D 32 DB 2238- 67 FE 10 CD 40 CD 2348- 67 DD 03 C3 06 01 3D 32 DB 2248- 67 3E 00 32 E1 67 3A DC 2340- 70 03 C3 06 01 3D 32 DB 2248- 67 3E 00 32 E1 67 3A DC 2348- 67 CD 70 03 C3 06 01 3D 32 DB 2258- CA 9D 02 FE 4A CA A3 02 2358- DA 67 CD 03 C3 06 01 3E 03 02 CD 2260- FE 4B CA BF 02 FE 41 CA 2360- E1 67 C3 06 01 3E 03 32 2266- FE 4B CA BF 02 FE 41 CA 2360- E1 67 C3 06 01 3E 03 32 2266- FE 4B CA BF 02 FE 44 CA 2360- E1 67 C3 06 01 3E 03 32 2268- CD 70 03 C3 06 01 3C DS 00 A7 FE 2388- DB 67 CD 70 03 C3 06 01 3E 03 32 2268- EB 02 FE 43 CA FD 02 FE 41 CA 2360- E1 67 C3 06 01 3E 00 32 2268- CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3E 00 32 2268- CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 22 DB 67 CD 2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 00 03 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 03 C3 06 01 3C DS 00 A7 FE E2388- DB 67 CD 70 CD 70 CD 70 CD A0 C2288- DB 06 CD 70 CD 70

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2400- E5 E5 E5 E5 E5 E5 E5 2408- E5 E5 EB F9 FB C9 2A D6 
 2410- 67
 22
 D8
 67
 11
 50
 00
 19
 2510- 35
 36
 00
 24
 28
 29
 5F
 BB
 2418- EB
 21
 30
 98
 19
 EB
 D2
 24
 2518- 00
 08
 00
 55
 49
 4F
 50
 5D

 2420- 04
 21
 00
 60
 22
 D6
 67
 CD
 2520- 00
 0A
 7F
 4A
 4B
 4C
 3A
 22

 2428- 00
 04
 7E
 FE
 FO
 22
 D8
 67
 CC
 2530- 00
 00
 00
 04
 1,5 \$\tilde{5}
 5B
 43

 2438- 00
 03
 2A
 D8
 67
 CD
 79
 04
 2538- 56
 24
 4E
 59
 00
 00
 20
 44

 2448- 52
 50
 02
 53
 04
 CD
 B7
 03
 2548- 52
 54
 00
 18
 21
 40< 2410- 67 22 D8 67 11 50 00 19 24D0- 07 D0 07 38 39 30 2D 3D 24D8- 5C 08 00 75 69 6F 70 5B 24EO- 5C OA 7F 6A 6B 6C 3B 27 
 24E8- 00 0D 37 6D 2C 2E 2F 00
 25E8- 00 00 00 00 00 00 00 00

 24F0- 00 00 00 00 61 7A 7B 63
 25F0- 00 00 00 00 00 00 00

 24F8- 76 62 6E 79 00 00 20 64
 25F8- 00 00 00 00 00 00 00

2500- 66 67 68 00 71 77 73 65 2508- 72 74 00 1B 31 32 33 34 2510- 35 36 00 2A 28 29 5F 2B 2518- 00 08 00 55 49 4F 50 5D 25DO- FF FF FF FF FF FF FF 25D8- FF FF FF FF FF FF FF 25E0- 00 00 00 00 00 00 00 00