Chapter 2: Programmable Logic Device

Logic circuit design review

- Sum of Product

- To get the desired canonical SOP expression we will add the minterms (product terms) for which the output is 1.

A	B		F		A	B		F		Minterm
0	0		0		0	0		0		A'B'
0	1		1		0	1		1		A'B
1	0		1		1	0		1		AB'
1	1		1		1	1		1		AB

- F = A'B + AB' + AB

- Product of Sums (POS)
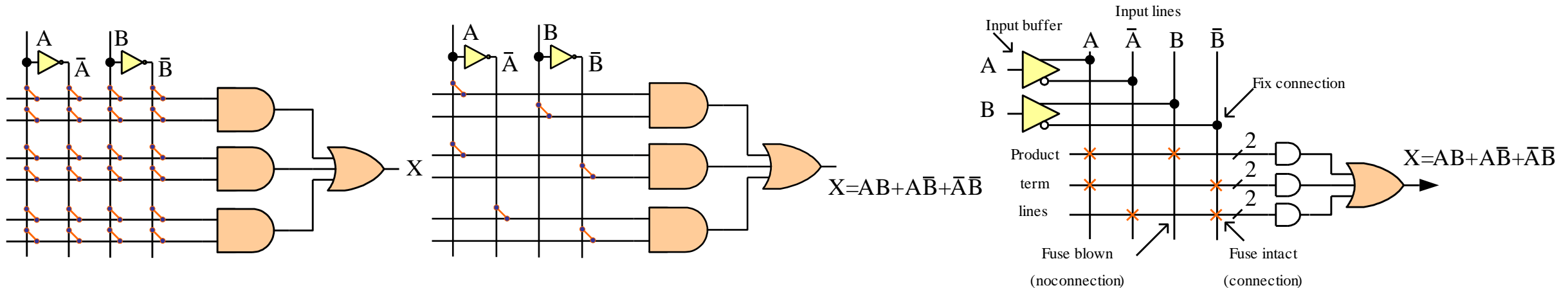- To get the desired canonical POS expression we will multiply the maxterms (sum terms) for which the output is 0.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

A	B	F	Maxterm
0	0	0	A+B
0	1	1	A+B'
1	0	1	A'+B
1	1	0	A'+B'

- F = (A+B) . (A'+B')

Simple Programmable Logic Device (SPLD)

- Programmable Array Logic (PAL)

- Generic Array Logic (GAL)

- The structure of PAL and GAL is composed of the programmable AND followed by the programmable OR gate.

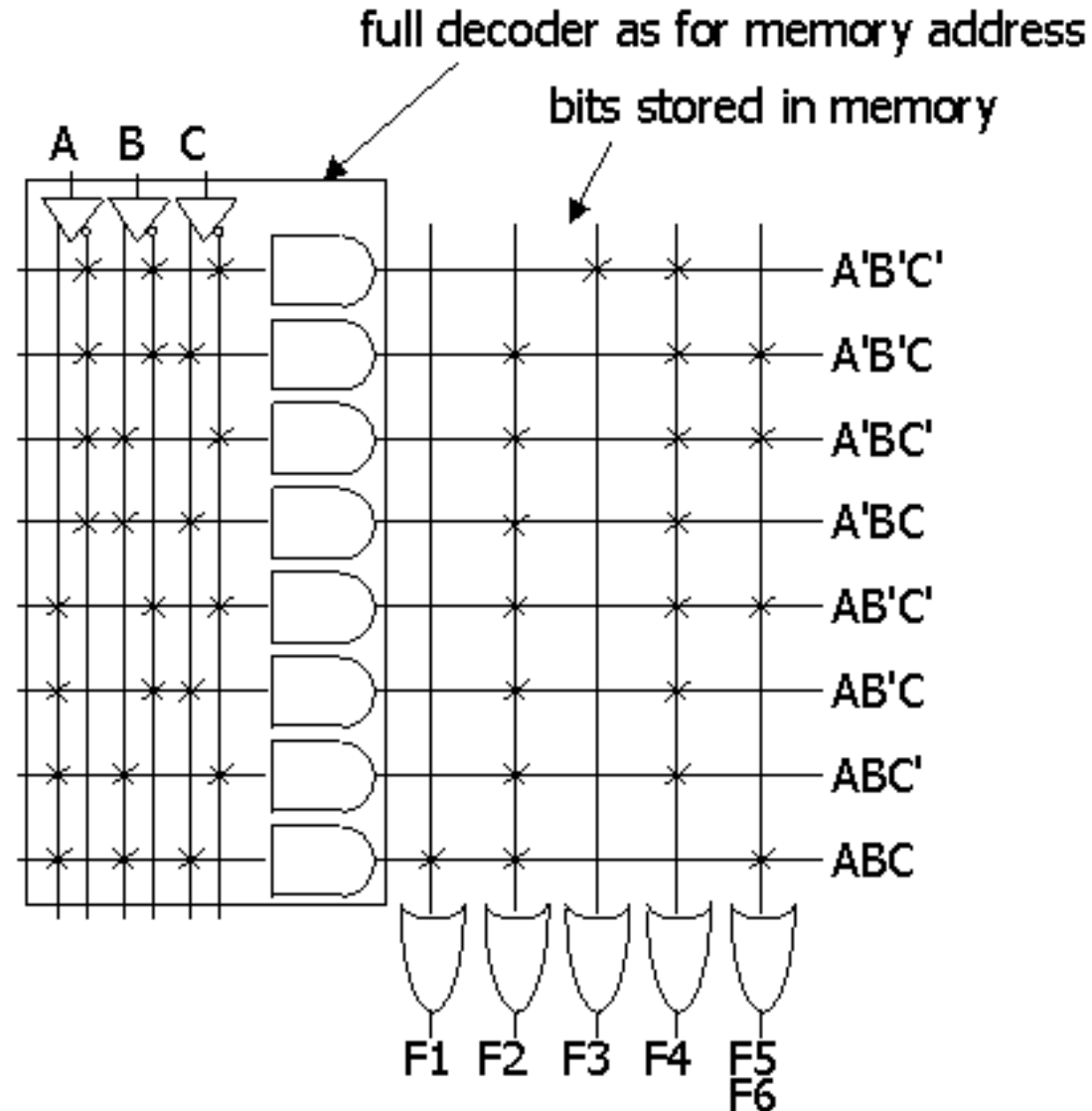- PAL, GAL can be used to configure the Sum of Product logic circuit.
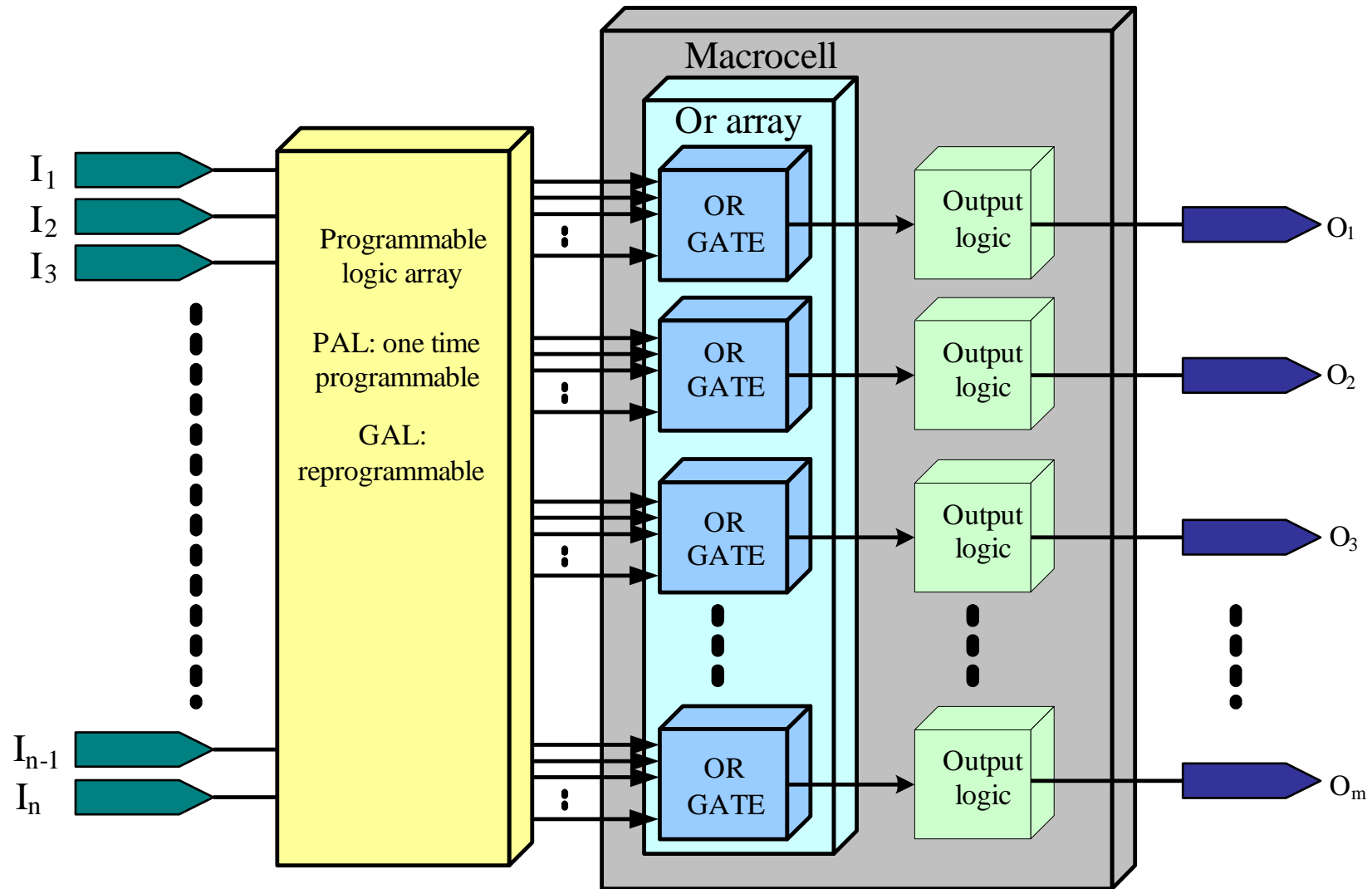
Example of PAL configuration

- Multiple functions of A, B, C
  - F1 = A B C
  - F2 = A + B + C
  - F3 = A' B' C'
  - F4 = A' + B' + C'
  - F5 = A xor B xor C
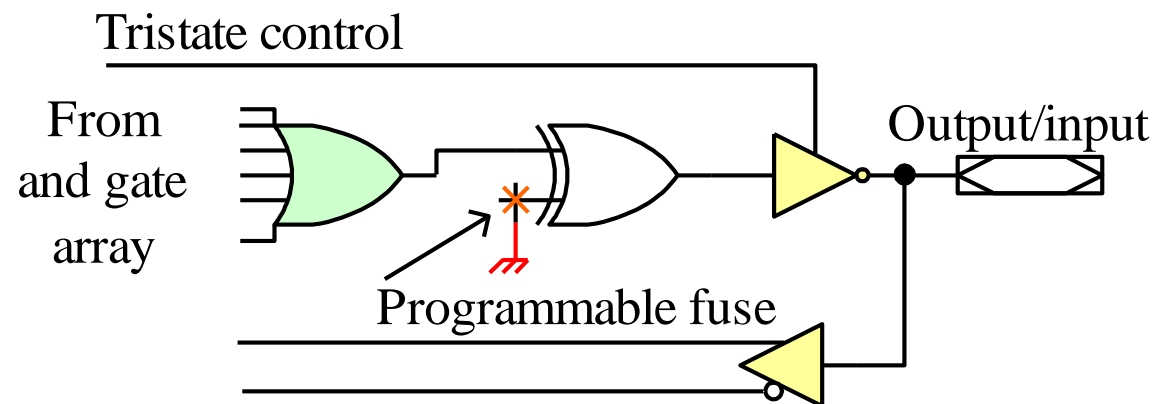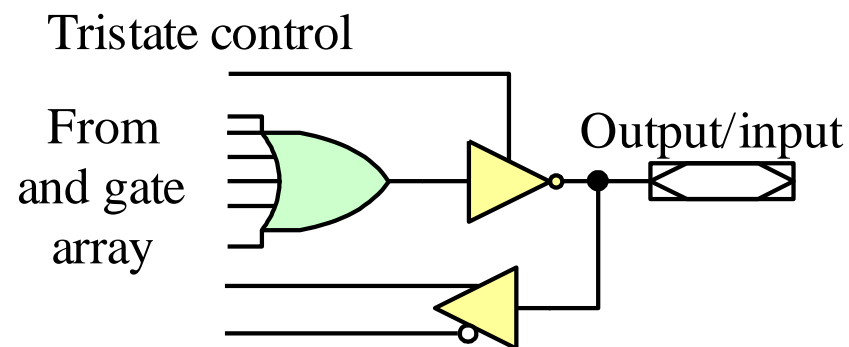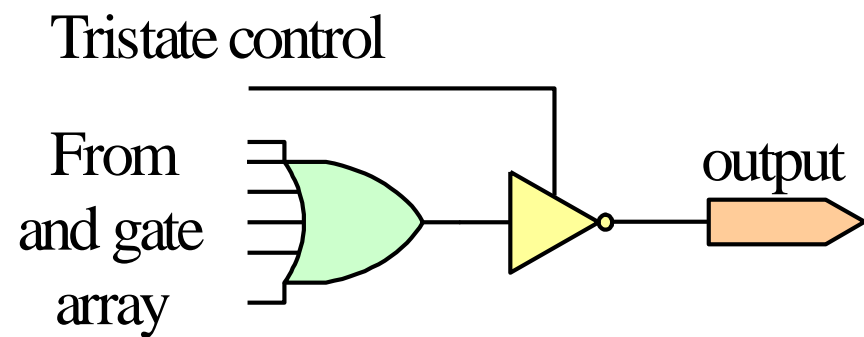 - F6 = A xnor B xnor C

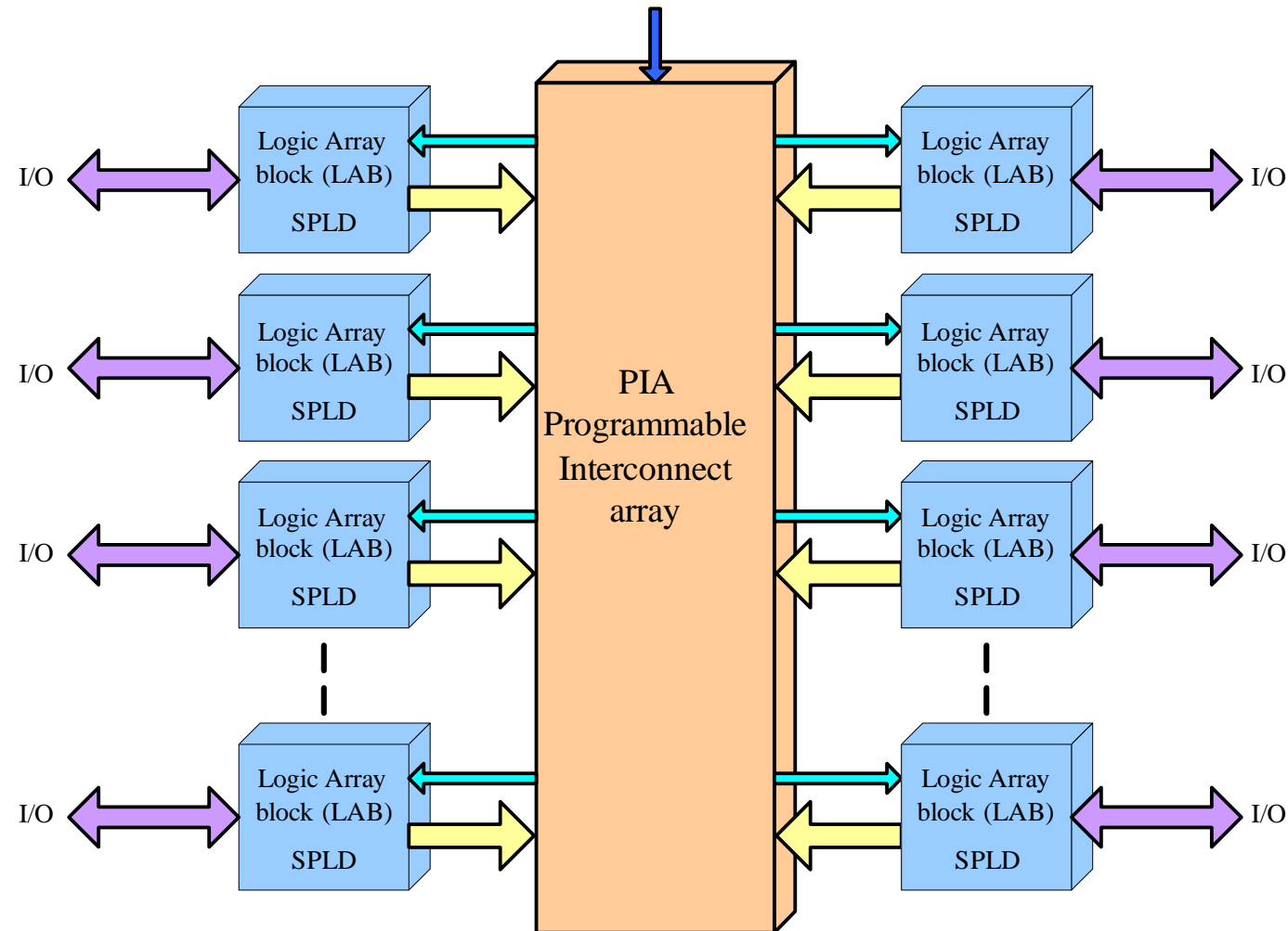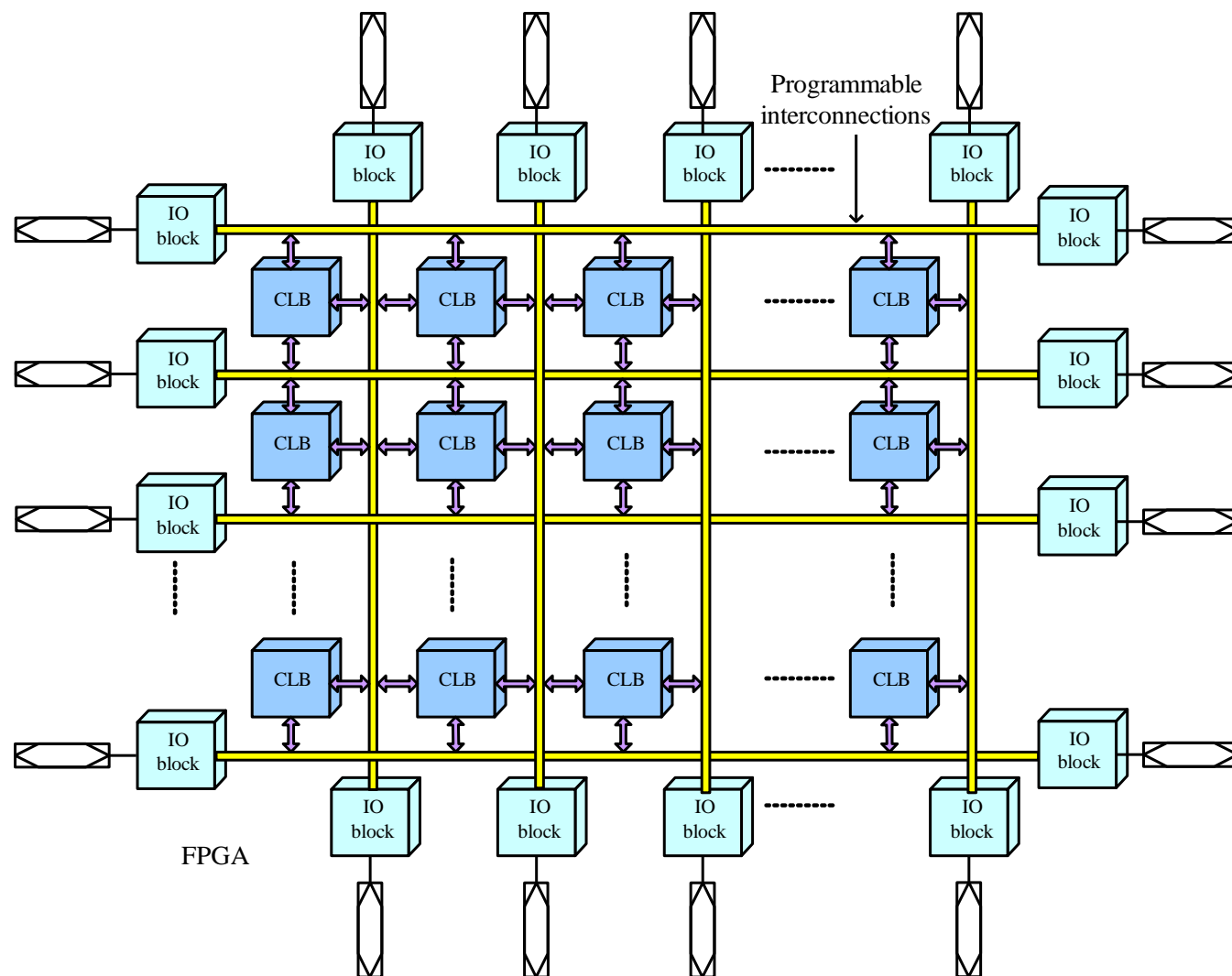| A	B	C	F1	F2	F3	F4	F5	F6
0	0	0	0	0	1	1	0	0
0	0	1	0	1	0	1	1	1
0	1	0	0	1	0	1	1	1
0	1	1	0	1	0	1	0	0
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	1	0	0
1	1	1	1	1	0	0	1	1

full decoder as for memory address

bits stored in memory

A B C

A'B'C'

A'B'C

A'BC'

A'BC

AB'C'

AB'C

ABC'

ABC

F1 F2 F3 F4 F5
                 F6

PAL /GAL

Macrocell

Complex Programmable Logic Device (CPLD)

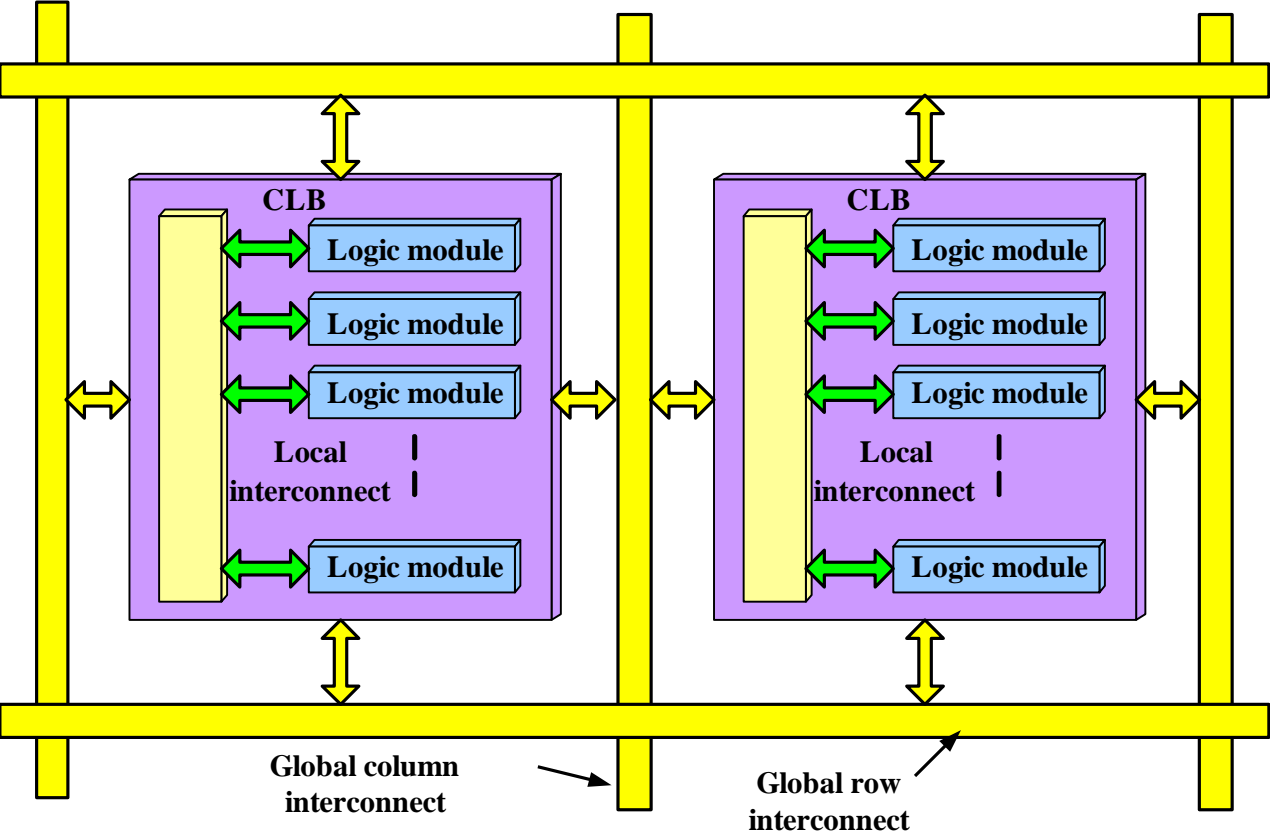- CPLD is consist of SPLDs

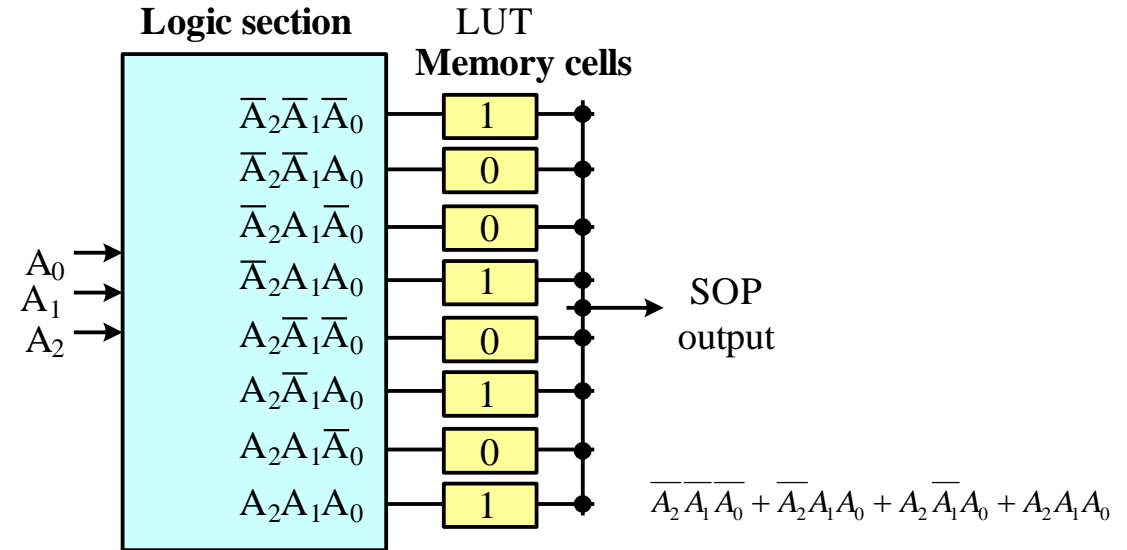# Field Programmable Gate Array)

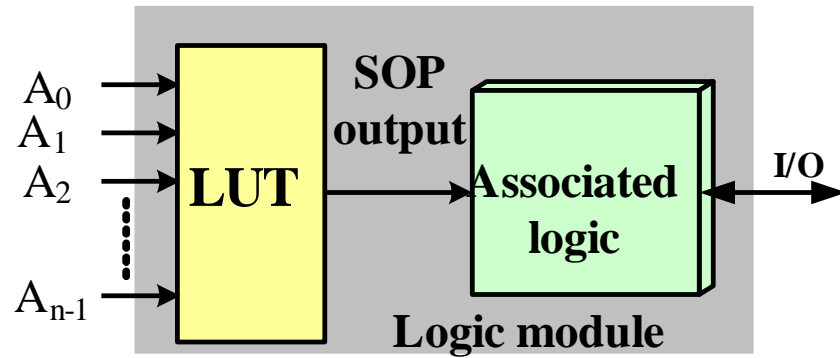

Configurable Logic Block (CLB)

CLB

Logic Module – Lookup table (LUT)

LUT

$$A_2 A_1 \overline{A_0} + A_2 \overline{A_1} \, \overline{A_0} + \overline{A_2} A_1 A_0 + A_2 \overline{A_1} A_0 + \overline{A_2} \, \overline{A_1} A_0$$