Radiation Hardened FPGA Technology for Space Applications

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Abstract—High performance, high density, radiation hardened Field Programmable Gate Arrays (FPGAs) are in great demand for military and space applications to reduce design cost and cycle time. BAE Systems has implemented radiation hardened 150nm bulk CMOS process technology in its foundry located in Manassas, VA to support such advanced product needs. BAE Systems and Actel Corporation are collaborating to bring the next-generation radiation hardened FPGA product for space applications to market. This paper will describe the rad hard AX-250 FPGA and the electrical and radiation test data on rad hard 150nm product hardware, FPGA device structures and anti-fuse arrays, as part of the overall FPGA product installation and qualification effort.

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1. INTRODUCTION

There is increasing demand for high density radiation hardened Field Programmable Gate Arrays (FPGAs) to be used in advanced military and space applications. The recently modernized foundry at BAE Systems in Manassas, VA offers strategically radiation hardened fully-scaled 150nm bulk CMOS process technology (RH15) [1]. This rad hard 150nm process technology supports advanced FPGA product, among other products and services.

BAE Systems has for over 25 years been a leading rad hard supplier. Actel Corporation is a recognized leading supplier of commercial FPGA product. BAE Systems and Actel have collaborated for over 12 years as suppliers of 0.8 µm anti-fuse based radiation hardened FPGAs. Building on this past experience, Actel's new metal-to-metal antifuse based AX-250 FPGA is being installed in BAE Systems' process facility at the 150nm technology node so that strategically hardened parts having same form, fit and function as the commercial version, are available for the next generation military and space systems [2].

The implementation approach being followed to install and qualify an antifuse based radiation hardened AX250 FPGA at RH15 is depicted in Figure 1.

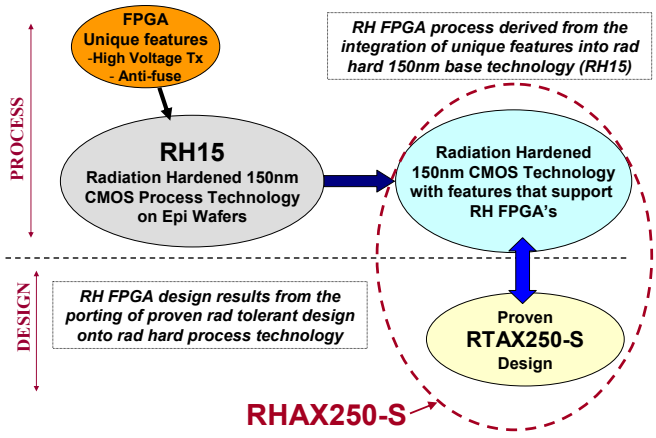

Figure 1. Rad Hard FPGA Installation and Qualification Approach.

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The unique features to support the FPGA, anti-fuses and high voltage programming transistors, have been integrated into the base RH15 technology. The hardware validated, radiation tolerant, 250K-gate FPGA design (RTAX250-S) was then ported to this technology providing a low-risk path to the final strategically radiation hardened, flight-qualified FPGA product, RHAX250-S. The radiation hardened RHAX250-S FPGA product will have the identical form, fit, and function as its radiation tolerant counterpart, RTAX250-S. A detailed description of the architecture, design tools and support for the RTAX250-S can be obtained from the Actel website, www.actel.com.

Currently, full RHAX250-S product prototypes have been built and tested. QML qualification is slated to begin in 2007 with flight production readiness targeted by yearend 2007.

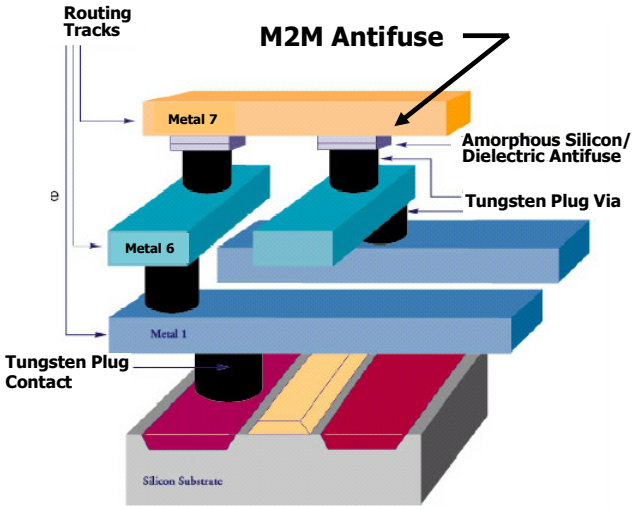

Figure 3. Illustration of the Antifuse Placement.

2. TECHNOLOGY FEATURES

The key features of RH15, the fully-scaled radiation hardened base 150nm CMOS technology, are provided in Figure 2 on a magnified image of the physical cross-section of the seven-level planarized metallization stack. This technology features high performance 150nm transistors and seven levels of metallization. A Dual Gate Oxide (DGO) process enables 1.5V / 3.3V operation. Into this base 150nm technology the added features needed for the FPGA, metal-to-metal antifuses and the high voltage programming transistors, have been integrated. The vertical profile of the DGO device was modified and optimized to enable high voltage programming transistors. The metal-to-metal (M2M) antifuses are placed between the sixth and seventh level metals, as illustrated in Figure 3. A magnified image of a section of the layout for the antifuse array provides a top view of the antifuse design in Figure 4.

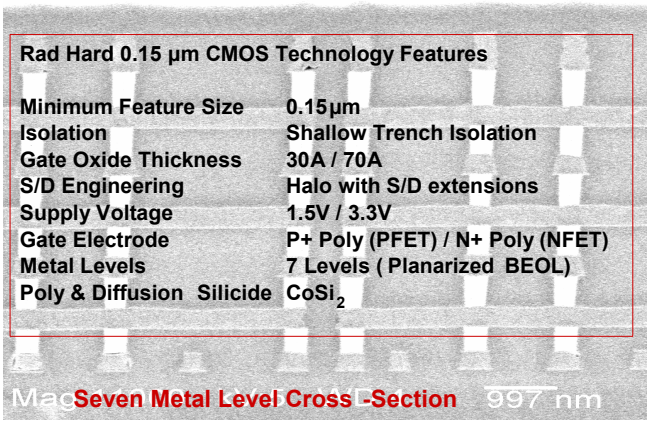

Figure 2. Radiation Hardened 150nm CMOS technology (RH15).

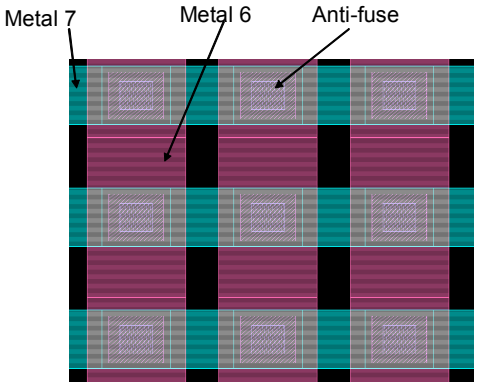

Figure 4. Magnified Section of Antifuse Array.

Antifuse arrays have been built and stressed to determine adequacy of their breakdown voltage and leakage margins. The antifuse stack must have a breakdown voltage that exceeds 4.2V to accommodate the antifuse programming regimen, and with an applied 3.0V, leakage through the antifuse stack of a 1K antifuse array must less than 100µA. Figure 5 shows the breakdown test results on a 1K antifuse array. The principal breakdown voltage distribution easily exceeds the >4.2V requirement while the 3.0V leakage distribution shown in Figure 6 far exceeds the <100 µA requirement. These test results confirm that the antifuse process module integrated into the base RH15 technology clearly supports the FPGA product.

RHAX250-S product will be subjected to a rigorous set of radiation and reliability tests to comprehensively assess the robustness of the technology and the product design across expanded voltage levels, temperature ranges, and operational modes. Testing is slated to begin in early 2007 and will

include a thorough assessment of the integrity of the antifuse and the supporting CMOS process technology, including extended accelerated life testing.

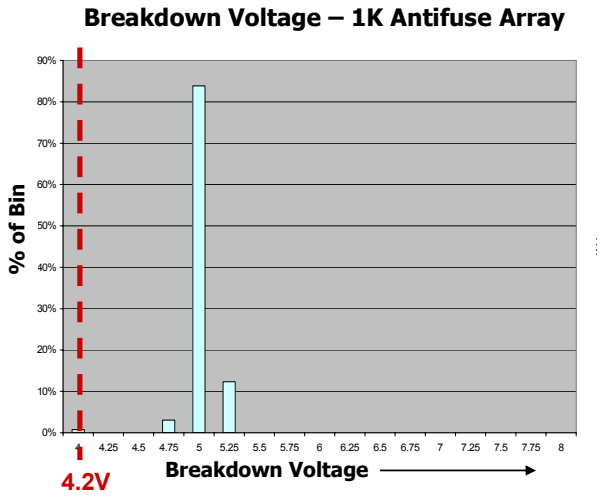

Figure 5. Antifuse Array Breakdown Voltage Distribution.

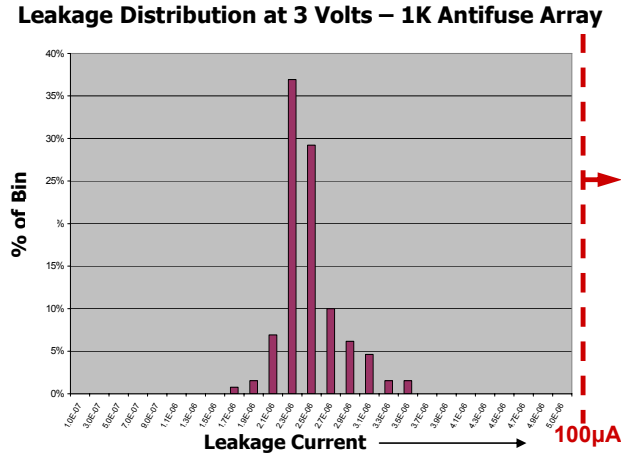

Figure 6. Antifuse Array Leakage Distribution.

3. PRODUCT DESCRIPTION

The BAE Systems rad hard 150nm antifuse based FPGA process will support the Actel RTAX250-S FPGA, transforming this radiation tolerant design into a strategically radiation hardened product, RHAX250-S, with >1Mrad(Si) total ionizing dose (TID) hardness. In addition to >1Mrad(Si) TID hardness, RHAX250-S devices offer inherent single-event latch-up (SEL) immunity and demonstrated hardness against single-event upsets (SEU) of < 1E-10 errors/bit-day for the registers that are designed using flip-flops, each having linear energy threshold (LET) > 37MeV-cm^2/mg, in a triple modular redundant (TMR) configuration. The FPGA also features embedded RAM with an upset rate of <1E-10 errors/bit-day with error detection and correction (EDAC). With 250,000 system gates, or 30,000 ASIC-equivalent gates, the RHAX250-S supports 54K bits of embedded SRAM, 248 user I/Os, and 1,408 SEU-hardened registers. The RHAX250-S product profile is shown in Table 1. The radiation hardness assurance levels targeted for this product are provided in Table 2. Its leading-edge performance attributes are listed in Table 3.

Table 1. RHAX250-S Product Profile.

Device	RHAX250-S
Capacity	
Equivalent System Gates	250,000
ASIC Gates	30,000
Modules	
Register (R-Cells)	1,408
Combinatorial (C-Cells)	2,816
Flip-Flops (Maximum)	2,816
Embedded RAM/FIFO (without EDAC)	
Core RAM Blocks	12
Core RAM Bits (K = 1,024)	54 K
Clocks Segmentable	
Hardwired	4
Routed	4
I/O's	
I/O Banks	8
User I/O's (Maximum)	248
I/O Registers	744
Package	
CCGA/LGA	-
CQFP	208, 352

Table 2. RHAX250-S Radiation Hard Assurance Levels.

TID	≥1Mrad(Si)
SEL	Immune
SEU_{REGS}	< 1E-10 errors/bit-day (TMR-hardened)
$SEU_{e\text{-}RAM}$	< 1E-10 errors/bit-day (EDAC)

Table 3. RHAS250-S Performance Targets.

1.5V Core; 3.3V I/O
High-Performance Embedded FIFOs
350+ MHz System Performance
500+ MHz Internal Performance
700 Mb/s LVDS Capable I/Os

4. RADIATION HARDNESS

The natural space environment is a highly energetic, charged environment where spacecraft electronics are subjected to radiation from a variety of sources. There are two primary radiation effects in the natural space environment in the absence of burst phenomena from the firing of space based weaponry. They are the cumulative deleterious effects in microcircuits due to low rate absorption of ionizing radiation. These cumulative effects are manifest in space electronics by increased leakage currents that often lead to reduction in circuit performance and, ultimately, to a cessation in circuit functionality. These effects are called total ionizing dose (TID) effects. The second class of radiation responses are called single event effects, to include subcategories such as single event upset (SEU), single event transient (SET), and single event dielectric rupture (SEDR). These subcategories define some of the potential consequences within a microcircuit that is subjected to highly energetic singular ions that are prevalent in the natural space environment. After being struck by an ion in a sensitive region of the circuit, the resulting circuit response potentially can be temporal, like a momentary voltage spike on a signal line (SET) that may propagate to a data storage element and corrupts the stored data (SEU). Permanent effects are also possible, like the destruction of the dielectric isolating two charged conducting surfaces following an ion strike that couples the charged plates. For microelectronics to be suitable for the natural space environment given the threats from radiation, they must be hardened to withstand the effects of radiation. That is, radiation hardened electronics are required for space system applications. The next sections assess the total ionizing dose and single event effects hardness targeted for the RHAX250-S.

4A TOTAL IONIZING DOSE TEST RESULTS

RHAX250-S is built using the RH15 process technology within which unique FPGA features have been integrated. The total ionizing dose hardness of RH15 technology is demonstrated by the radiation test results on a 4M SRAM product built using the RH15 process. The 4M SRAM is a dense, complex 150nm circuit design with over 30 million transistors within a circuit area of approximately 13mm by 13mm, much larger than a 250K-gate FPGA. The SRAM standby leakage versus dose response is shown Figure 7. No increase in leakage or degradation in performance was observed in devices under test out to the tested cumulative dose range of 2Mrad(SiO_2) and after a 168-hour post-exposure anneal at 100°C.

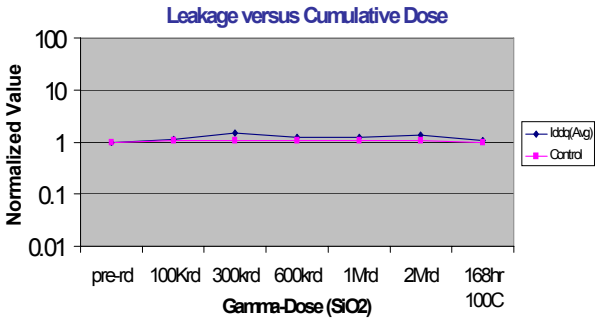

Figure 7. Total Ionizing Dose Test Results.

4B SINGLE EVENT EFFECTS TEST RESULTS

The susceptibility of the antifuse stack to single event dielectric rupture (SEDR) was assessed using energetic ions while changing the angle of incidence to offer a range of effective linear energy transfer (LET) characteristics. The applied voltage to the antifuse stack was varied up to 4.5V during the exposures. The onset of dielectric rupture was assessed by monitoring the antifuse array current as a function of increasing ion fluence. The maximum ion fluence at each applied voltage step was 2M ions/cm^2. An abrupt inflection in the measured current with fluence would signal rupture. The SEDR test data is shown in Figure 8. Rupture was first detected at 4.5V, the top curve. No rupture was observed up to an effective LET of 145 MeV·cm^2/mg with Vdd = 4.2V, demonstrating a very large SEDR hardness margin for the nominal 1.5V antifuse array.

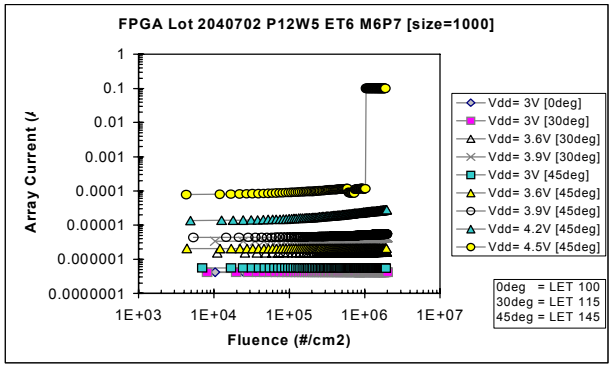

Figure 8. SEDR Radiation Test Results.

The SEU hardness assurance level for RHAX250-S is achieved primarily by design. Figure 9 shows the logic schematic of one hardened user flip-flop [3]. Flip-flops are hardened using the triple modular redundant (TMR) design.

In the hardened flip-flop, both master and slave latch are triple redundantly hardened in an asynchronous manner.

To examine the effectiveness of the SEU hardened design, RTAX FPGA devices were SEU tested using highly energetic ions. The devices were subjected to a variety of ion beams and incident angles to generate a range of effective LETs. Testing was done at room temperature and the parts were biased at their nominal voltages, 3.3V for the I/Os and 1.5V for the core logic. The test results for the hardened user flip-flop are shown in Figure 10. As shown, the flip-flop has a very small cross-section indicating an extremely low SEU rate of <1E-10 errors/bit-day. The data demonstrate that the hardened designs are very effective.

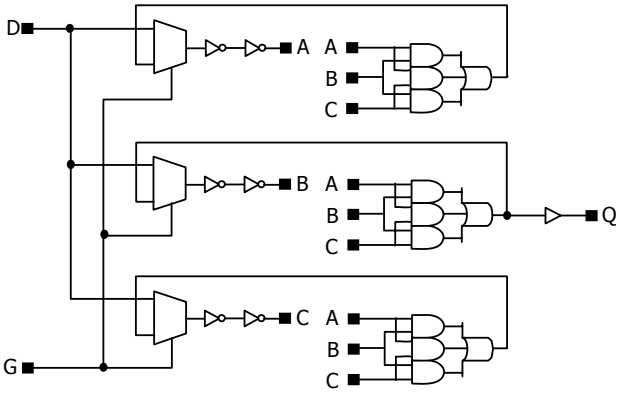

Figure 9. Logic schematic of the triple redundant latch in the SEU hardened user flip-flop [3].

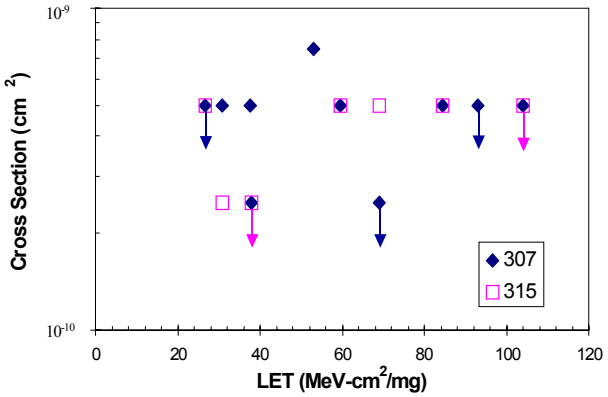

Figure 10. Cross-section per bit versus LET of user flip-flop, using the checkerboard signal pattern clocked at 1 MHz. 307 and 315 are serial numbers of two DUT [3].

Single event transients (SET) were examined using a RTAX FPGA device to configure the logic register string illustrated in Figure 11. The register string consisted of 700 D-flip flops interwoven with eight levels of combinational logic.

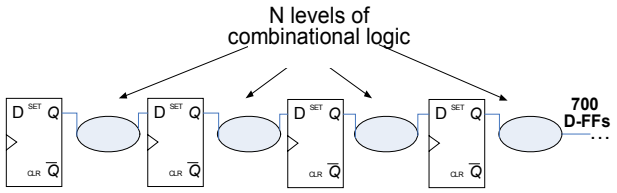

Figure 11. Shift Register String Used for Evaluating SETs.

Figure 12 shows a plot of the SEU cross section (σ_{SEU}) versus effective LET for this register string design, labelled 4F8L. Signal patterns during exposure were checkerboards running at 15, 37.5, 75, and 150 MHz. Data points and Weibull-fitting curves are displayed in the figure.

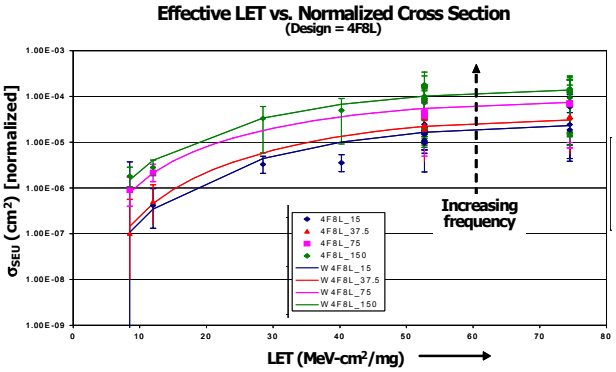

Figure 12. SET Radiation Test Results.

The predicted SEU rates in upsets/bit/day at the four signal frequencies in the radiation environment of GEO-min and 100-mil of Al shielding are provided in Table 4.

Table 4. SEU Rates vs. Signal Frequencies.

Signal Freq.	15 MHz	37.5 MHz	75 MHz	150 MHz
Upset Rates	5.31E-9	7.88E-9	3.75E-8	8.17E-8

As expected the SEU rate worsens with signal frequency but nonetheless the upset rates indicate adequate hardness margin.

5. SUMMARY

BAE Systems and Actel Corporation are continuing their long successful collaboration, producing a 150nm radiation-hardened 250K gate antifuse-based FPGA for space applications, RHAX250-S. This product will provide the much needed radiation hardened, single-chip, nonvolatile FPGA solution for mission-critical aerospace and military systems. The antifuse process has been successfully integrated into the base rad hard 150nm CMOS technology (RH15). Total ionizing dose radiation data on RH15 demonstrates mega-rad hardness. Single event effects tests have shown the FPGA design to have adequate hardness margin against a variety of heavy ion threats. A full suite of comprehensive radiation and reliability tests is planned as part of rad hard FPGA product demonstration and qualification activities. The overall RHAX250-S product installation and qualification efforts are progressing well toward completion in 2007.

ACKNOWLEDGEMENTS

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BIOGRAPHIES

Leonard Rockett *is the manager of the microelectronics business area at BAE Systems in Manassas VA. He has over 30 years of both engineering and management experience primarily in the areas of radiation hardened technology development and microcircuit design. He has authored or co-authored over 50 published technical reports and papers. He currently holds 15 U.S. patents plus he has other patents pending. He earned his B.S. degree in electrical engineering from Howard University in Washington DC, and his M.S. and Ph.D. degrees in electrical engineering with a specialization in microelectronics from Columbia University in the City of New York. Dr. Rockett is a Senior Member of the IEEE.*

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Steven Danziger *is the semiconductor technology diversification Program Manager with BAE Systems. He is the program manager for the RHAX250-S installation and qualification program. He earned a B.S. in Physics from Queens College City University of New York and a M.S. in Physics from The Pennsylvania State University. He has over 23 years of experience as an engineer and a manager in semiconductor development and production for various defense and commercial semiconductor*

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Brian Cronquist: *is Senior Director Technology Development at Actel Corp. Mr. Cronquist graduated cum laude (Chemistry Medal) in Chemistry from the University of Santa Clara. He manages new process/materials/device and radiation effects development and wafer foundry relationships for the anti-fuse and Flash products. He has published or co-published over 20 technical papers, many in the field of radiation effects and hardening.*

Jih Jong Wang *is a Senior Principal Radiation Effects Scientist at Actel Corp. He received a PhD. degree in Material Science and Engineering from Case Western Reserve University. At Actel, he has been involved all the radiation related projects and products. Dr. Wang has presented and published over 30 times on the subject of radiation effects on semiconductor microelectronics in various conferences and journals.*