**01. Interface to the processor and memory via the system bus or central switch and interface to one or more peripheral devices by tailored data links are two major functions of an \_\_\_\_\_\_\_\_\_\_\_\_\_.**

I/O module

**02. An external device connected to an I/O module is often referred to as a \_\_\_\_\_\_\_\_\_\_ device.**

peripheral

**03. We can broadly classify external devices into three categories: human readable, communication, and \_\_\_\_\_\_\_\_\_\_.**

machine readable

**04. The U.S. national version of the International Reference Alphabet is referred to as \_\_\_\_\_\_\_\_\_\_.**

ASCII

**05. The categories for the major functions or requirements for an I/O module are: control and timing, device communication, data buffering, error detection, and \_\_\_\_\_\_\_\_\_.**

processor communication

**06. In \_\_\_\_\_\_\_\_\_\_ mode the I/O module and main memory exchange data directly, without processor involvement.**

direct memory access (DMA)

**07. There are four types of I/O commands that an I/O module may receive when it is addressed by a processor: control, test, write, and \_\_\_\_\_\_\_\_\_.**

read

**08. When the processor, main memory, and I/O share a common bus, two modes of addressing are possible: memory mapped and \_\_\_\_\_\_\_\_.**

isolated

**09. The \_\_\_\_\_\_\_\_ is a single-chip, general-purpose I/O module designed for use with the Intel 80386 processor.**

82C55A

**10. A \_\_\_\_\_\_\_\_ controls multiple high-speed devices and, at any one time, is dedicated to the transfer of data with one of those devices.**

selector channel

**11. In a \_\_\_\_\_\_\_\_\_ interface there are multiple lines connecting the I/O module and the peripheral and multiple bits are transferred simultaneously.**

parallel

**12. In a \_\_\_\_\_\_\_\_ interface there is only one line used to transmit data and bits must be transmitted one at a time.**

serial