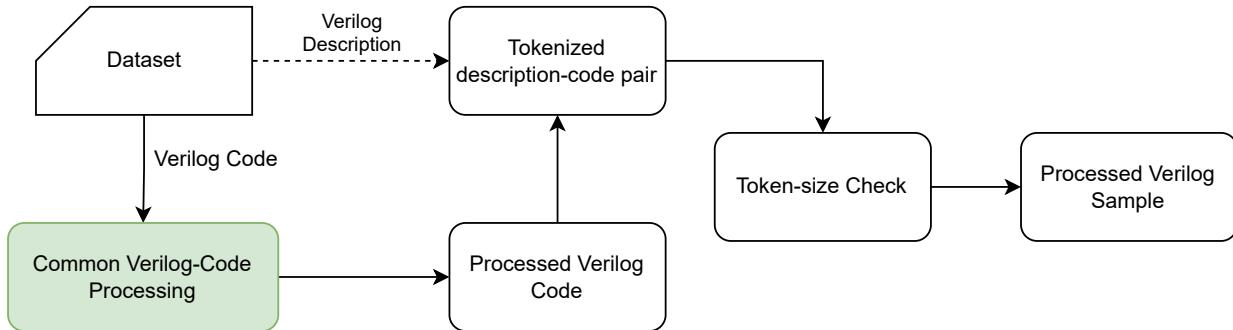
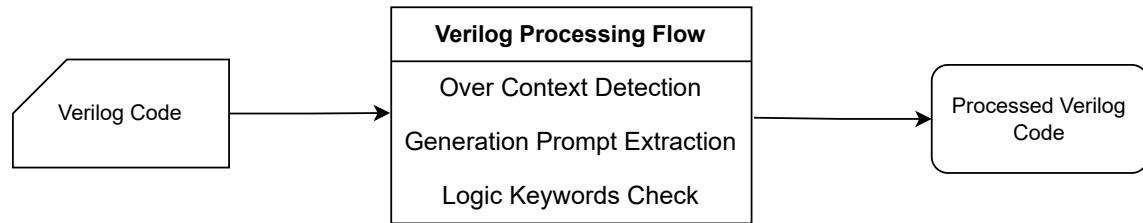


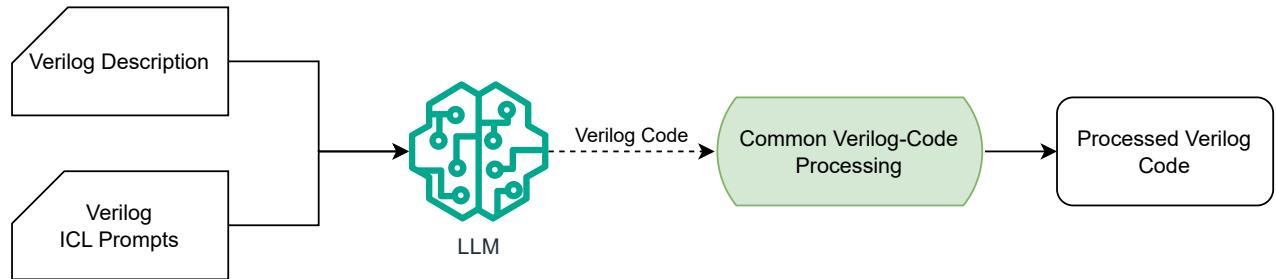
Dataset preprocessing



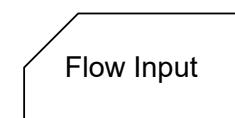
Common Verilog-Code Processing



Inference



Flow Annotations



Data path
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