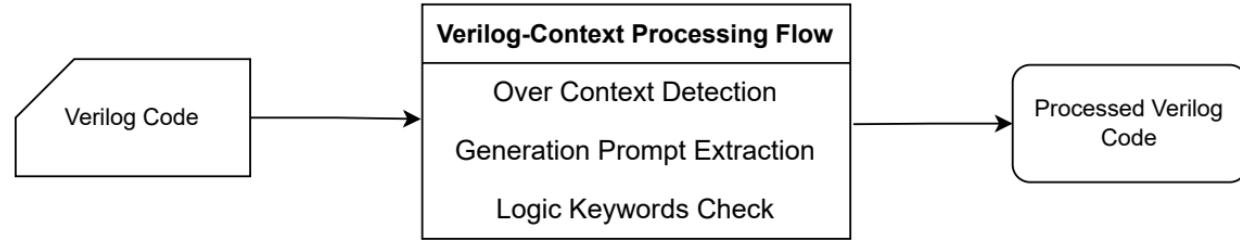
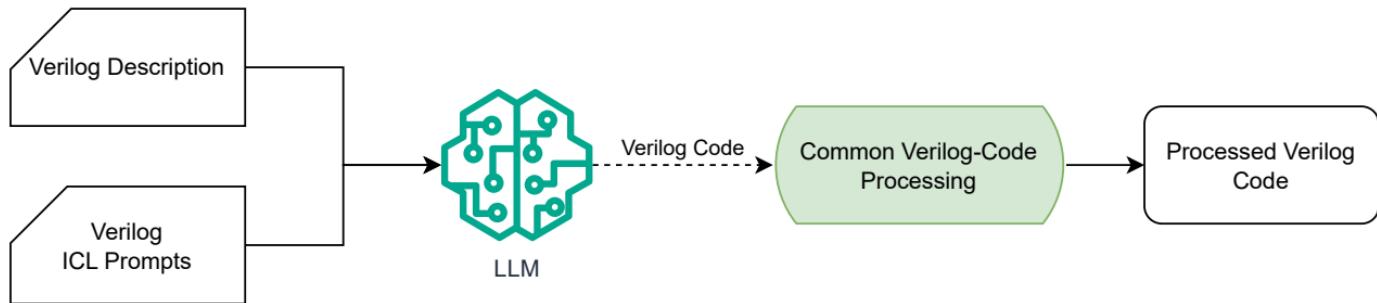


Common Verilog-Code Processing



Inference



Flow Annotations

