Digital Logic Design

Final Project

Due Date: 99/10/26

1- Implement the Boolean function below using transistor-level Verilog coding.

$$f(A,B,C,D) = ADC + AB'C + BD' + A'C'D'$$

In your testbench, test the module for all different combinations of inputs. (50 points)

2- Implement an 8-bit signed adder using gate-level Verilog coding. The adder should have an overflow detector.
In your testbench, test it for different inputs (once with two positive numbers without overflow, once with two positive numbers with overflow, once with two negative numbers without overflow, and once with two negative numbers with overflow). (50 points)

3- Implement an ALU with two 8 bit signed inputs A and B and with 4 different operation modes mentioned below. (100 points)

0- $(A \ <<< \ 2) \ + \ (B \ >>> \ 2)$

1- $A + 2B$

2- $-B$

3- $|3A - B|$

Each of the four operations should be implemented in a distinct module using dataflow coding. Then in a top module file, the modules should be connected to each other in a proper way. The final output should also be coded using dataflow.
(Note: "<<<" and ">>>" mean arithmetic shift to left and arithmetic shift to right, respectively.)

4- Implement a 32 bit carry-lookahead-adder (CLA). First design a Full-adder module using behavioral coding. Use that FA module to make the CLA. Use another module to calculate Carry. (This problem is optional and has extra points) (150 points)

Good Luck!
Mosayebi
Do not hesitate to ask your question
Via eeXBee@gmail.com

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Note 1: You should at least provide two Verilog files for each question: one for the module, and one for the testbench. There should be enough test cases in your testbenches to test modules for different input and output values.

Note 2: This project must be done individually; thus, in case of any similarities between the codes provided by the students, all of those will receive a "-50".

Note 3: Upload your codes as one zip file. Each question must be placed in a separate folder inside the zip file.

Note 4: Please name your files as below:

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.v

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.Testbench.v

Example: Cruise.Tom.98777777.Main.Testbench.v

Note 5: Provide a report in pdf format alongside with project files. Report should be at least 3 pages, proving that your design actually works. It should contain schematics, several screenshots from simulation waves and your descriptions.

Good Luck!

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