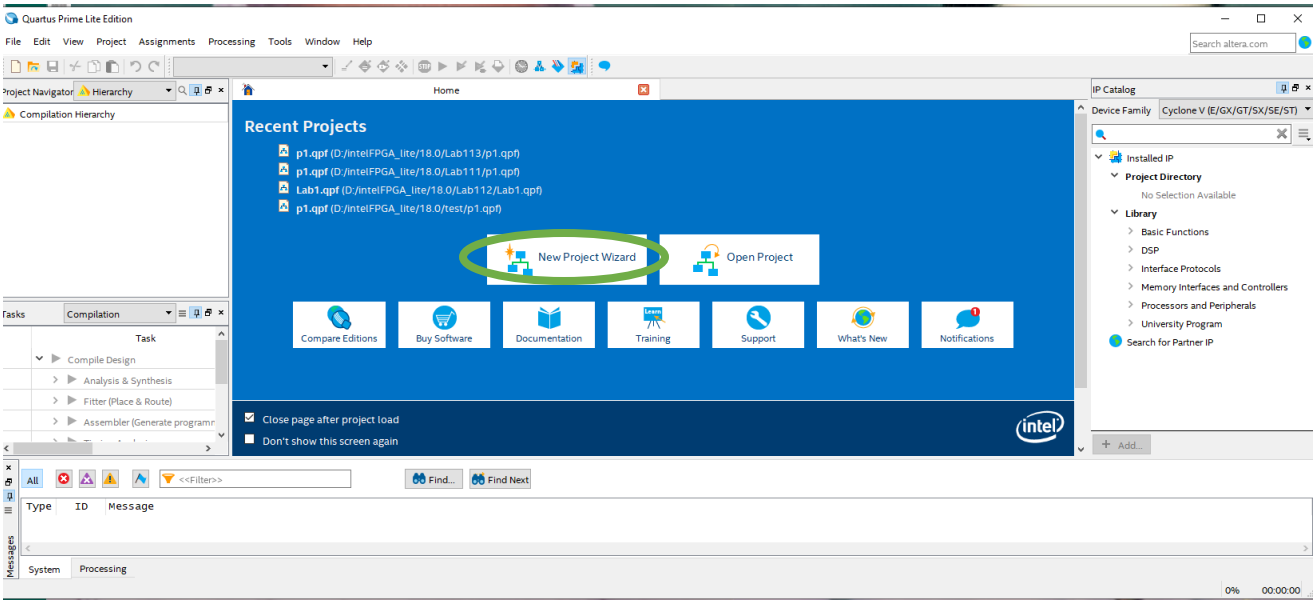
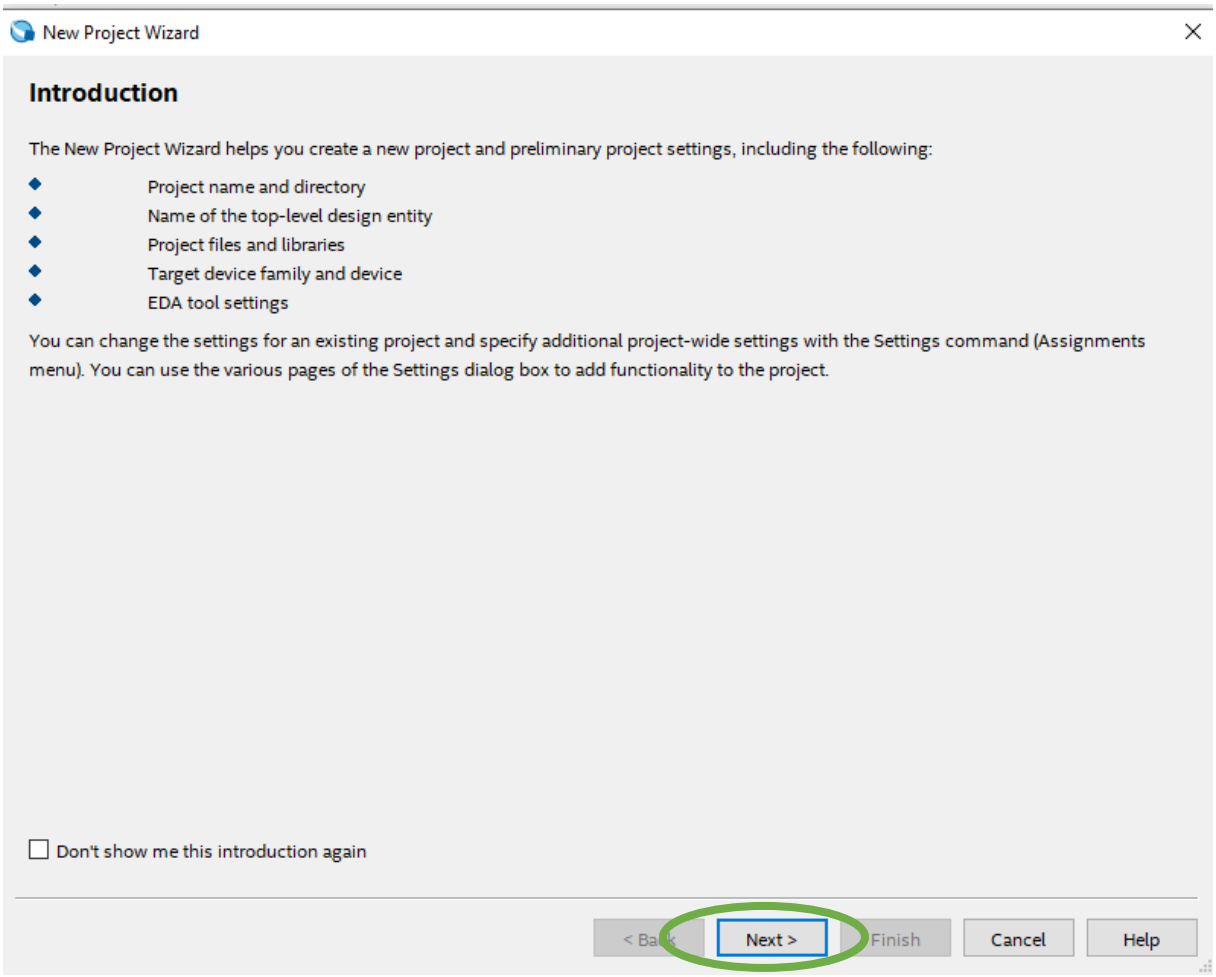
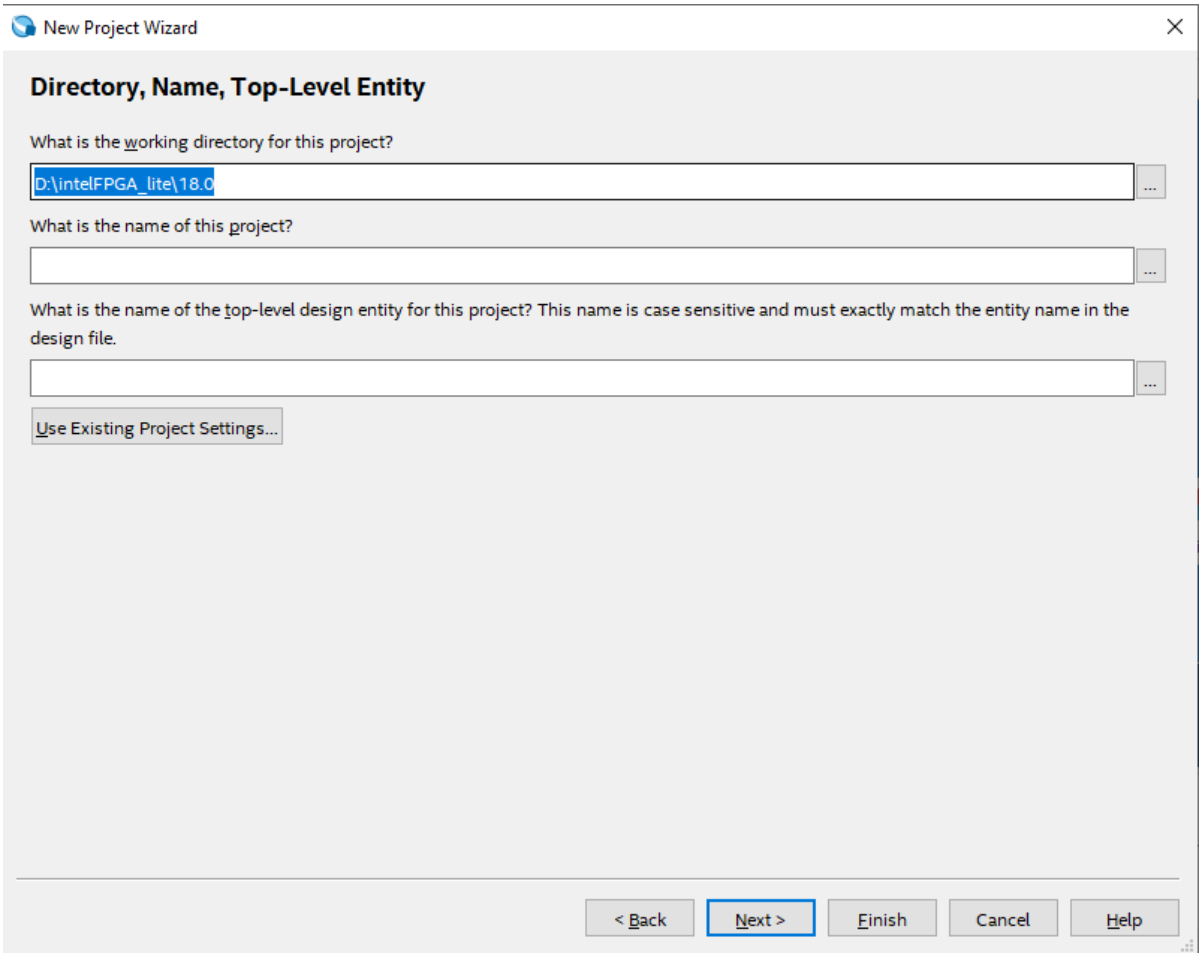


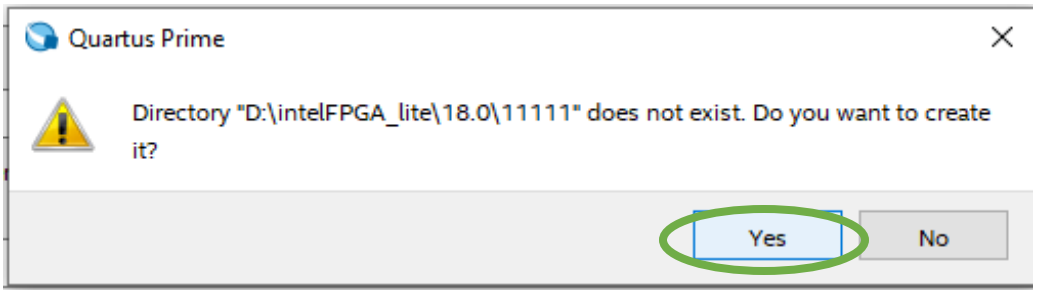
Select New Project Wizard



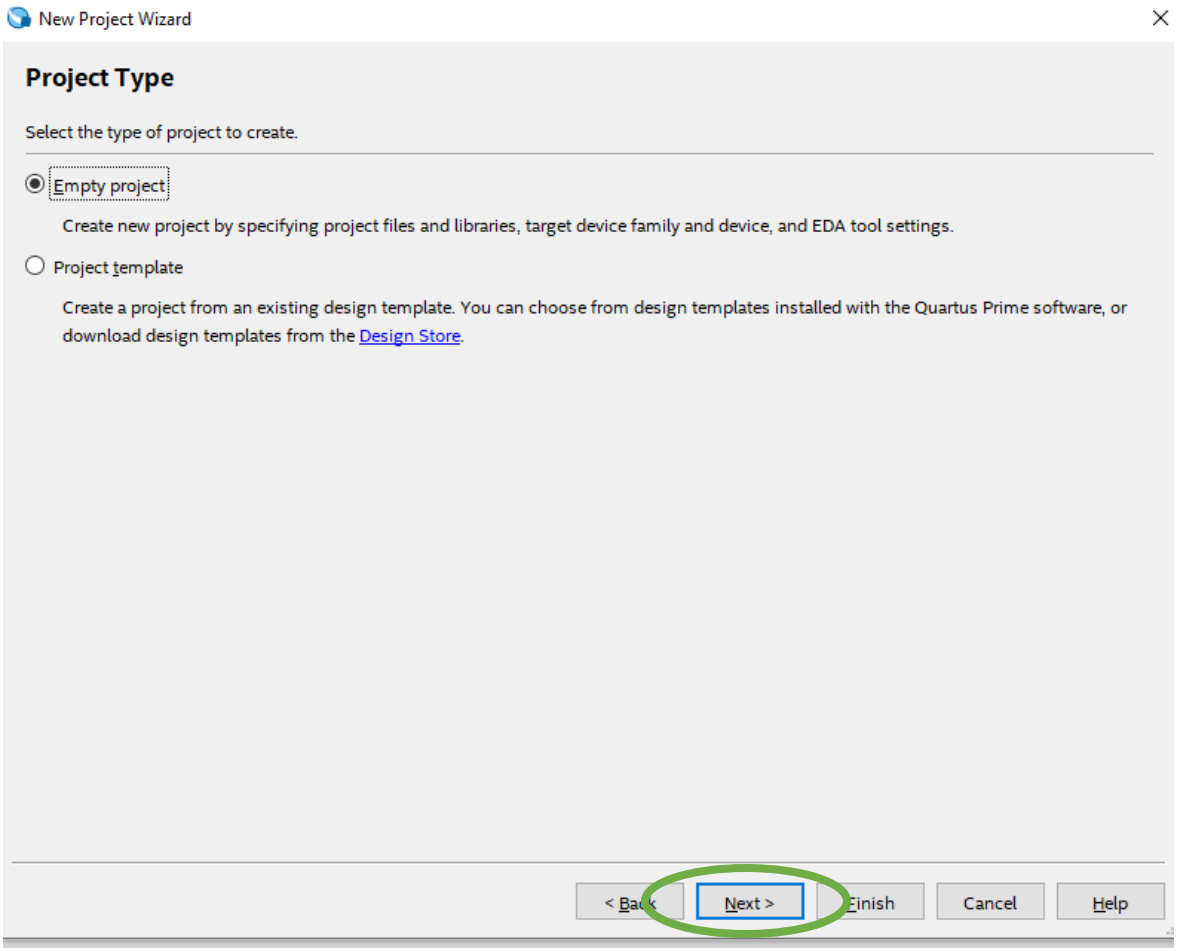


Make sure not to change the default directory. You can add the folder to it by adding “\foldername”

Later give the project a name



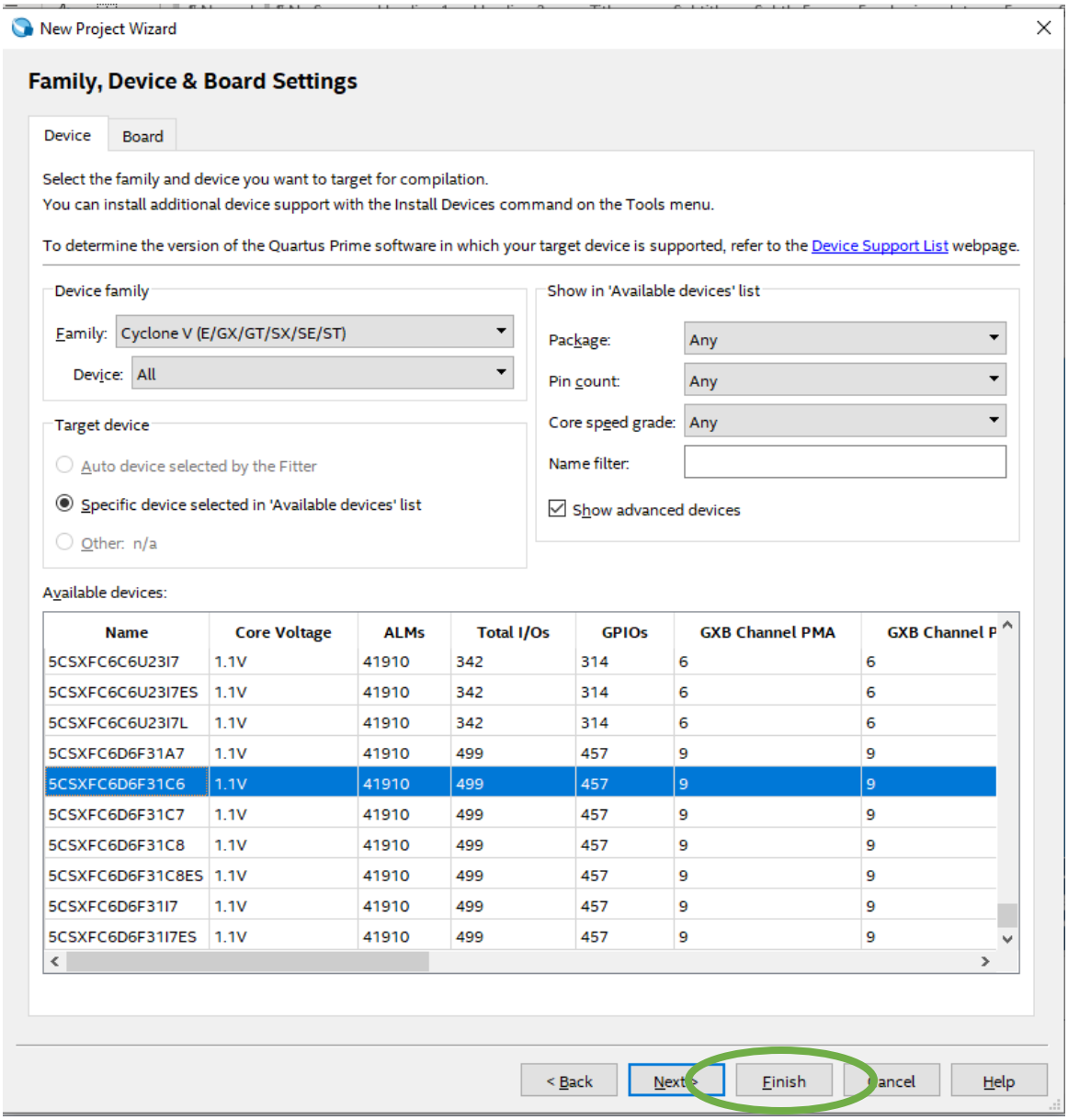
It might give you a prompt click Yes.

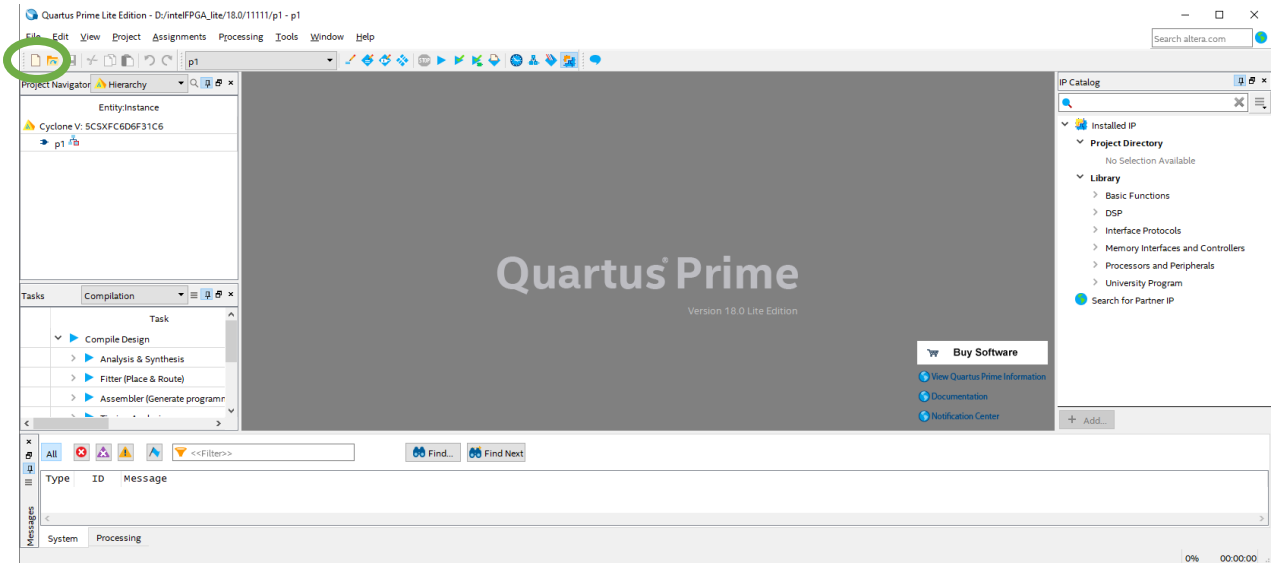


Hit next in the following screen as well

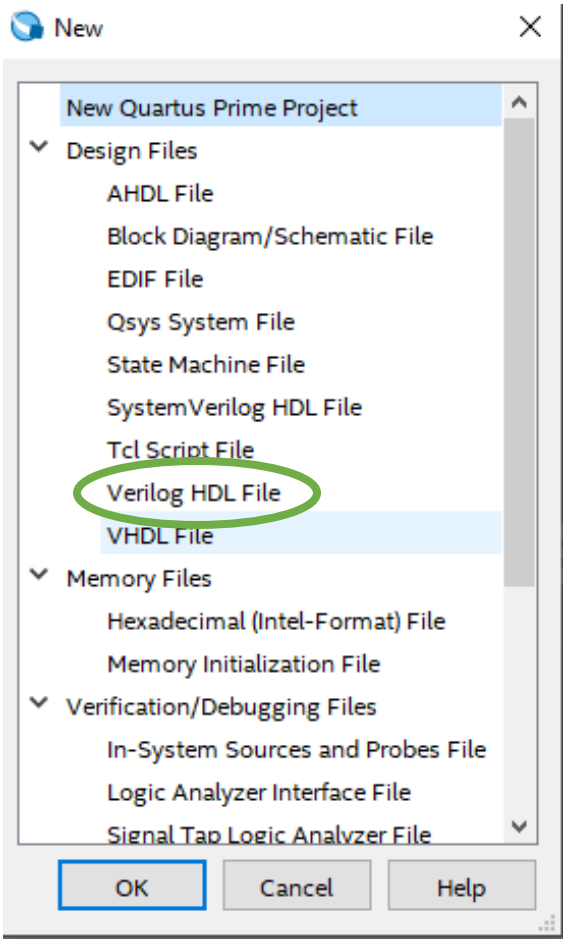
On the next screen you can drag the edges (top and bottom) to make it bigger.

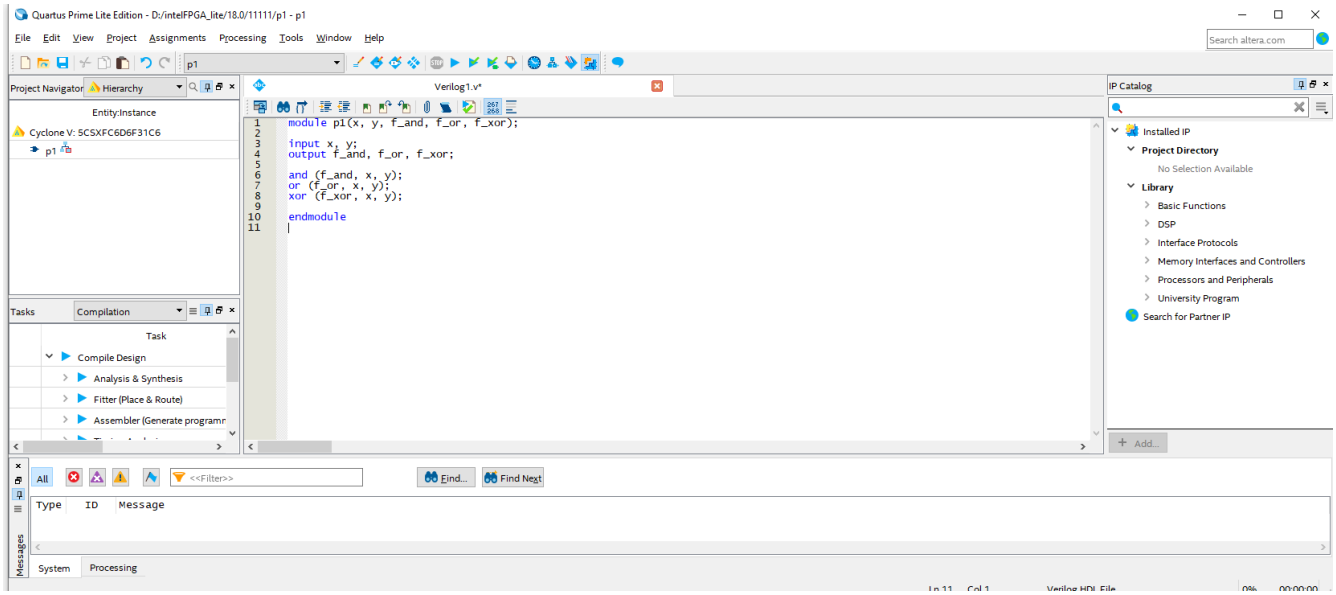
Select the device that is 6th from the last named 5CSXFC6D6F31C6


New Project Wizard
Family, Device & Board Settings
Device
Board
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported, refer to the Device Support List webpage.
Device family
Family: Cyclone V (E/GX/GT/SX/SE/ST)
Device: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Core speed grade: Any
Name filter:
Show advanced devices
Available devices:
Name | Core Voltage | ALMs | Total I/Os | GPIOs | GXB Channel PMA | GXB Channel P
5CSXFC6C6U23I7 | 1.1V | 41910 | 342 | 314 | 6 | 6
5CSXFC6C6U23I7ES | 1.1V | 41910 | 342 | 314 | 6 | 6
5CSXFC6C6U23I7L | 1.1V | 41910 | 342 | 314 | 6 | 6
5CSXFC6D6F31A7 | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31C6 | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31C7 | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31C8 | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31C8ES | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31I7 | 1.1V | 41910 | 499 | 457 | 9 | 9
5CSXFC6D6F31I7ES | 1.1V | 41910 | 499 | 457 | 9 | 9
< Back
Next >
Finish
Cancel
Help



Select the first icon or press “ctrl + N”





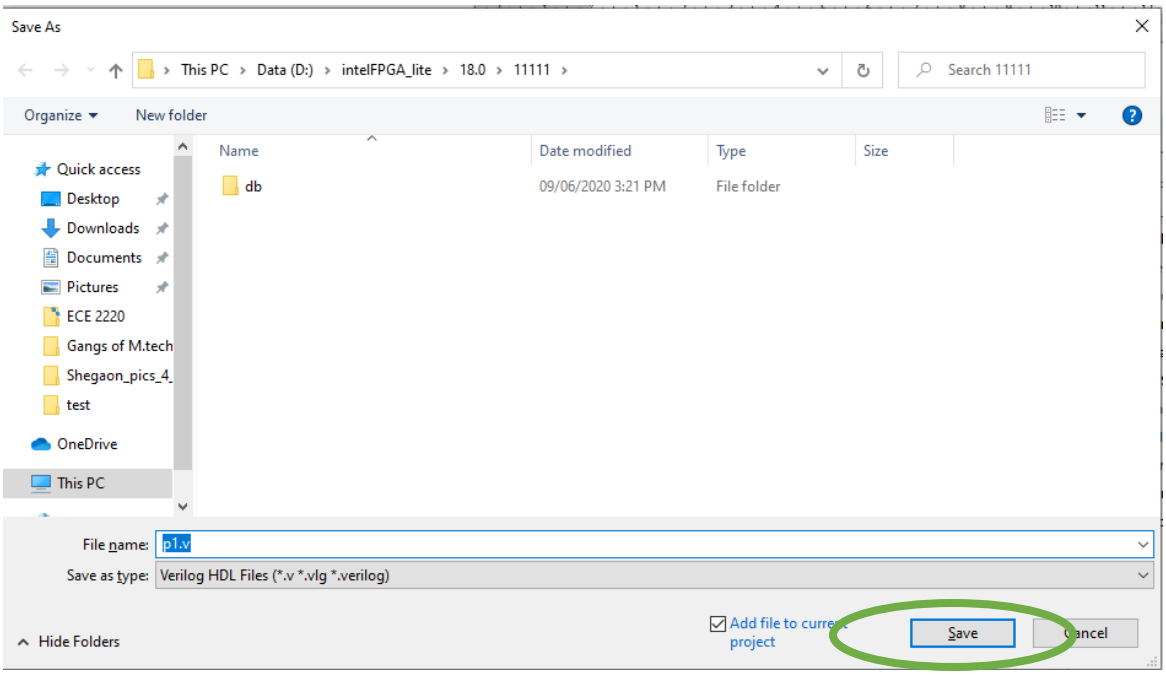
Write your code in this newly opened Verilog file and save it.

Make sure to have the main module name same as the project name.

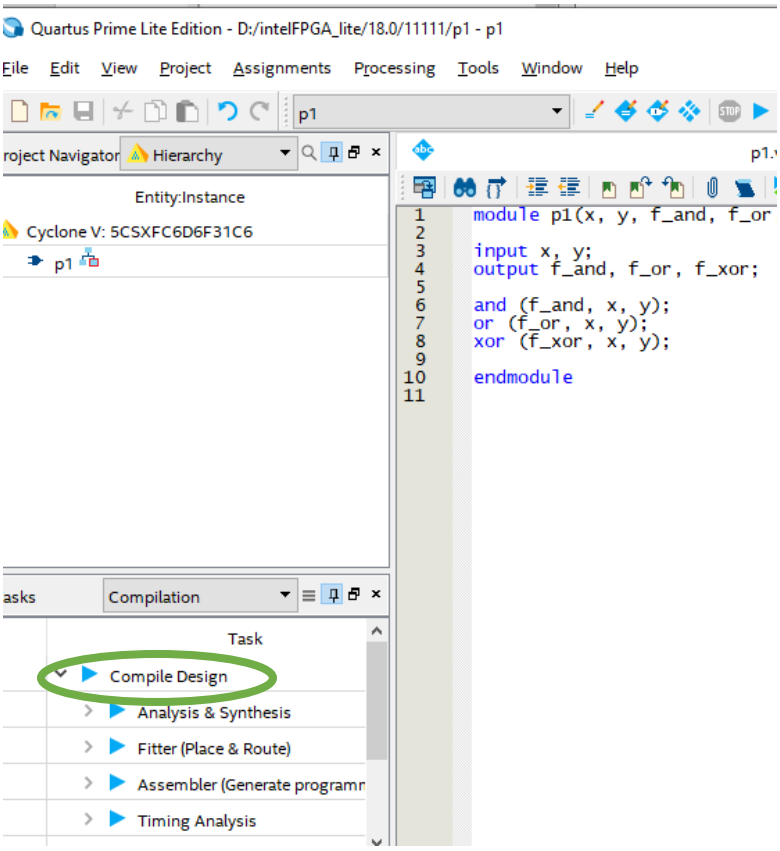
When you save this file make sure the file name is also same as the main module name and the project name.

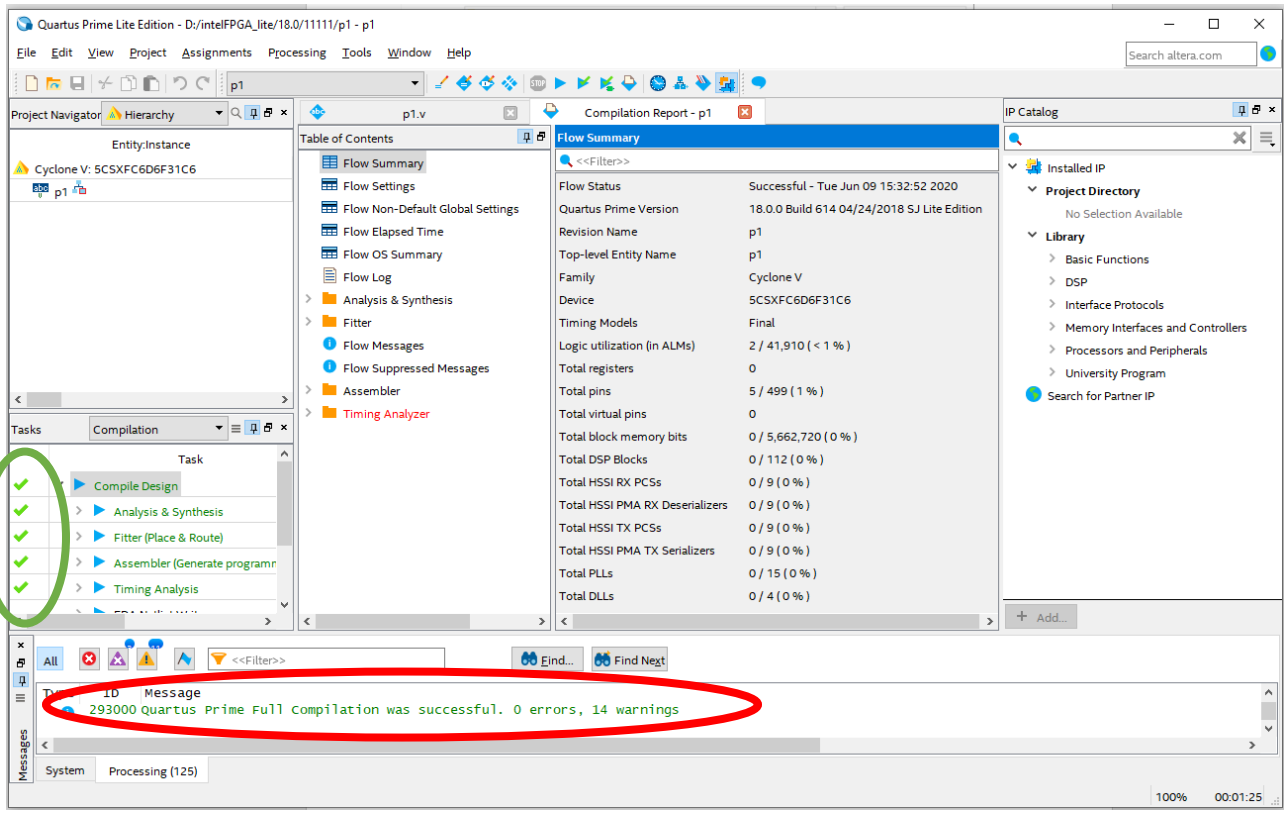
For the case in example project name is p1. So the module and file name are going to be p1 and p1.v respectively.

Also make sure you're not changing the project directory.



Double click on compile design

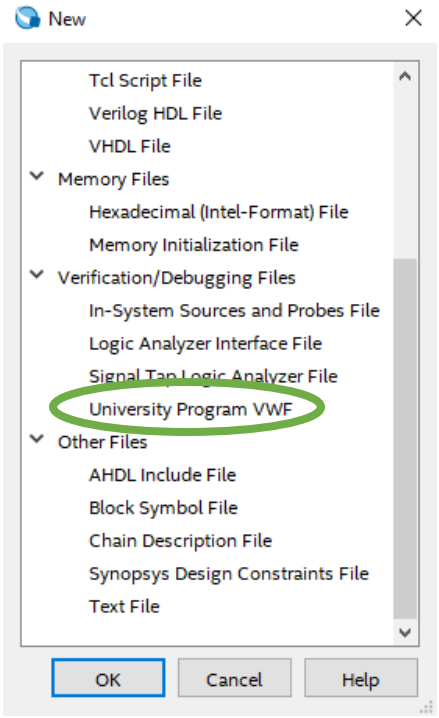


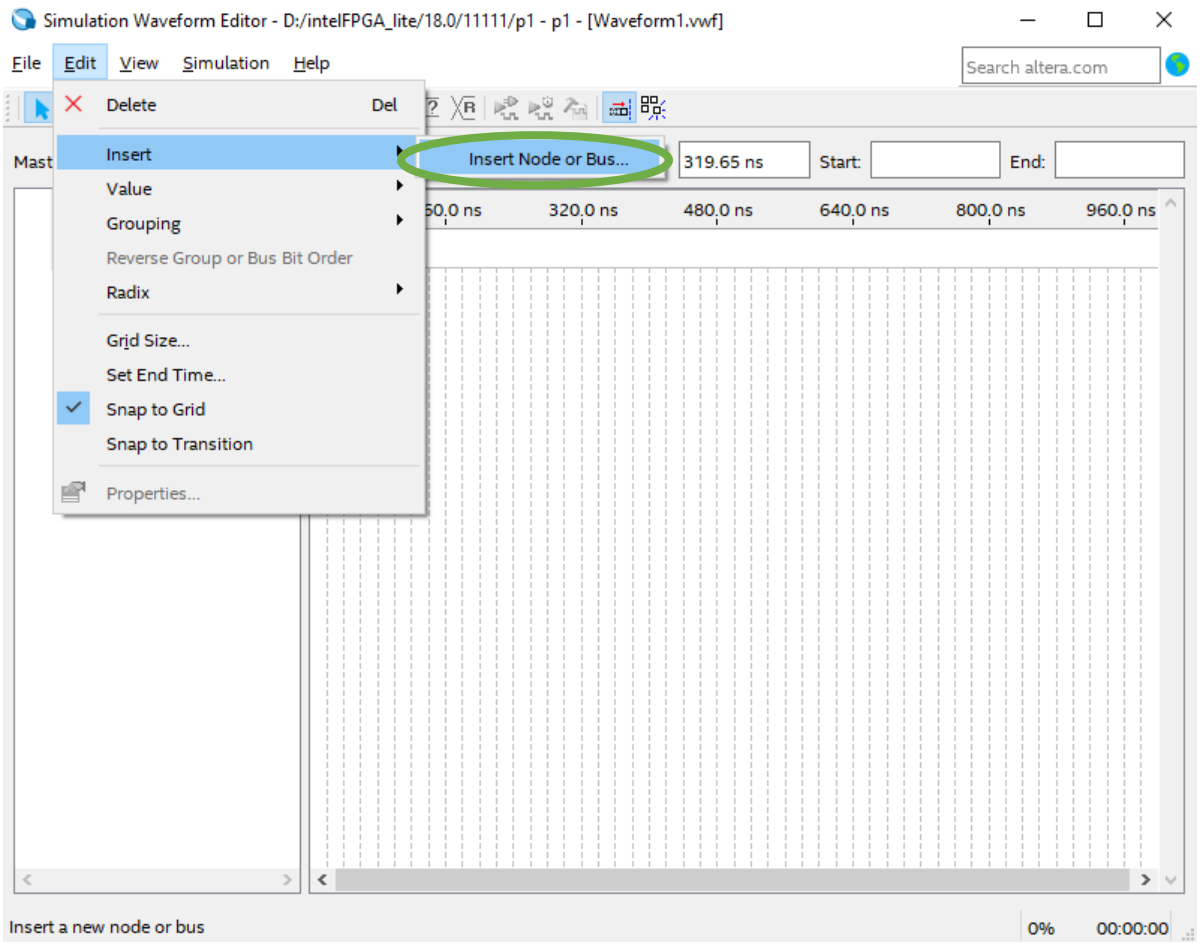


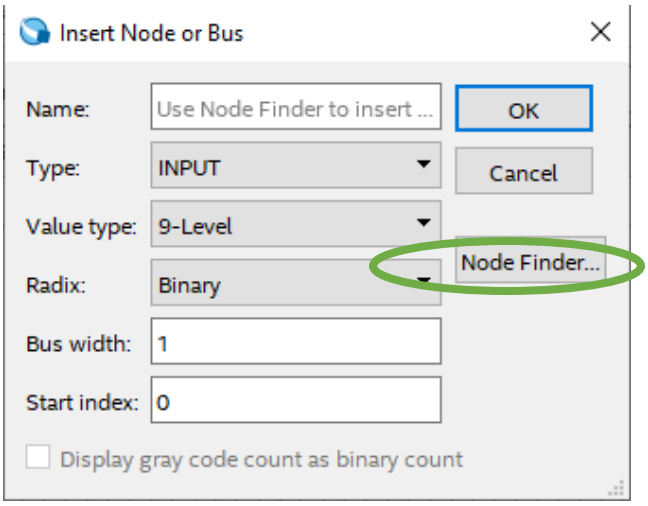
You should see 5 green ticks.

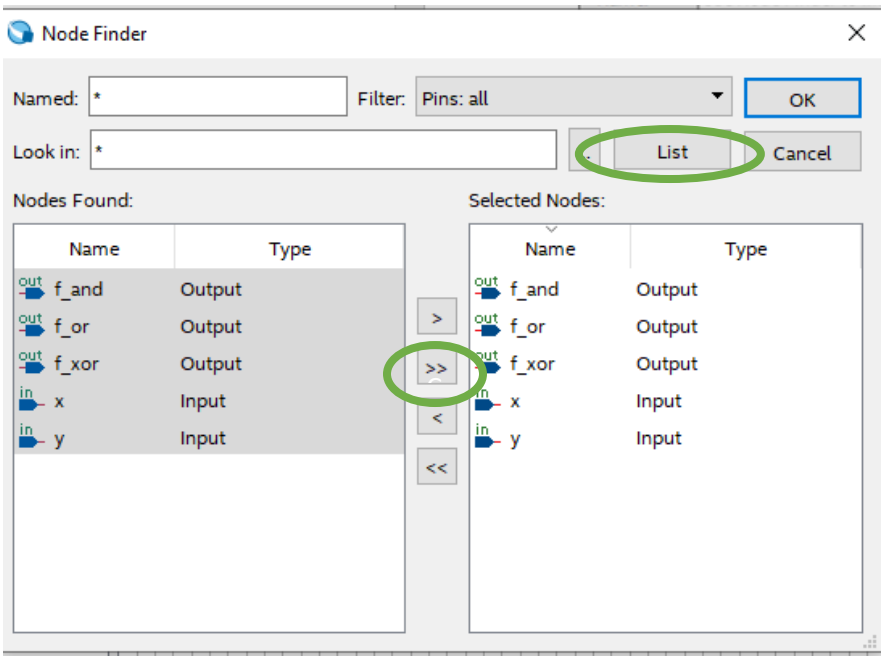
If not, then there are some syntax errors and can be looked for in the area outlined in red.

Again press “ctrl + N” to have the waveform analysis


New
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
Signal Tap Logic Analyzer File
University Program VWF
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel
Help


Simulation Waveform Editor - D:/intelFPGA_lite/18.0/11111/p1 - p1 - [Waveform1.vwf]
File
Edit
View
Simulation
Help
Search altera.com
Delete
Del
Insert
Value
Grouping
Reverse Group or Bus Bit Order
Radix
Grid Size...
Set End Time...
Snap to Grid
Snap to Transition
Properties...
Insert Node or Bus...
319.65 ns
Start:
End:
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Insert a new node or bus
0%
00:00:00

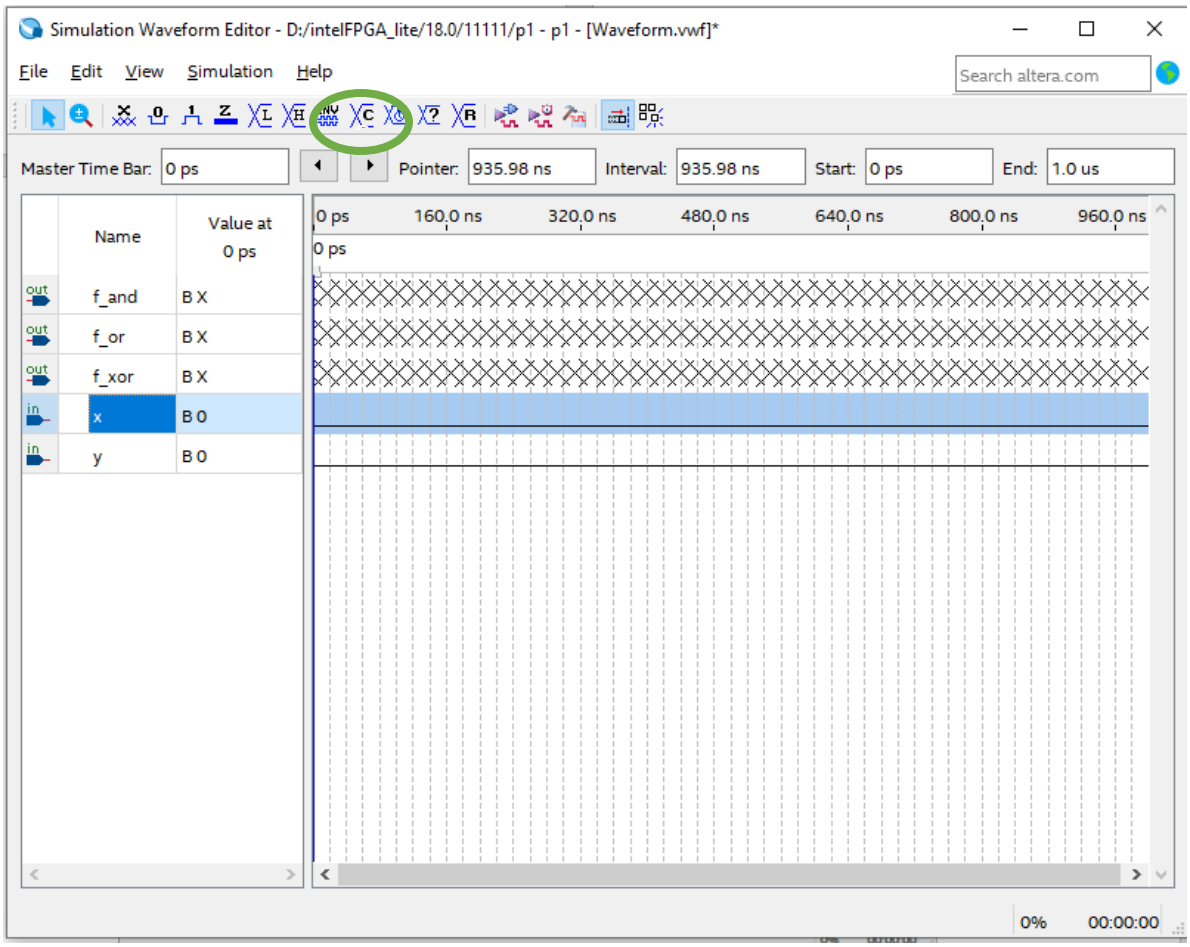




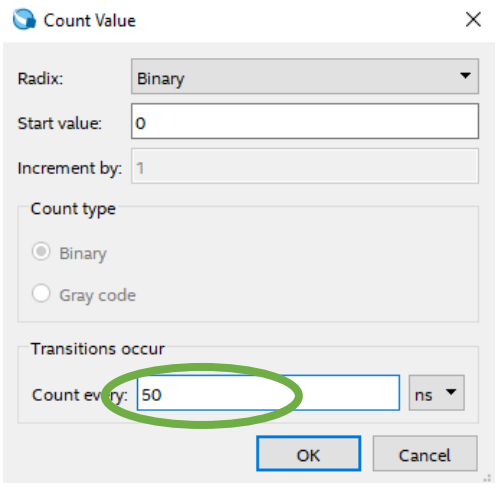
Hit the List button and then the >> button.

Later click OK for this window and the window that appears after this.

You can see the inputs and outputs in the window like this.

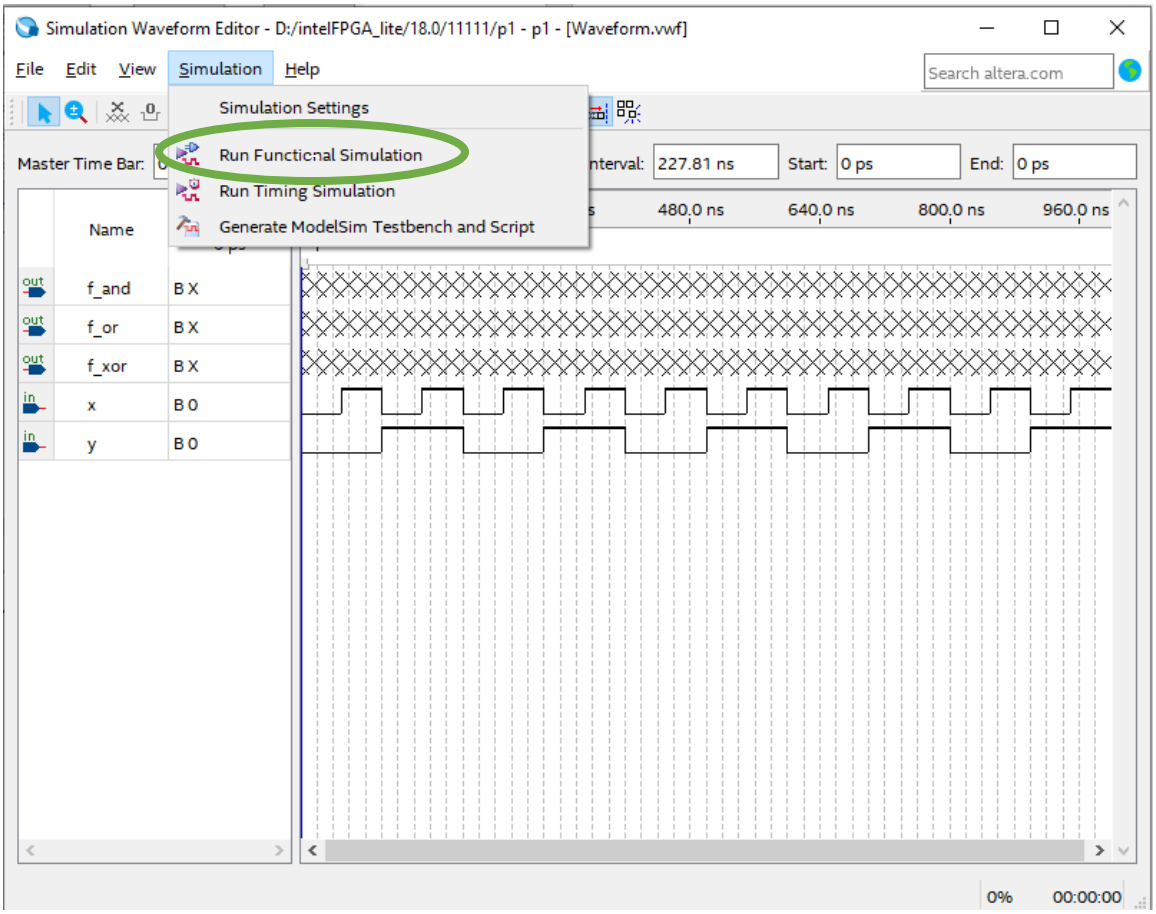


Select any input and click the “count value” button

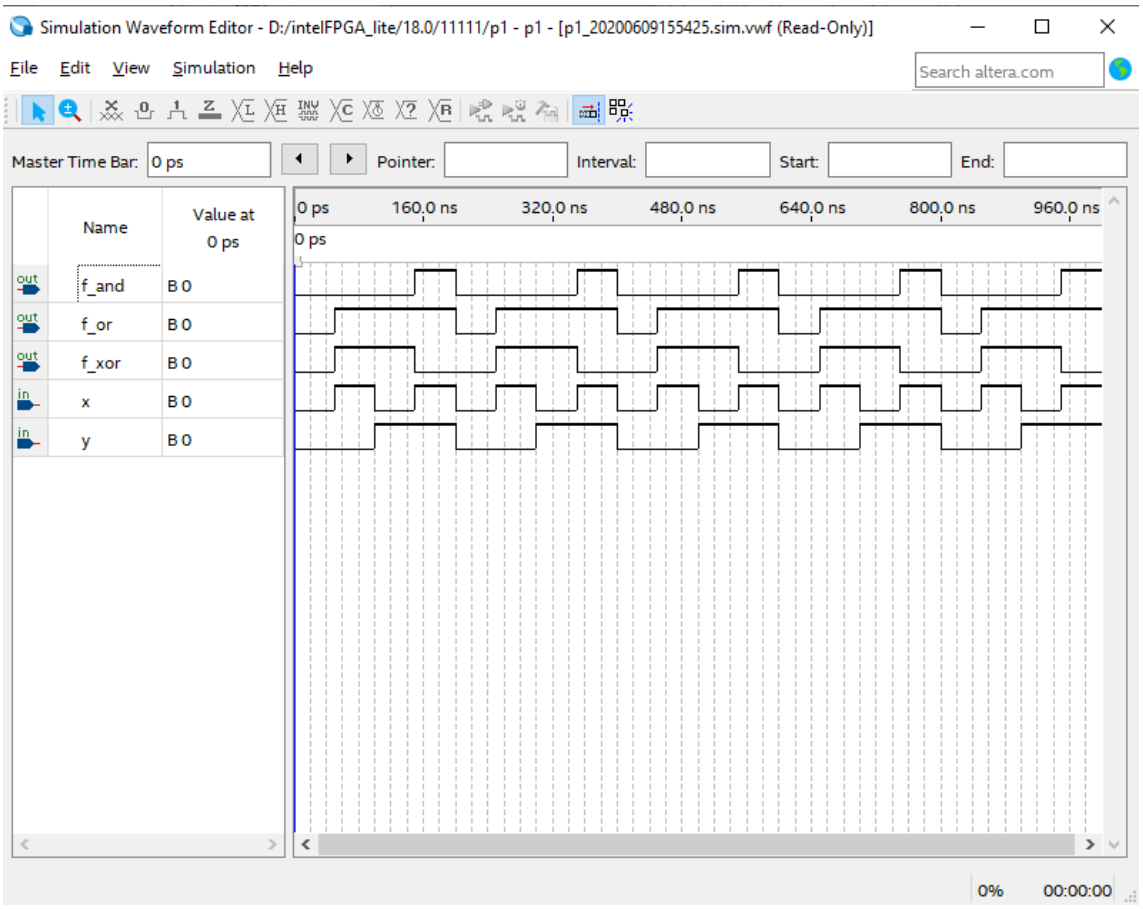


Give it a value and hit OK. Do the same for all other inputs.

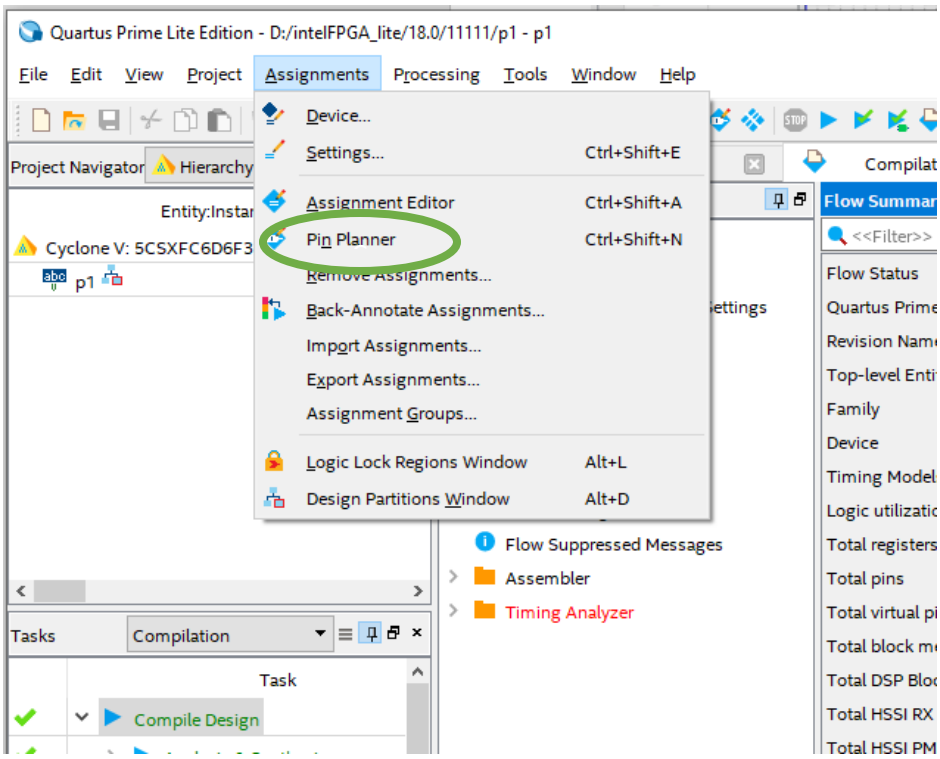
After that save it and make sure **not** to change the file name or the directory. Default name will be waverorm.vwf

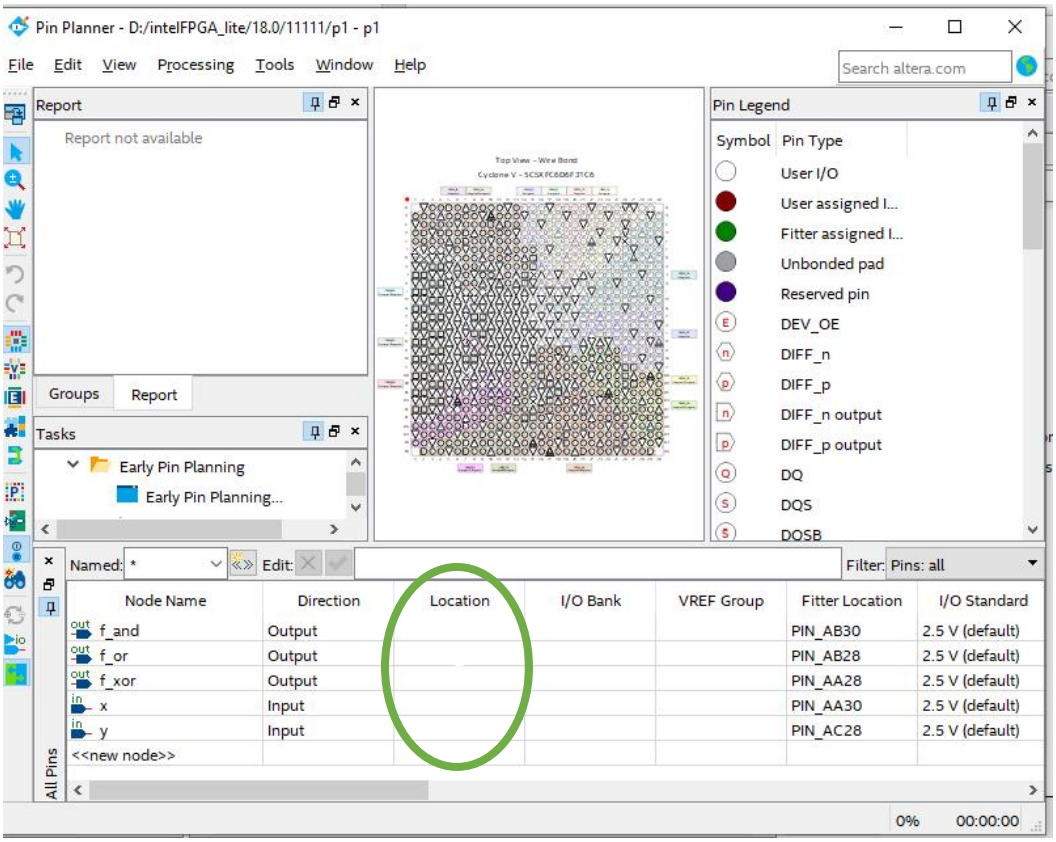


Hit “Run Functional Simulation” and it should simulate and assign values to all the outputs in a new window.

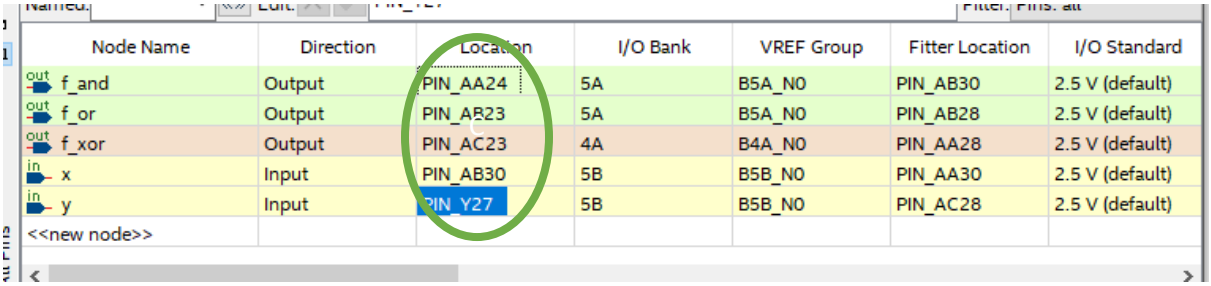


To program the DE-10 board, need to do the pin assignments. Keep the pin assignment sheet ready.


Quartus Prime Lite Edition - D:/intelFPGA_lite/18.0/11111/p1 - p1
File Edit View Project Assignments Processing Tools Window Help
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
Logic Lock Regions Window Alt+L
Design Partitions Window Alt+D
Project Navigator Hierarchy
Cyclone V: 5CSXFC6D6F3
p1
Flow Suppressed Messages
Assembler
Timing Analyzer
Flow Summar
Flow Status
Quartus Prime
Revision Nam
Top-level Enti
Family
Device
Timing Model
Logic utilizatio
Total registers
Total pins
Total virtual pi
Total block m
Total DSP Bloc
Total HSSI RX
Total HSSI PM
Tasks Compilation
Task
Compile Design

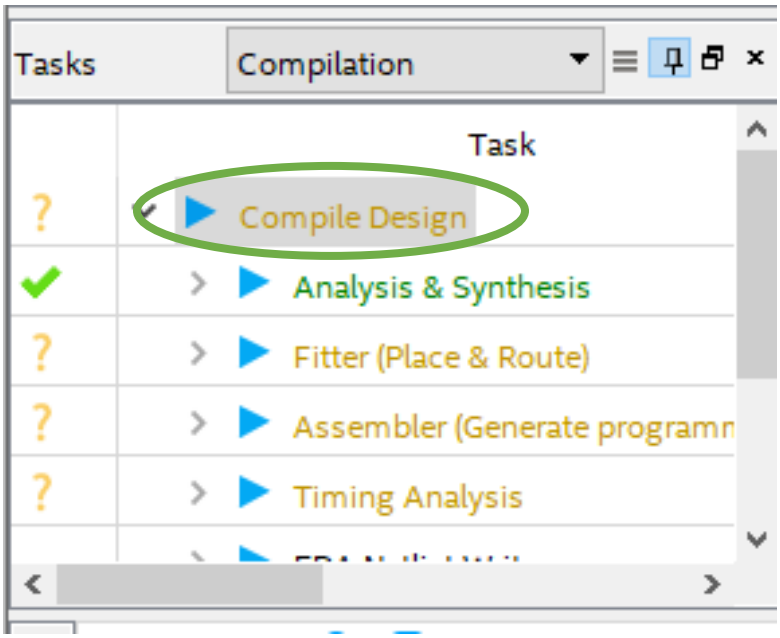

Pin Planner - D:/intelFPGA_lite/18.0/11111/p1 - p1
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Pin Legend
Symbol Pin Type
User I/O
User assigned I...
Fitter assigned I...
Unbonded pad
Reserved pin
DEV_OE
DIFF_n
DIFF_p
DIFF_n output
DIFF_p output
DQ
DQS
DQSB
Named: *
Edit:
Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
f_and Output PIN_AB30 2.5 V (default)
f_or Output PIN_AB28 2.5 V (default)
f_xor Output PIN_AA28 2.5 V (default)
x Input PIN_AA30 2.5 V (default)
y Input PIN_AC28 2.5 V (default)
<<new node>>
All Pins
0% 00:00:00

Assign the addresses from the pin assignment sheet in this column.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
f_and	Output	PIN_AA24	5A	B5A_N0	PIN_AB30	2.5 V (default)
f_or	Output	PIN_AB23	5A	B5A_N0	PIN_AB28	2.5 V (default)
f_xor	Output	PIN_AC23	4A	B4A_N0	PIN_AA28	2.5 V (default)
x	Input	PIN_AB30	5B	B5B_N0	PIN_AA30	2.5 V (default)
y	Input	PIN_Y27	5B	B5B_N0	PIN_AC28	2.5 V (default)
<<new node>>						

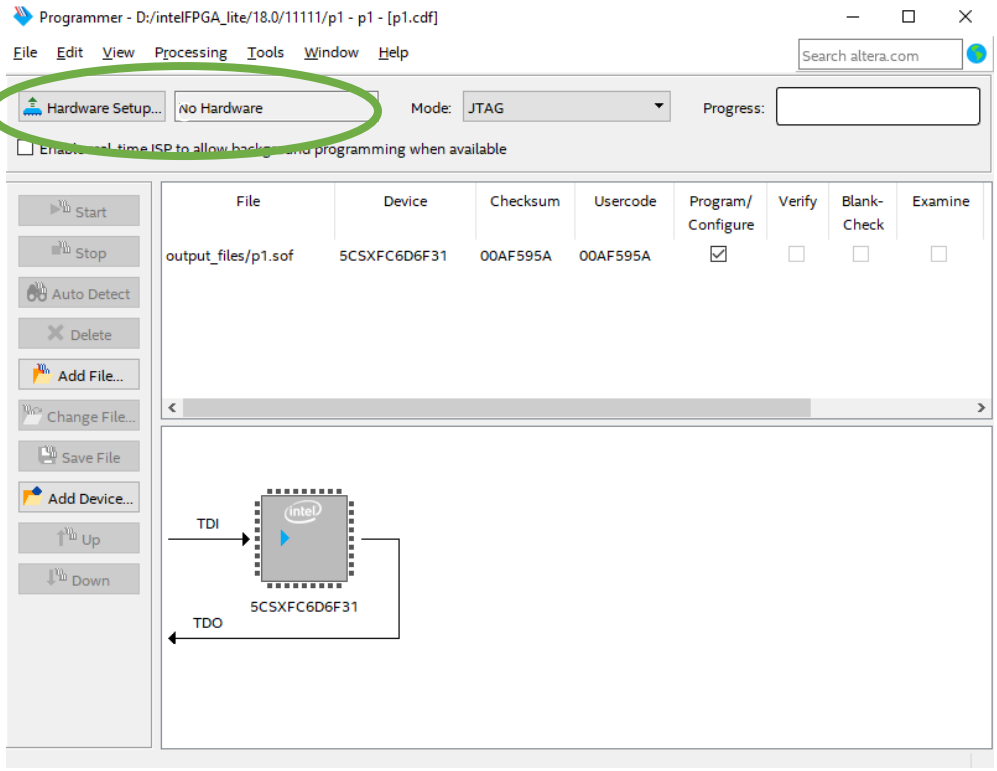
Once this is done, close this window and compile the design again.



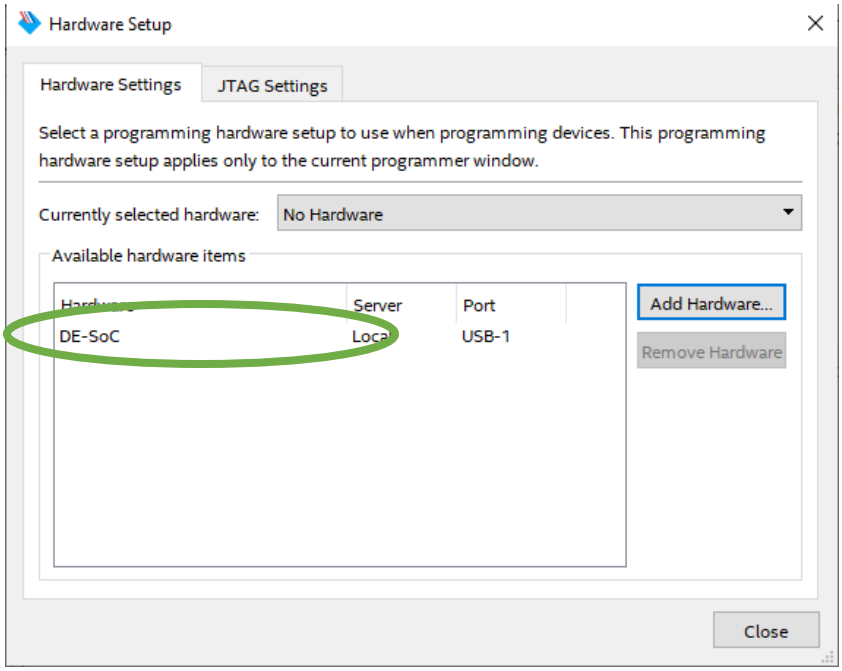
Once you compile the design all these should turn to green ticks.

Once this is done click on “Program Device” slightly below the Compile design option.

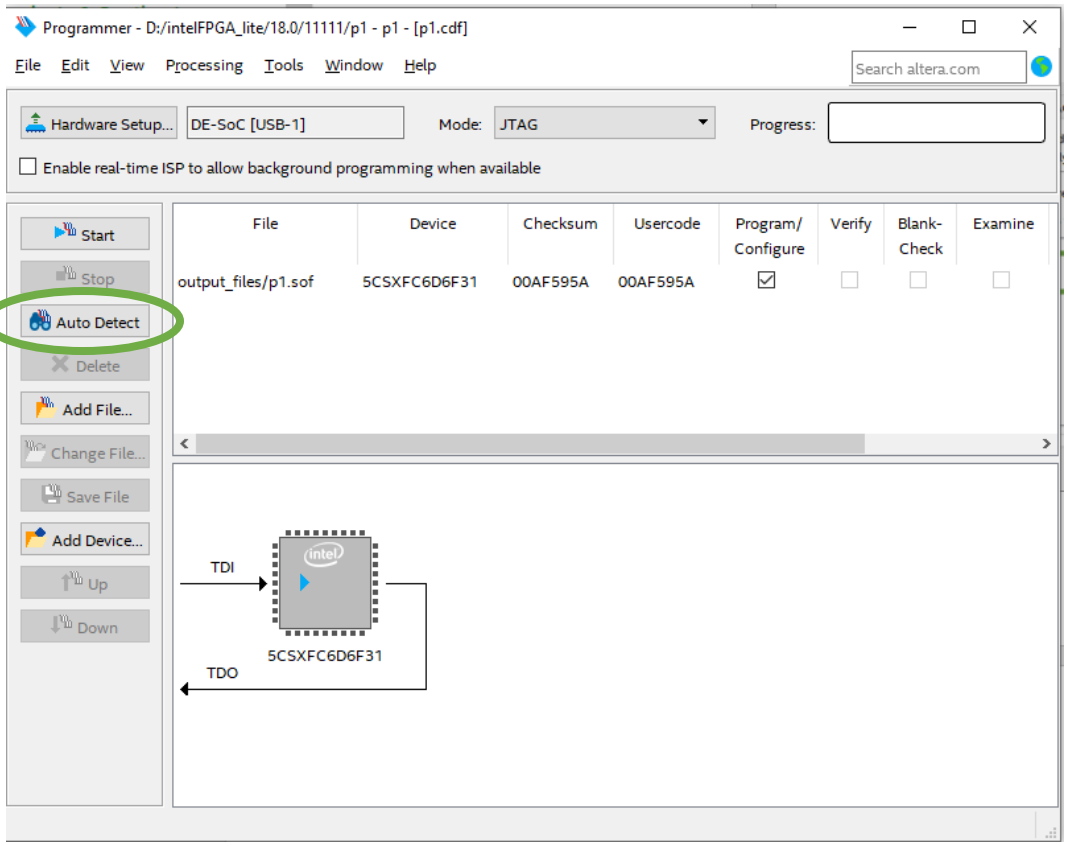
Make sure the board is turned on and is connected to your computer.

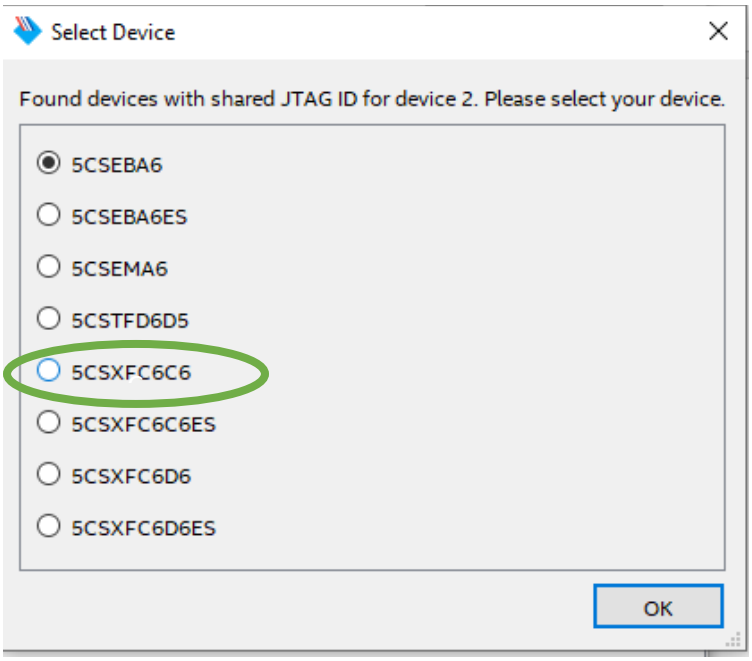


If this shows no hardware, then click on hardware setup.

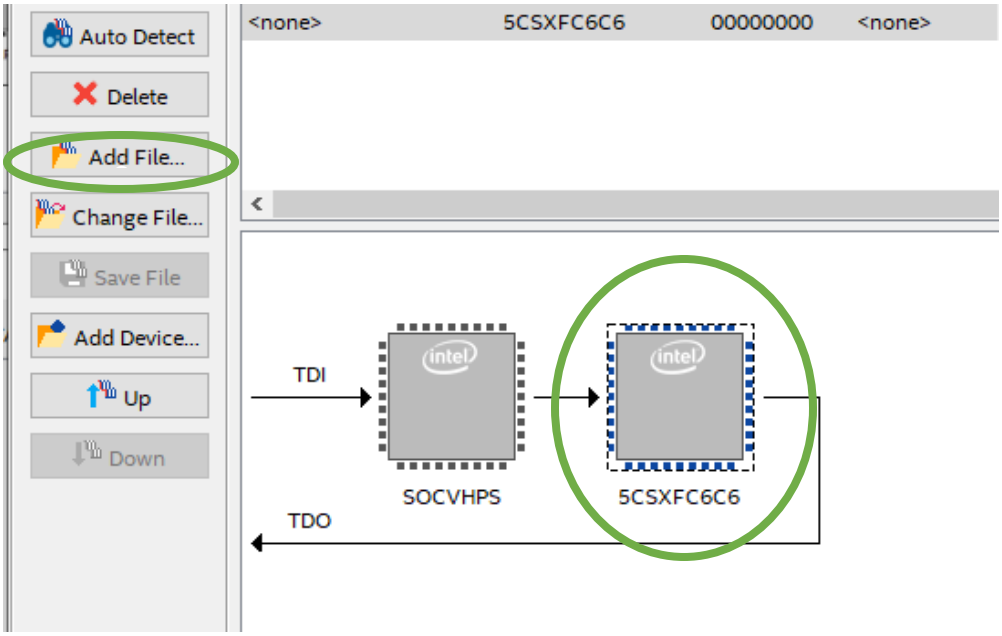


Double click on DE-SoC and close.



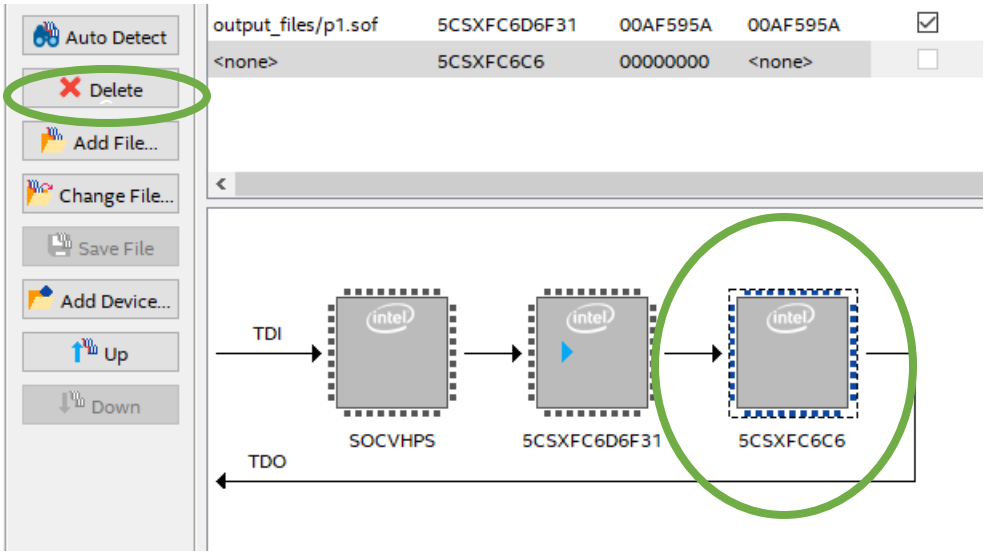


Select 5CSXFC6C6, 4th from the last



Select the 2nd chip and hit Add file.

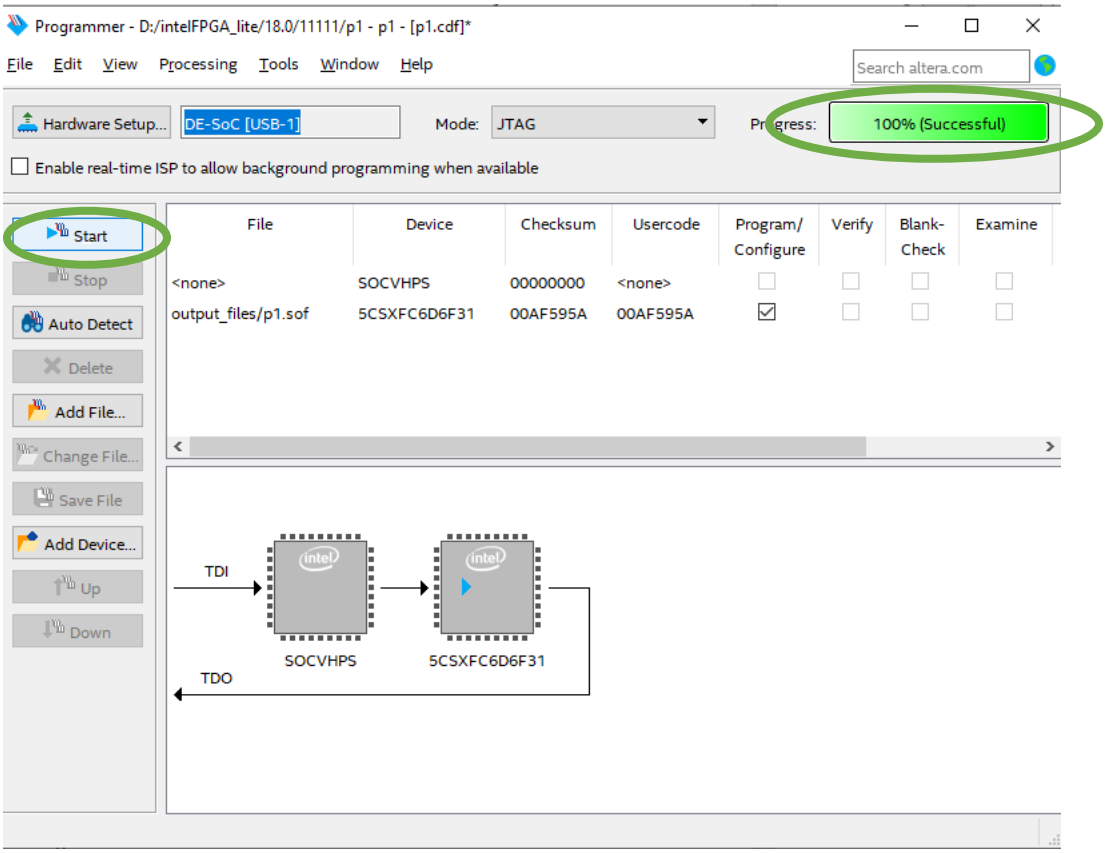
Go to the output files folder and select the .sof file



Select the last one and hit delete.

Finally click start so that it'll program the board

You can see the programming status on top right corner of the window



Check your board for the output.