Latches & Flip-Flops

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Combination/Sequential circuits

- Combinational circuits
  - Uses primitive gates
- Sequential circuits
  - Uses primitive gates
  - Also uses feedback and memory elements
  - Latched and flip-flops
    - Have feedback and are a memory element
  - Can be asynchronous – not synchronized to a clock
  - Can be synchronous – synchronized to a clock

Latch

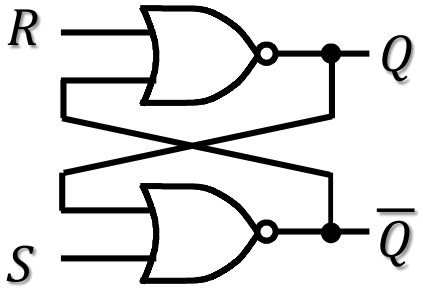
- Since latches are a memory with feedback
  - Always concerned with the
    - Present output or state Q_t
    - And the next output state Q_{t+1}
- Combinational circuits (what we have done so far)
  - Output only depends on the inputs
- Sequential circuits (with latches and flip flops)
  - Output depends on the inputs but also on the current state or current output values
- Many different kinds SR, D, JK, T etc,

SR Latch

- States (outputs) can be defined by a truth table

"Truth table" or "characteristic table"

		Current State	Next State
S	R	Q_t	Q_{t+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	?
1	1	1	?

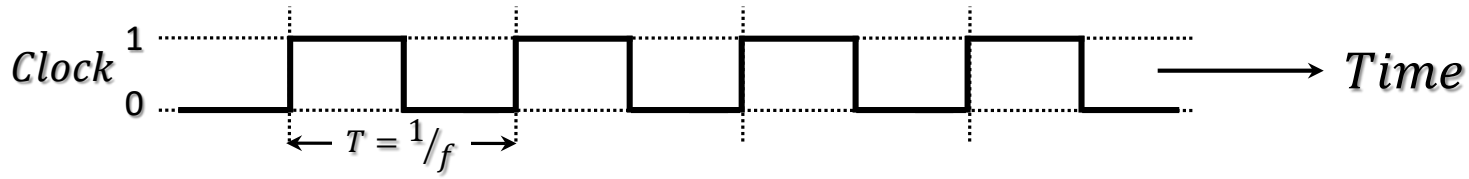


S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	0/1 ?

undefined state

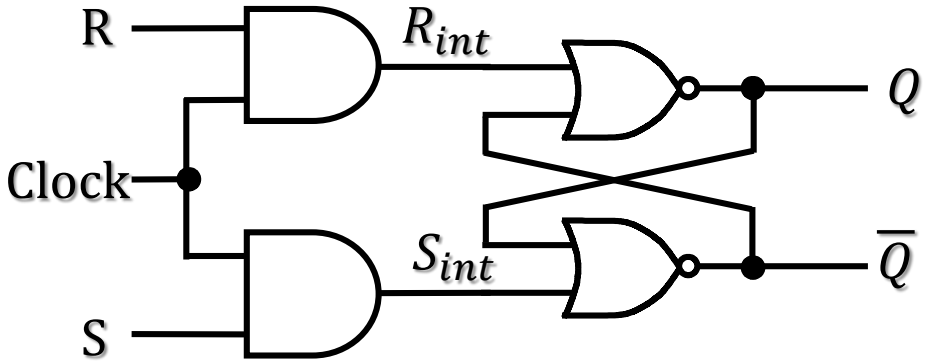
Gated SR Latch (with clock)

- States (outputs) can be defined by a truth table
- Clock – square wave, 50 % duty, at given frequency



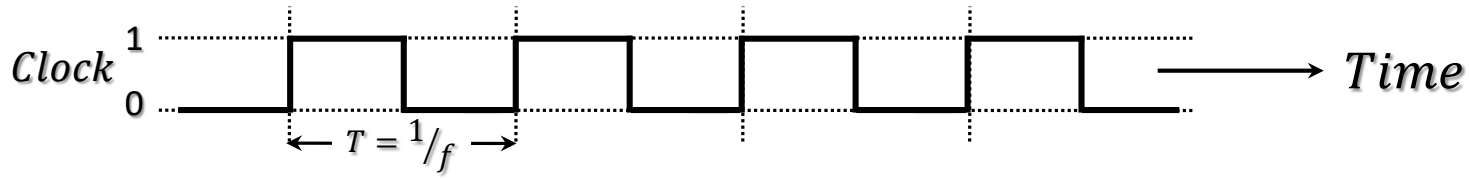
Characteristic table

Clock	*S*	*R*	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	0/1



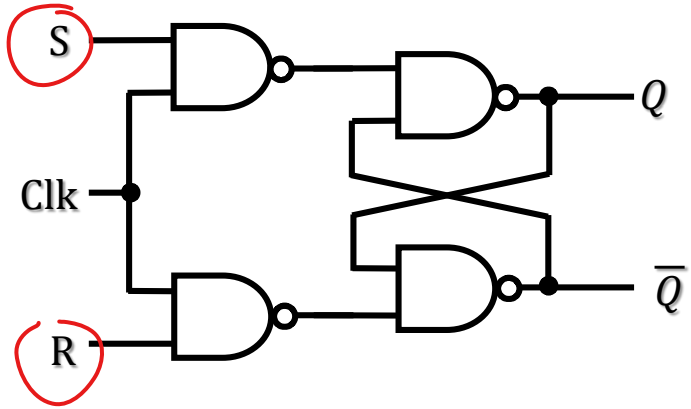
Gated SR Latch - NAND (with clock)

- Can also be done using just NAND gates
- Clock – square wave, 50 % duty, at given frequency



Characteristic table

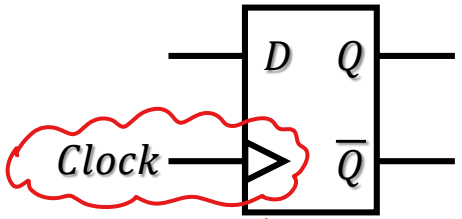
Clock	S	R	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	0	1
1	0	1	0
1	0	1	0



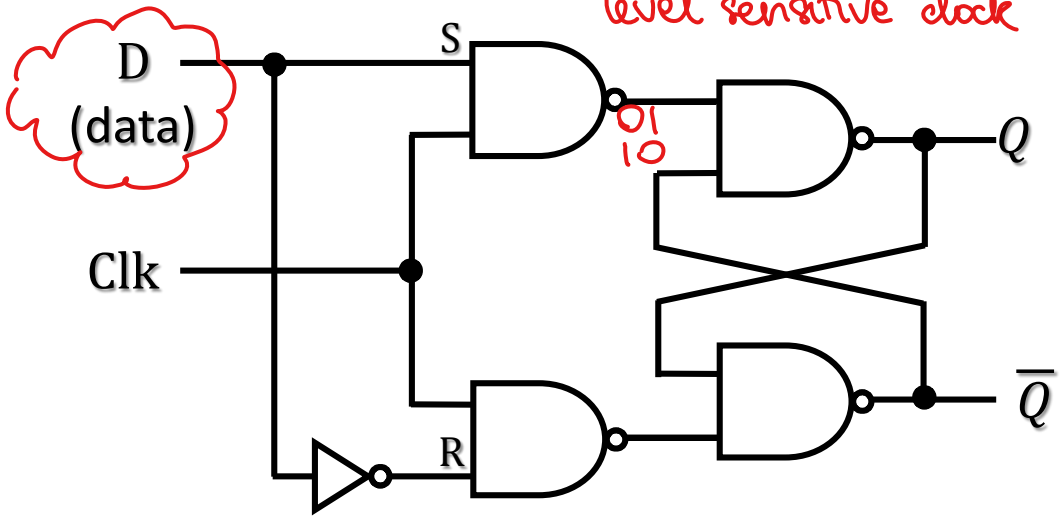
Gated D Latch (with clock)

- D-latch transfers input D to output Q
  - Next state $Q_{t+1} = D$
  - Simple 1-bit register (memory cell)
  - From SR latch – but $R = \overline{S}$

D-latch symbol



level sensitive clock



Characteristic table

Clock	D	Q_{t+1}
0	X	Q_t
1	0	0 = D
1	1	1 = D

↳ when clock's ON

JK Latch (SR + D + T 's functn)

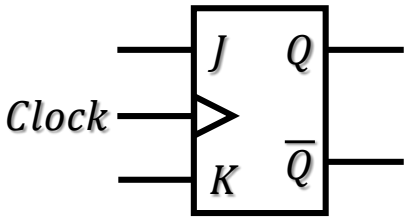
- JK-latch – likely most versatile latch

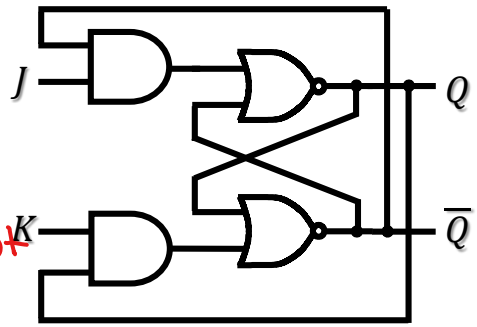
Characteristic table

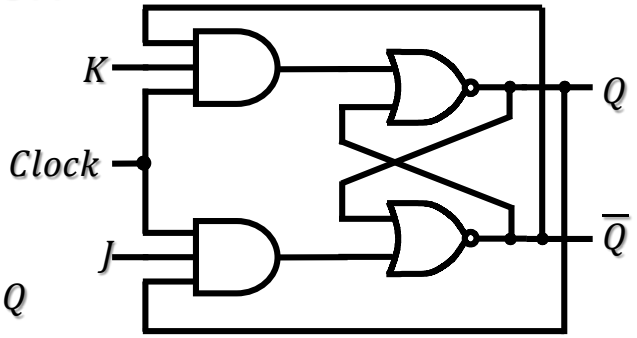
Clock	J	K	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	0	$\overline{Q_t}$

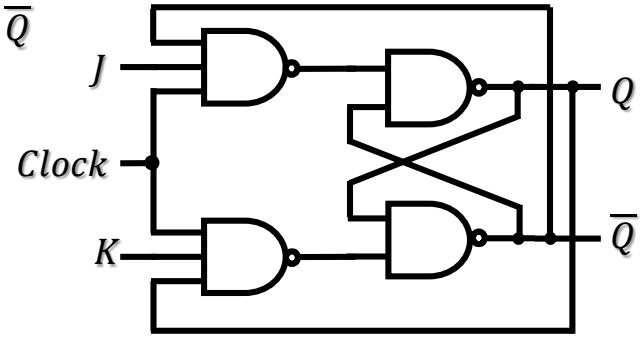
toggle output

JK-latch symbol









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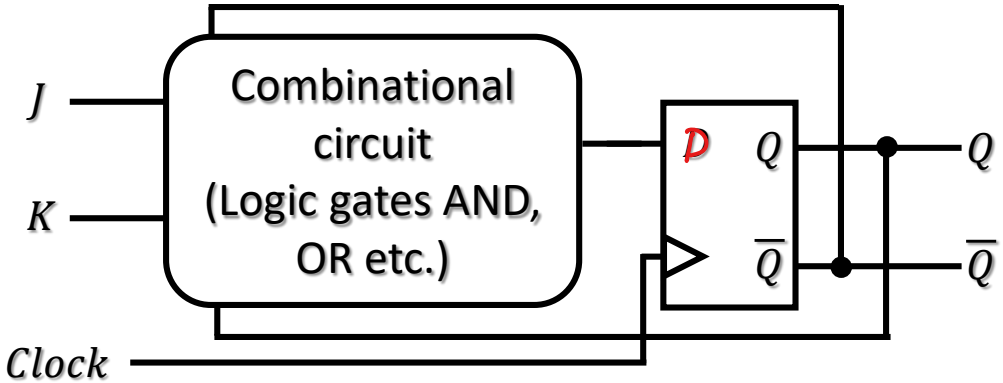
Make 1 latch from another type

- JK-latch – from a D
- Need to produce D as a function of J and K

What "D" input produce this value

J	K	Q_t	Q_{t+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

toggle



D	JK 00	01	11	10
Q = 0	0	0	1	1
Q = 1	1	0	0	1

$JQ + KQ$