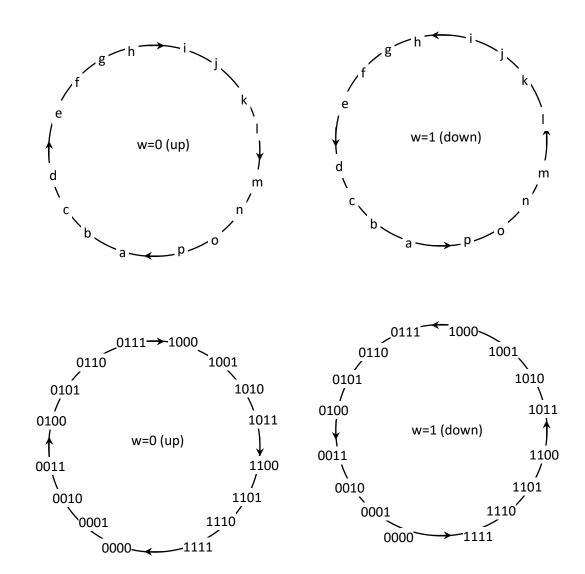
## 2020 Fall - ECE 2220 Laboratory 8: A Finite-State Machine - Up/Down Counter

## Instructions

1) Design a finite-state machine to generate the following sequence where the outputs and next state are dependent upon both the state of the circuit and the inputs. This is an up/down counter where the input (w) determines the direction of the counter. As show in the figure below, if the input, w=0, the sequence goes clockwise and if w=1, the sequence goes counter clockwise. The sequence just demonstrates a simple 4-bit up down counter.



DAB/2020-07-22

a) Create a state table for this finite state machine for the up/down counter.

Present	Next state	Output			
state	w=0	w=1	w=0	w=1	

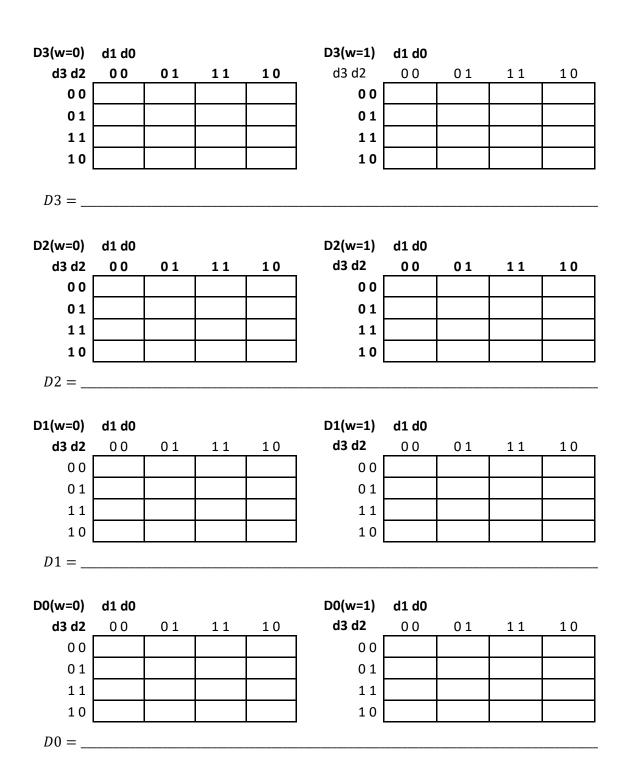
b) Explain how you could implement the same circuit with D flip-flops

Clock	D	Q(t+1)
0	0	Q
1	0	0
1	1	1

## State assignment

Current state					Next state w=0				Next state w=1					
			ļ											

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Using the any of the internal clocks, add a clock into your code such that the counter will count up or down at a 1 second interval. You will need to write a separate module for this. Use SW[0] to control the direction (up/down)of the counter and SW[9] as a reset which puts the counter back to zero. Use one of the LEDS in the middle show the state of the slow clock. Use the 1<sup>st</sup> and last LED to show the state of w and reset. Use one of the seven-segment displays to show the hexadecimal state of the machine. LEDs can be used to confirm the binary count and the slower clock. You may implement this counter using the D-latches as before or with some other "more efficient" code. Simulate the code and show it is working on the DE10 board.