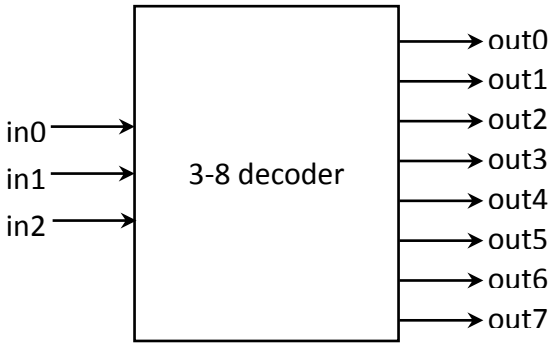
UNIVERSITY OF MANITOBA | Department of Electrical and Computer Engineering

2018 Fall - ECE 2220 Laboratory 6: Decoders and Encoders

Name(s):	Student number(s):	Section:

1) Introduction

In this lab, you will start by building a "3-8 decoder", a block diagram for which is shown in the figure below. The decoder has 3 inputs (in0, in1, in2) and 8 outputs (out0, out1, out2, out3, out4, out5, out6, out7). Based on the input values only one output will be set to 1 with the remaining outputs set to 0. For example, the first row in the truth table indicates that if the inputs to the decoder are in0=0, in1=0, and in2=0, then out0=1 and the remaining outputs are set to 0. If instead the inputs to the decoder are in0=0, in1=1, and in2=1, then the fourth row of the truth table indicates output out3=1 and the remaining outputs are set to 0.



a) Complete the truth table below.

In2	in1	in0	out0	out1	out2	out3	out4	out5	out6	out7
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

b) Implement the decoder behaviorally using Verilog, following the specifications in the truth table. Run a function simulation of the code. Using 3 switches for the inputs and 8 LEDs to display the outputs, implement the code using only primitives (AND, OR, NOT etc.) or their symbols ($, |, ~ etc.) on the DE10 board. Rewrite the code using a "case" statement.

Show the completed table, Verilog code, simulation and working hardware to the TA.

TA's signature

Priority Encoders

A priority encoder is a "one-hot" encoder where each input has an associated priority level and the output identifies the input with the highest priority. The input with a high priority is asserted and the rest of the inputs are ignored.

c) Design a 8-3 priority encoder where the 8 inputs are encoded in order such that in[7] has the highest priority and in[0] has the lowest priority. The data is only valid if another output, z=1. If no inputs are selected (In=0), z=0. Start by filling out the truth table below.

	In[7]	In[6]	In[5]	In[4]	In[3]	In[2]	In[1]	In[0]	Out[2]	Out[1]	Out[0]	z
i_0												
i_1												
i_2												
i_3												
i_4												
i_5												
i_6												
i_7												

d) Implement this circuit in Verilog using the row by row technique that was demonstrated in class. Create a Boolean expression for each row in the truth table. Calculate the output,

Show the completed table, Verilog code, simulation and working hardware to the TA.

TA's signature

e) Now implement this circuit using a **"casex"** statement.

Show the completed table, Verilog code, simulation and working hardware to the TA.

TA's signature

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