2020 Fall - ECE 2220 Laboratory 7 : Latches and Sequential Circuits

1) Introduction

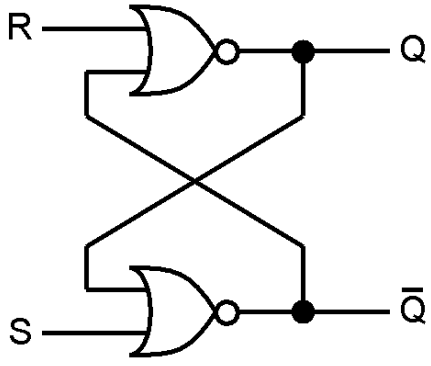
The circuits constructed in previous labs can be described as having user generated inputs provided on one side of the circuit and output(s) on the other side. These are referred to as *combinational circuits*. However, this is not the only form in which circuits may be constructed. In this lab, the concept of feedback and/or memory elements is introduced in which the final result utilises both of the circuit's input **AND** output signals to generate a final output.

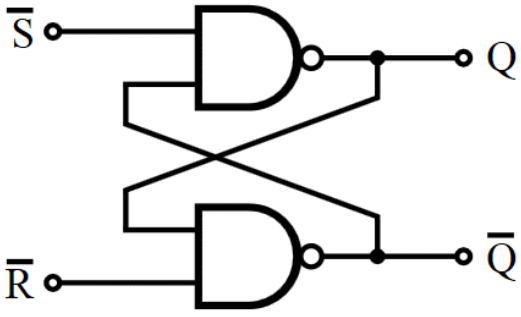
A pair of circuits utilizing the concept of feedback is shown below. Notice that the outputs, labeled Q and Q', feed back into the inputs of the gates. When NAND gates or NOR gates are connected as shown, the circuit is referred to as a "latch" or "flip-flop". The goal of this lab is to understand the operation of these types of circuits.

When Q = 1 and Q' (Q bar) = 0, it is in the **set** state (or 1 state); and when Q = 0 and Q' = 1, it is in the **clear** state (or 0 state). Since Q and Q' are defined as complements of one another any other state is considered invalid. A basic flip-flop is constructed from either **NOR** or **NAND** gates. In the **NOR** "latch", the gates operate with both inputs normally 0 unless the state of the flip-flop has to be changed. Conversely, for the NAND "latch" gates, the inputs are set to 1 under normal operation conditions unless the state of the flip-flop has to be changed.

2) Instructions

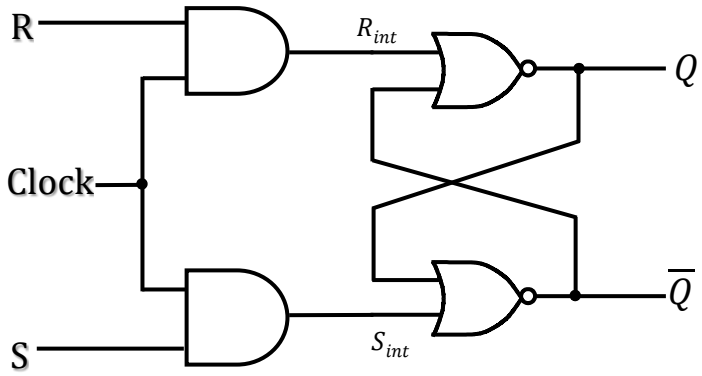
a) Build both versions of the flip-flop using the schematic diagrams and observe their operation. The "latches" must be built using the basic logic gates (NAND and NOR) and not using the Flip-Flop" blocks in Quartus II. Simulate these functions. Using switches as the inputs (R=SW[0] and S=SW[1]) and the two right (LED[1] and LED[0]). Leaving one LED blank use next 2 LEDs (LED[4] and LED[3]) as the outputs (Q and Q'). Complete the tables below. Explain the function of these circuits (relating the output to the inputs.) Why would inputs of these circuits be called "R" and "S"?





NOR FF						NAND FF				
S	R	Initial State (Q)	Q	Q'		S	R	Initial State (Q)	Q'	Q'

b) Add a clock input to your circuit as shown below. Use the switch SW[9] for the clock input and LED[9] as the clock output. Fill in the following table and simulate the circuit. Inlcude you code and the simulation in your report.



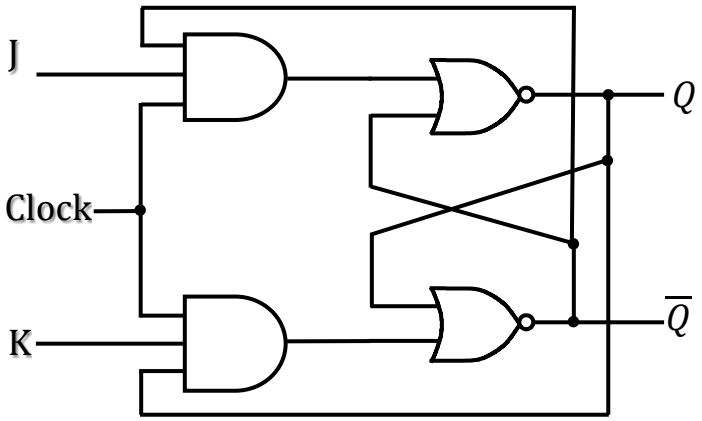
Before applying the clock				After applying the clock		
S	R	Q	Q'	Q	Q'	State

How does the clock input affect the function of the circuit? The previous circuits are referred to as being "asynchronous" while the clocked circuit is referred to as a "synchronous" circuit. Do these descriptions make sense to you? Why?

c) A D-latch simply transfers the input "D" to the output "Q" on each clock cycle. If the Clock is not high nothing happens to the output. Fill out the table below to find the circuit required to produce the inputs for the RS latch from the input of the D-latch. (Hint: Compare the conditions required for $RS - Q_{t+1} = D - Q_{t+1}$). Using the code from the Clocked RS latch as a module, write the top level model for the D-latch. Simulate the code and then download it to the board and test the functionality.

D	S	R	$RS - Q_{t+1}$	$D - Q_{t+1}$

d) A J-K latch can be made using a D-latch. The characteristic table for a J-K latch is given below. Fill out the characteristic table for a J-K latch made from a D-latch. Using the Karnaugh map, minimise the circuit required. Draw the circuit diagram. Using (some of) the code form your previous clocked D-latch (from an RS latch) write the Verilog code to implement this J-K latch. Simulate the code, compile it and download it to the board and test it. Comment on the simulation and test results on the DE-10 board



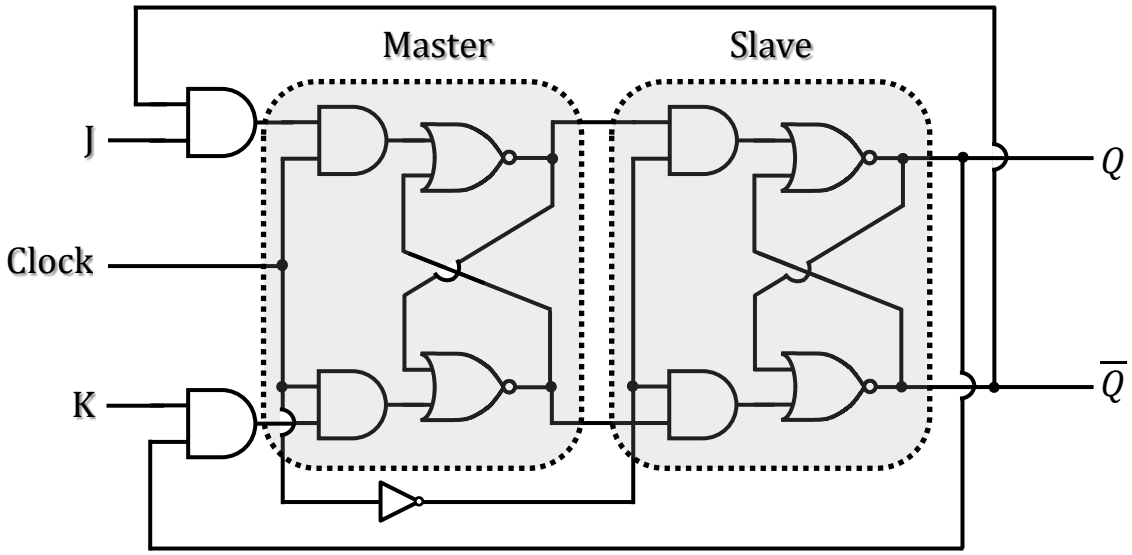
J-K Latch		
J	K	$Q(t)$
0	0	0
0	1	0
1	0	1
1	1	$\overline{Q}(t)$

J-K Latch from D-latch				
J	K	$Q(t)$	$Q(t+1)$	D

Q	JK 00	01	11	10
0				
1				

A more stable for of the J-K latch is referred to as a "master-slave" latch, which consists of two stages. This latch is edge triggered (as opposed to level triggered) where the "master" stage operates off of the positive edge of the clock and the "slave" stage off of the negative edge of the clock. The "master-slave" J-K latch is shown in the following diagram.

e) **<u>Master-Slave J-K latch</u>**. A simple clocked J-K latch is given in the diagram below.



Write the Verilog code for this J-K latch and implement this master slave latch. Simulate the code, compile and assemble and include your results in your report. You may use the previous code, but you are not required to.