2020 Fall - ECE 2220 Laboratory 4 : A 4-1 Multiplexer

Instructions

1) Draw the internal logic circuit diagram of a 4-1 multiplexer using AND, OR and NOT gates and include it in your report.

2) Implement this circuit using AND, OR and NOT gates in Verilog using switches for the inputs and selects, and LEDs to display the output.
   a) Write your Verilog code and include it in your report.
   b) Run a simulation of you Verilog code of the 4-1 Mux.. Show this to the TAs.
   c) Use switches SW[0], SW[1] SW[2] and SW[3] as the mux inputs. Use SW[8] and SW[9 as your selects. Use the corresponding LEDs for the inputs and selects (i.e SW[0]-SW[3] go to - LEDR[0], LEDR[1], LEDR[2], LEDR[3]) , the switches SW[8]-SW[9] go to LED[8] -LED[9] . Put the output MUX value (f) on LED[6].

3) Re-write the Verilog code using a "case" statement to model the MUX.
   a) Include your code in your lab report
   b) Assemble your code and run a functional simulation of this code. Show the output to the TAs.
   c) Assemble your code and program DE10 board using the same inputs and outputs used in 2).

4) Comment on the two Verilog codes (primitives or case statement) used to implement the same MUX. Is there any simpler way to implement this MUX? If yes, write the code for that.