The State University of New York at Binghamton

Department of Computer Science

CS 520 – Spring 2019

Project #2: Cache Design, Memory Hierarchy Design

By

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Honor Pledge: I have neither given nor received unauthorized aid on this test or assignment.
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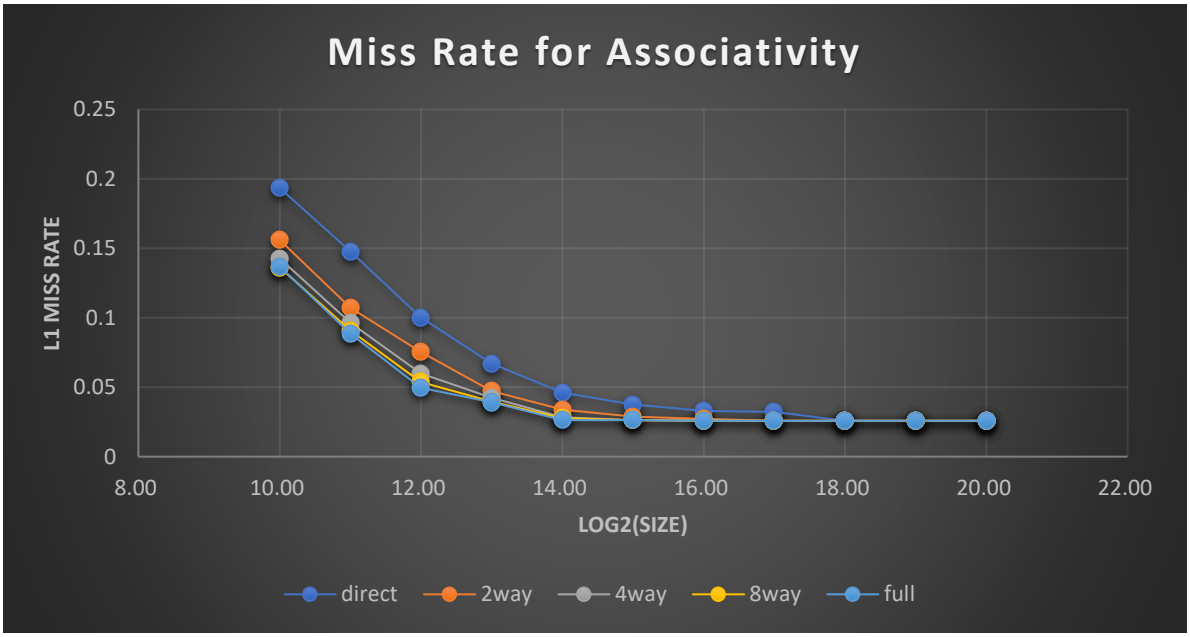
Graph 1:

Plotting L1 miss rate on y – axis and log2(size) on x-axis, for cache sizes 1KB, 2KB, …., 1MB in the power of two. The graphs contain five separate curves for different associativities i.e. direct-mapped, 2way set associative, 4way associative, 8way associative, and fully associative.



size	direct	2way	4way	8way	full
10	0.19346	0.15603	0.1427	0.13627	0.13696
11	0.14774	0.10714	0.09622	0.09069	0.0886
12	0.10017	0.07528	0.05992	0.05365	0.04954
13	0.067	0.04734	0.04247	0.03954	0.03912
14	0.04609	0.03384	0.02832	0.02774	0.02634
15	0.03768	0.02881	0.0264	0.02625	0.02624
16	0.03292	0.02713	0.02595	0.02589	0.02583
17	0.03233	0.0259	0.02582	0.02582	0.02582
18	0.02584	0.02584	0.02582	0.02582	0.02582
19	0.02584	0.02582	0.02582	0.02582	0.02582
20	0.02584	0.02582	0.02582	0.02582	0.02582

1) Trends in graphs

For the given associativity, when the size of cache increases the miss rate decreases, for higher cache sizes, the miss rates for the various caches have the same value.

For the given cache size, the miss rate decreases with an increase in cache associativity, because of the decrease in conflict miss rates.

2) Compulsory miss rate

When a block is referenced for the first time, compulsory miss rate occurs. We can estimate the compulsory miss rate with the larger size cache and for the full associative cache so the estimated value of compulsory miss rate be 0.02582

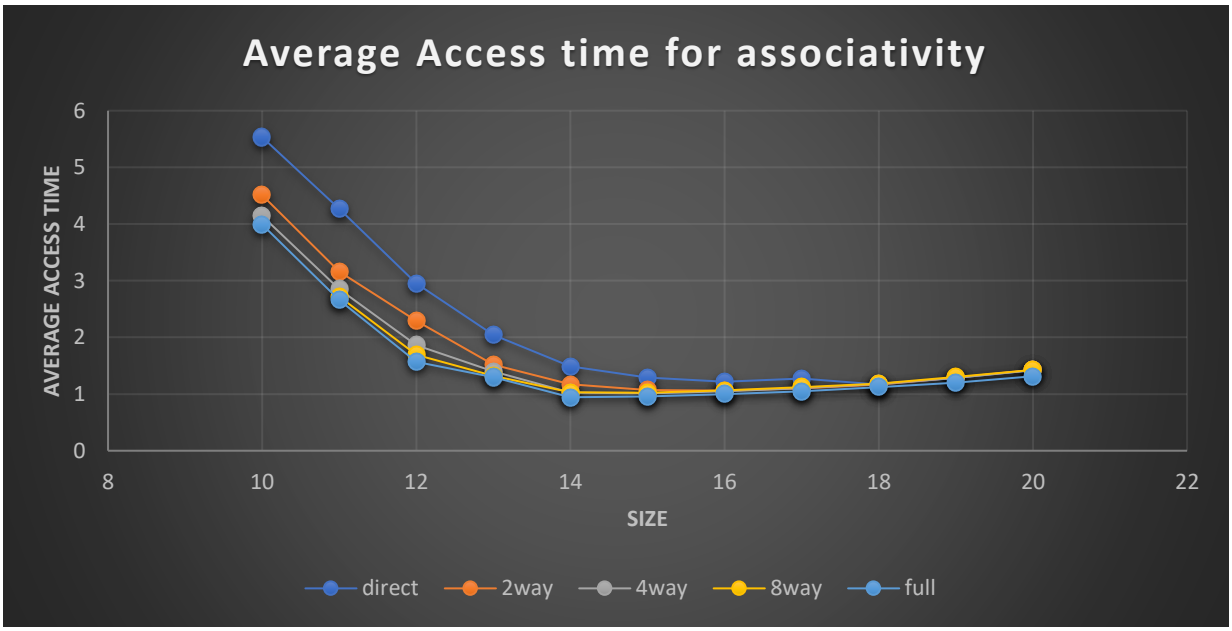
3) Conflict miss rate

Conflict miss rate can be calculated by the difference between the miss rate for fully associative and for different N way set associative cache.

	10	11	12	13	14	15	16	17	18	19	20
Direct	0.056	0.0591	0.0506	0.0278	0.019	0.0114	0.007	0.006	0	0	0
2way	0.019	0.0185	0.0257	0.008	0.0075	0.0025	0.0013	0	0	0	0
4way	0.005	0.007	0.01	0.003	0.002	0	0	0	0	0	0
8way	0.0006	0.0021	0.0041	0.0004	0.0014	0	0	0	0	0	0

Graph 2:

Plotting Average Access time on y – axis and log2(size) on x-axis, for cache sizes 1KB, 2KB, …., 1MB in the power of two. The graphs contain five separate curves for different associativities i.e. direct-mapped, 2way set associative, 4way associative, 8way associative, and fully associative.



size	direct	2way	4way	8way	full
10	5.531677	4.509169	4.14242		3.990364
11	4.26581	3.161611	2.848656	2.720006	2.657315
12	2.951765	2.288971	1.863445	1.691265	1.570068
13	2.03983	1.519715	1.400333	1.320031	1.293941
14	1.488937	1.171437	1.026896	1.031074	0.943128
15	1.288393	1.069126	1.01045	1.023511	0.95946
16	1.216387	1.060367	1.046081	1.066133	0.999521
17	1.27204	1.099803	1.10324	1.124196	1.045446
18	1.167332	1.169449	1.180645	1.181885	1.118969
19	1.286971	1.290704	1.287378	1.301137	1.198688
20	1.4229	1.429006	1.422567	1.428779	1.311434

For a memory hierarchy with only an L1 cache and Block size = 32

Fully associative yields the best average access time as the value at size 14 produces the lowest average access time i.e. 0.943128