# Nick **Gregorich**

Senior Engineer With Expertise in HW, SW, and Data

*San Francisco, California*

(858) 663-3229 | nlikenick@gmail.com | nick-gregorich

*Broadly skilled, system-level thinker with a passion for data, an eye for detail, and a love for bringing products to life*

## Education

### San Diego State University

*San Diego, California*

Master of Science in Electrical Engineering

- Emphasis in digital signal, video, and image processing including thesis under professor fred harris (sic)
- Courses: general / multi-rate DSP, modem design, adaptive algorithms, stochastic signals, estimation theory, A/V compression, image processing
- Thesis: *Audio Frequency Shifting on FPGA* implementing a real-time *brick wall* audio filter using Xilinx System Generator targeting a Virtex II FPGA

### San Diego State University

*San Diego, California*

Bachelor of science in Electrical Engineering

- Emphasis on DSP, FPGA, analog instrumentation
- Advanced technical writing for STEM students

## Skills

| | |
|---|---|
| **General** | Technical leadership, problem solving, creative thinking, proof of concept, prototype, debug, design for test / manufacture, metrics. |
| **Docs** | Product / engineering requirements and specifications, test protocols, code reviews, blogs, wikis, block diagrams, whiteboards, photography, annotation, demo videos, IEC 60601 / 62304, DFMEA. |
| **Computing** | macOS, Linux: Ubuntu / Mint, Red Hat / CentOS, Fedora; Windows 10, git: GitHub, GitLab, BitBucket; SVN, Mercurial, Jira, Slack, Confluence, Quip, Coda, Notion, Google Suite, Office 365. |
| **Tools** | JetBrains: PyCharm, DataGrip; VSCode, Sublime Text, Eclipse, Fork, HomeAssistant: ESPHome, AppDaemon; GitHub: Actions, Codespaces; brew, Wireshark: network, BLE, CVAT. |
| **DSP** | FFT, spectrograms, FIR, IIR, CIC, Reed Solomon, Viterbi, peak detectors, envelope followers, time series analysis, Nyquist sampling, SNR, convolution, windowing, wavelet, DCT, quantization, fixed point. |
| **Hardware** | Altium 365: library, schematic capture, layout; OrCAD: Capture CIS, PSPICE; KiCAD, DipTrace, LTSpice, Lab equipment: DC power supply, DMM, oscilloscope, current probe, signal generator, battery tester, spectrum analyzer, ESD tester, hipot tester, Saleae analyzer; calibration, compensation, low power, board bring-up, factory line bring-up, SolidWorks. |
| **Sensors** | Temperature, humidity, Hall effect, load cell / strain gauge, ambient light, image, voltage / current, pressure, flow, button / debounce, ultrasound, audio, piezo / vibration, PIR motion, ADC / DAC. |
| **FPGA** | Altera: Quartus 16.x, Stratix / Arria V, SignalTap II, Nios II, DSP Builder, Video and Image Processing Suite, Yocto, BitBake; Xilinx: ISE, ChipScope, System Generator, Spartan 3, Vertex II; technologies: I/O ring design, PLL / DLL, RTL design, place and route, timing closure, SERDES, LVDS, PCIe Gen3, DDR3, QDR II; simulation: RTL / gate level, component / chip level, self-checking test benches, bus functional models, ModelSim AE / DE / SE, QuestaSim, Aldec HDL, VCS MX, NCSim. |
| **Protocols** | Bluetooth Low Energy, UART, I2C, SPI, I2S / TDM, AC97, FTDI VCP / FIFO, PCIe. |
| **Embedded** | Platforms: ST Micro STM32, Microchip SAM4S, Nordic: NRF51, NRF52, NRF52840; Espressif ESP32, Microchip PIC 8 - 32-bit, Microchip / Atmel AVR 8-bit, Raspberry Pi 5, NVIDIA Jetson; Tools: gcc / make, Espressif IDF, ARM Keil, IAR, Segger J-Link, ST CubeMX, Microchip Studio, AVR Studio; RTOS: FreeRTOS, mynewt. |
| **AI / ML** | Linear regression , XGBoost, CNN, LSTM, ChatGPT / LLM application (via API), K-means, K-nearest neighbors, regressor, classifier, prediction; Database: Snowflake, InfluxDB / Flux, PostgreSQL / TimescaleDB. |
| **Full stack** | Web Bluetooth, AWS: CDK, IoT, CloudFormation, Certificate Manager, IAM, Amplify, API Gateway, Lambda, S3, RDS, Secrets Manager, ECR, ECS / Fargate, EC2 / Load Balancer; Docker, Podman, OpenAPI REST, Energy / Carbon APIs: WattTime, ElectricityMaps. |
| **Visuals** | Interactive dashboards, Streamlit, Plotly, Vega-Altair, Matplotlib, Grafana, Tablaeu, Numbers, Excel, MATLAB, ffmpeg. |
| **Languages** | Python: pandas, DuckDB, PySpark, NumPy, scikit-learn, XGBoost, PyTorch; SQL: Snowflake, PostgreSQL; MATLAB: Simulink; C, C++, Swift / SwiftUI: iOS / iPadOS / macOS / visionOS, Foundation, UIKit, Vision; Objective-C, Verilog / SystemVerilog, VHDL, HTML, CSS, JavaScript: TypeScript, Node.js, Yarn, D3.js, jQuery, Electron; Markdown, JiraQL, bash / zsh. |

# Experience

## Mill (Food Recycling Device / Service Startup)

*San Bruno, California*

Sensors and Algorithms Software

*March 2023 - Present*

- Led cross functional team to design multiple sensor systems, ESP32 and SAM4S firmware algorithms, and cloud ML for two generations of Mill food recycling devices and user apps
- Designed and instrumented lab experiments with high resolution firmware serial logs stored to InfluxDB via Python scripts on Raspberry Pi
- Developed interactive dashboards for teams to quickly and effectively parse and process large amounts of experimental data using Python, Flux for InfluxDB, Streamlit, pandas, and Plotly
- Developed temperature sensor fusion algorithm targeting SAM4S to reduce heater recalls from 100% to < 1% by identifying sensors not implemented in firmware using Altium 365, Saleae, VSCode, C, gcc, make
- Resolved post-launch factory lines down issue by going on-site, root causing issue, and developing component and top level assembly sensor tests
- Developed patent pending firmware sensor calibration routine to normalize input vs output humidity sensors per cycle to prevent offset creep from causing excessively long run-times, saving over 33% energy usage, and preventing RMAs
- Developed grinder jam prediction AI / ML classifier using PySpark, XGBoost, SciPy, scikit-learn on Snowflake in order to address #1 NPS feedback complaint: device jams. Optimized with parameter tuning and weighting unbalanced data. Achieved high precision and acceptable recall
- Developed Snowflake cloud-based gearbox failure classifier using increased motor tachometer sampling rate, band pass FIR filters, peak detection, and spectrograms to identify skipping gears. Exceeded company expectations by additionally detecting ”silent” shaft seal failure
- Developed in-field mass system validation by reverse engineering Bluetooth LE kitchen scale, developing accompanying Swift / SwiftUI iOS app that sends scale measurements to the cloud and compares with the on-device mass system. Deployed via TestFlight to around 50 users. Significant sources of mass system error identified and addressed in firmware algorithm
- Developed interactive device debug dashboards to aid firmware, hardware, and customer service teams in issue triage using Amazon AWS CDK Python, Docker, ECR, ECS / Fargate, EC2 / Load Balancer, Google OAUTH, and supporting functions to host Python Streamlit, pandas, and Plotly to visualize sensor readings, events, and AWS IoT shadows in a powerful yet easy to use fashion
- Developed computer vision system to replace traditional sensors in order to improve reliability, lower cost, and increase customer engagement using image sensor, Raspberry Pi, AWS S3, PyTorch, CLIP, ffmpeg
- Debugged, root caused, and fixed dozens of issues small and large in firmware, cloud, app, electrical, and mechanical systems
- Issue management using JIRA, communication via Slack, Google Suite, Coda, Notion
- Technical leadership and mentorship to bring together firmware, cloud, electrical, mechanical systems, operations, test, and product teams including teaching Python, pandas, Streamlit, SQL, and debugging to junior to mid-level engineers

## Calyxo (Kidney Stone Removal Startup)

*Pleasanton, California*

Consultant: Hardware / Software Architect

*October 2022 - March 2023*

- Developed proof of concept vision system for mechanical-only kidney stone aspiration (vacuum) system
- Researched image sensors that met strict mechanical requirements, found only 2 vendors: OmniVision and AMS
- Purchased and demonstrated both image sensors using demo boards featuring image sensor to USB UVC interface in video acquisition applications such as VideoLAN VLC
- Recommended Calyxo design in OmniVision OVM6948 image sensor module including lens. OmniVision would not respond to our calls or emails, so project was taken on by Synapse, an existing OmniVision partner who supported the design
- Reverse engineered OmniVision OVM6948 analog interface using an image sensor, power supply, Saleae ADC, and Python pandas and matplotlib. The intent was to lower BOM cost, de-risk the program, and improve image quality. Used data sheet and test cases such as all white and all black backgrounds to derive the critical timing parameters of the analog signal and decode it successfully in software
- Developed proof of concept irrigation and aspiration system including researching and specifying an irrigation pump and Alicat water and air flow / pressure controllers and sensors with serial interfaces. Developed irrigation / aspiration sequencing and data acquisition software in Electron / JavaScript to simplify packaging and deployment. Software featured sliders for various parameters, a real-time visualization of the specified sequence, and real-time plots of the sensor data as the sequence was running. System used as a prototype platform for aiding surgeons removing kidney stone fragments without the aid of a technician as is required today
- Interviewed hardware / software candidates on Calyxo’s behalf to hire a single engineer with electrical and Linux experience after the company was no longer happy with the results from Synapse. Bridged gap between Synapse and hiring an FTE
- Ran pre-TUV IEC 60601 EMC, EMI, ESD, hipot testing on NVIDIA Jetson Nano based image sensor to HDMI *Control Unit* box using spectrum analyzer, ESD tester, and hipot tester. Addressed issues with electrical layout changes, NVIDIA Jetson Nano pin out changes, and software mitigation
- Led Control Unit manufacturing process with mechanical and manufacturing teams including writing a PCBA electrical test procedure, implementing critical component FAI and IQC tests, and writing a system integration test procedure
- Wrote IEC 62304 compliant software documentation including SDP, SRS, SWAD, SDS. Wrote a requirements trace matrix tool in Python that read requirements and test documents in Word format and ensured all requirements were satisfied
- Resolved all open software bug reports and feature requests in GitLab including UI revamp, image scaling, auto-brightness algorithm adjustments, and graceful recovery after ESD events re-enumerated the USB UVC interface. Software stack included linux4tegra and GStreamer written in C. Implemented CI / CD pipeline to build after merging pull requests and automated testing on Control Unit hardware

### Apple Inc. (Software engineering organization)

*Cupertino, California*

Senior Software Engineer / Architect

*April 2021 - October 2022*

- Hired as system level hardware / software architect for newly formed, yet to be released *ultra* project
- Researched in-home energy and carbon optimization products, standards, and techniques including reading Department of Energy, National Renewable Energy Laboratory, and IEEE white papers as well as understanding products on the market including WattTime, ElectricityMaps, REsurety
- Developed energy optimization techniques using Python, pandas, and matplotlib to process user charging and grid emissions data. The result of the modeling was rolled out as part of the iOS *Clean Energy Charging* feature which uses ML to learn user charging trends and minimizes the carbon emissions during the learned charging window
- Continued R&D for other proprietary carbon optimization features including integrating ML models into interactive dashboards in Tableau to aid team in exploration
- Prototyped novel user interfaces in Swift and SwiftUI targeting iOS in order to provide a working demonstration of simple user interfaces for complex, abstract optimization features
- Participated on a team developing a new iOS daemon. Significant contributions to Swift CLI daemon control utility in order to exercise the daemon and its internal and REST API calls
- Instrumented home with NIST calibrated sensors, dedicated wireless network, and high resolution data logging to PostgreSQL running TimescaleDB time series database in order to help quantify energy and comfort
- Developed energy field trial including selecting data acquisition systems, standing up Prometheus time series database, designing a database schema with the flexibility to track changes to the system over time, and designing Grafana dashboards to monitor the data acquisition
- Joined Connectivity Standards Alliance Matter energy working group in order to influence group to include and mandate additional device control and reporting in order to facilitate smart energy optimization
- Developed proof of concept proprietary wireless networking features on Nordic NRF52840 in C using 2.4 GHz IEEE 802.15.4 radios
- Technical leadership between AI / ML, data science, data engineering, hardware, software, product, legal, and business development teams

### Progenity - Precision Medicine (Drug & Device Startup, Smart Capsule)

*La Jolla, California*

Principal Electrical Engineer

*August 2020 - April 2021*

- Transitioned prototype electrical and firmware design from NOVA Engineering to Progenity internal, including clean up of Altium library, schematic, and layout, partnering with a PCBA vendor to design ICT test fixtures and setting up a factory line where the PCBA was assembled into the smart capsule
- Designed break-out development and programming board to aid in firmware development and programming boards at the factory in Altium, including writing a board checkout procedure
- Rewrote RGB LED and ambient light sensor color-based localization algorithm in order to correctly calibrate system and improve sub-par clinical trial localization results in C targeting STM32
- Optimized power of sub-GHz ISM to Bluetooth LE radio interface by reducing quiescent current in the electrical system and introducing sleep in the NRF52 BLE radio to address clinical trial power failures
- Added battery impedance and open circuit voltage tester and data logging on the factory line in order to address other clinical power failures
- Developed increasingly complex test fixtures to test localization algorithm improvements without needing to schedule a costly in-animal study. Simple fixtures were painted, light-blocking 3D printed cylinders, complex were firmware-controlled, motorized, string-drawn capsules surrounded by anatomically accurate prints within PVC pipe

### JUUL Labs (E-Cigarette / Vaporizer Startup)

*San Francisco, California*

Technical Lead

*October 2018 - July 2020*

- Led team of 5 engineers in R&D of novel inductive heat drug delivery system including developing non-contact heating and temperature control loop, designing proof of concept hardware, designing and rendering product in SolidWorks, and presenting product line proposal to C-suite including CEO. Inductive heating enabled environmentally friendly designs featuring no plastics, only paper, cellulose, and foil. Procured foil heating elements with critical material properties required for temperature control. Wrote temperature control loop monitoring zero-voltage-switching oscillator frequency to set output power using C targeting STM32 microcontroller
- Designed novel test fixture to detect battery short circuit while inserting FPC connector into PCBA to fix critical lines down issue blocking product launch in South Korea. Test fixture used strategically placed Hall effect sensors to monitor excessive current in the battery FPC traces. Other technologies evaluated included thermal imaging and temperature sensors, which had significant shortcomings compared to the Hall effect sensor. Characterized sensor using pulse generator and oscilloscope to vary amplitude and duration of short circuit event. Managed test engineer to implement Hall effect sensor with LabView. Went to factory in Suzhou, China to add test fixture to factory line. Improved factory line safety, increased yield, and unblocked Korean launch
- Designed flexible, quad-zone resistive heater R&D drug delivery system using JUUL proprietary temperature coefficient of resistance based temperature control loop. Firmware written in C++ ”C with classes” in Apache mynewt RTOS targeting STM32 and included device drivers, CLI interface, data logging, PID control loops. Used Python pandas and matplotlib to analyze data logs
- Developed firmware for R&D testing in MicroPython targeting PyBoard including writing a patch to MicroPython to support interrupt / buffer based UART TX functions over the MicroPython polling design. Projects include interfacing to biometric sensors for age-based verification and automation of heating element characterization equipment
- US Patent granted: US20230157373A1: Vaporizer device including adaptive temperature profiling

### Chrono Therapeutics (Drug & Device Startup, e-Nicotine Patch)

*Hayward, California*

Manager of Systems and Electrical Engineering

*January 2016 - June 2018*

- Managed team of 6 firmware engineers, 1 electrical engineer, 1 systems engineer, and 1 technician to develop proof of concept e-nicotine patch to clinical trial and DFT / DFM for mass production. Included designing in Altium library, schematic capture, and layout and writing firmware in bare metal C using Keil targeting STM32, NRF51, and NRF52. Designed under IEC 60601 and 62304 standards including SDP, SRS, SWAD, SDS, SVT protocol, ERS, and TUV testing including EMC / EMI / ESD. Design included primary cell batteries, low power design, two processors with a SPI-based inter-processor communication bus, a brushed DC motor and motor driver, Bluetooth LE including PCB antenna, and a user interface using an OLED display and push buttons. Bluetooth LE connected to an iOS device which would log data to Azure cloud
- Developed device "report card" interactive dashboards using Azure SQL and Python pandas, matplotlib and bokeh
- Verified Bluetooth LE functionality using Wireshark and Nordic Bluetooth LE sniffer including advertising specifications, pairing / bonding, and debugging communication issues between the nRF51 / nRF52 and iOS
- Developed lab and factory test procedures for battery open circuit voltage and impedance testing, motor drive algorithm development, and firmware integration test using Python Jupyter Notebooks and PySerial
- Managed project using Visual Studio Online, Teams, Slack, JIRA, bitbucket / git

### Acutus Medical (Med Device Startup, Mapping Atrial Fibrillation)

*Carlsbad, California*

Consultant: FPGA, ARM, and Electrical Engineering

*April 2017 - March 2018*

- Participated in a team of 8 engineers to develop second generation of the Acutus AcQMap catheter localization, ultrasound, and dipole moment sensing system. Work divided 80% FPGA development, 10% ARM firmware, and 10% electrical engineering. Design had 32 pizza box sized cards each containing 2 large FPGAs. System interconnected with custom SERDES links running over SFP fiber and eventually aggregated to a single FPGA for transmission to a Windows PC via USB 2.0 and later GbE
- Designed all FPGA logic with another FPGA engineer including part selection, I/O ring design, 90-page schematic reviews, proof of concept using development kit and "coupon" board populated with critical components to test communication on. Collaborated with other FPGA engineer to define every module required in the design, divided the work, and developed each module including self checking test bench in Altera Quartus and ModelSim targeting Stratix IV / V, and integrated the modules into full FPGA images
- Developed modules for custom console messaging protocol implemented by Windows PC, every FPGA, and every ARM in the system, developed remote system upgrade for FPGAs to receive new image via messaging protocol and write it to QSPI flash, updated SERDES from 1.125 to 3.125 Gbps which required all interfaces be redesigned from 8-bit to 32-bit. Added automated git code check in per FPGA build and added hash to FPGA image in order to provide certainty of the exact codebase used to generate every image which was very helpful in lab debug
- Developed FPGA and ARM firmware for Analog Devices ultrasound analog front end (AFE). The AFE data bus was connected to the FPGA via source synchronous LVDS and the control bus was connected to ARM via SPI. A complex state machine was required to do phase alignment and word synchronization on the LVDS bus where the FPGA would instruct the ARM to turn on different I/O test patterns in the AFE via SPI bus
- Developed Jupyter notebooks to verify FPGA CRC32 logic and generate realtime ultrasound time of flight animations to verify functionality of DDS chirp, signal path to the transducer, reflection from the DUT, AFE, FIR filters, and ToF calculator

### Octera Solutions / Macnica (Demand Creation Altera FPGA Distributor)

*Solana Beach, California*

Central Applications Manager

*March 2011 - May 2014*

- Managed team of 5 Altera and Broadcom applications and design services engineers including managing relationships with Altera and Broadcom, hiring team, balancing load across applications engineers, bidding on FPGA and DSP design services work, and managing server infrastructure
- Provided technical support and design services for all aspects of Altera products including Stratix, Arria, Cyclone, and MAX product lines, Quartus, IP cores, DSP Builder. Provided day to day applications support, reviewed FPGA schematics and layout according to Altera guidelines, built FPGA I/O ring by adding complex IP including PCIe, DDR3, QDR II, 10G+ Ethernet, added timing constraints, closed timing, ran place and route seed sweeps, built NIOS II embedded processor design examples, demonstrated DSP Builder MATLAB Simulink block set, built Yocto Linux BSPs for Arria V / Cyclone V SoC
- Participated on a team of 3 to develop DrivExpress C++ based PCIe simulation BFM including writing re-entrant functions targeting Verilog DPI to run PCIe simulations in ModelSim significantly faster than RTL BFM provided by Altera

### Erthenvar (Boutique Electronic Musical Instruments & DIY)

*San Diego, California*

Small Business Owner

*November 2010 - September 2018*

- Founded lifestyle electronic music and maker business designing mechanical components in SolidWorks, audio schematics and layout in DipTrace, analog simulation in LTSpice, FPGA synthesizer design in Altera Quartus targeting Cyclone IV, RTL simulation in ModelSim, and ARM synthesizer design in Keil doing realtime FFT processing using CMSIS DSP for STM32. Work extended beyond engineering into e-commerce on self-hosted OpenCart and Shopfiy, digital marketing campaigns, YouTube demonstration videos, inventory management, accounting, hiring a customer service and shipping specialist, and managing manufacturing in China

### Altera (FPGA vendor, now Intel Programmable Solutions)

*San Diego, California*

Advanced Applications Engineer

*November 2008 - March 2011*

- Developed and supported DSP, embedded, and software reference designs for Altera FPGAs using Altera Quartus II, DSP Builder MATLAB Simulink block sets, NIOS II embedded processor and toolchains. DSP designs included FFT, FIR, CIC, Viterbi decoder, Reed Solomon encoder and decoder, and video and image processing. Software designs include sdc timing constraints for I/O and internal logic, timing closure, place and route, synthesis, and simulation. NIOS II designs include CLI interfaces and interfacing to triple speed Ethernet core using uCOS II RTOS and NicheStack