Outline

- Internship — Assistant Test Engineer of Wafer at **KYEC (*Wafer chip probing*)**
- Course Record — Convolution Neural Network, Computer Graphics 3D Rendering, Digital IC Design Practice
- Master thesis (MATLAB,ImageJ) — Portable Low-Cost Confocal Microscope Based on Pinhole Array and Smartphone (***Image processing***)
- Personality

Underwater image deblurring

Fast Underwater Image Enhancement, FUnIE

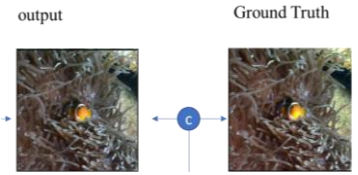
Model: FUnIE-GAN

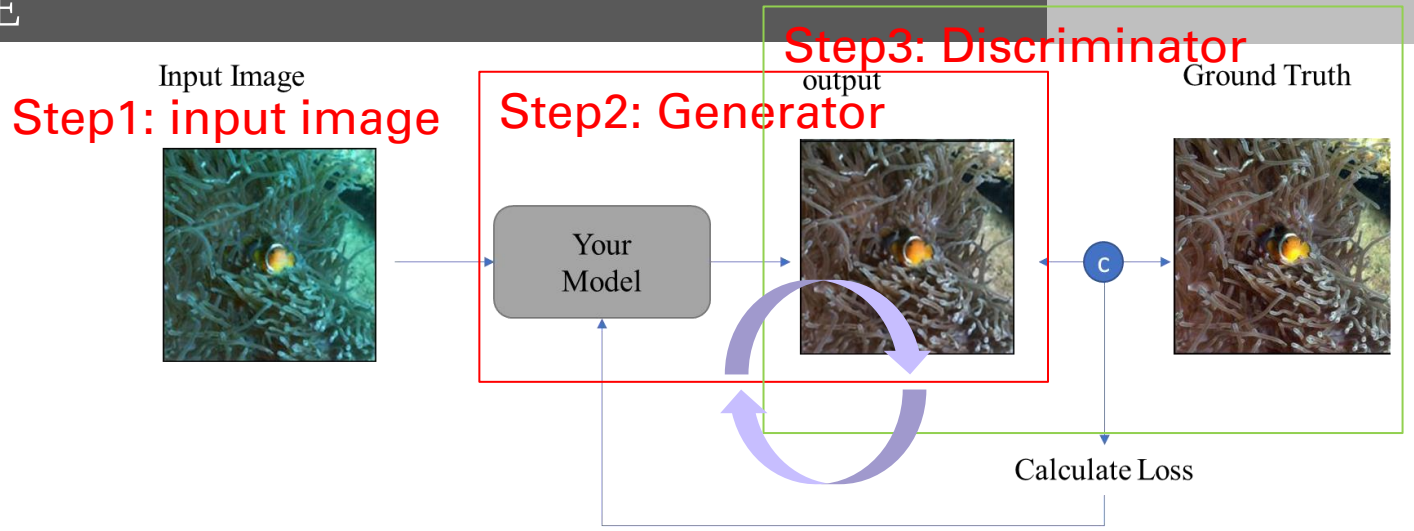
- **Neural Network**
  1. Generator: Using **Unet**
  2. Discriminator: Using **PatchGAN**
- **Loss function**
  1. Loss_G
  2. Loss_D

```
# Total loss (Section 3.2.1 in the paper)
loss_G = loss_GAN + lambda_1 * loss_1 + lambda_con * loss_con
```

```
# Total loss: real + fake (standard PatchGAN)
loss_D = 0.5 * (loss_real + loss_fake) * 10.0 # 10x sca
```

- **PyTorch**
- **Results**
  1. 515 sample
  2. SSIM : range[0, 1] , ***SSIM=0.8***
  3. PSNR : range[20dB, 40dB] , ***PSNR=26dB***





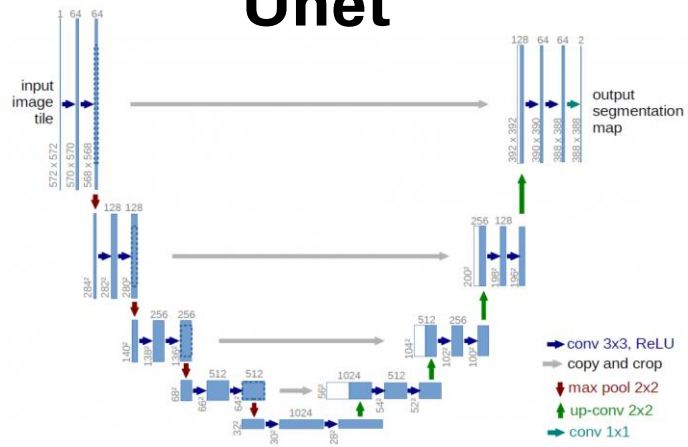
Underwater image deblurring

Fast Underwater Image Enhancement, FUnIE

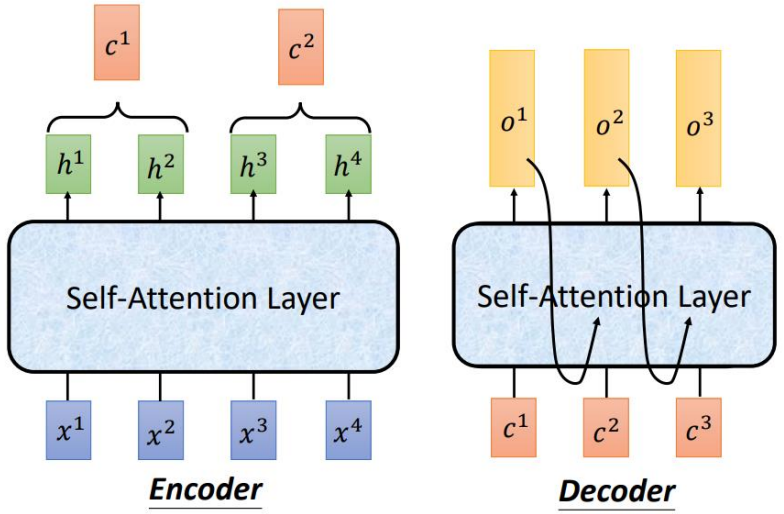
FUnIE-GAN

- **Neural Network**
  1. Generator: Using **Unet**
  2. Discriminator: Using **PatchGAN**

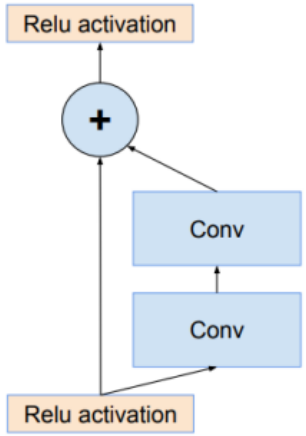
Unet



Seq2seq with Attention



Skip Connection



Residual Net V1

$$H(x) = F(x) + x$$

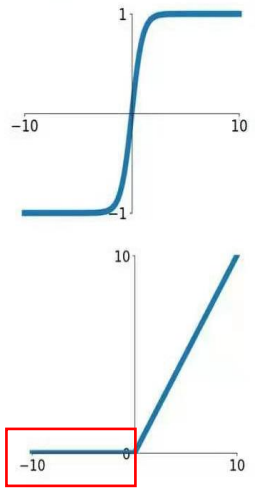
Vanishing gradient problem

tanh

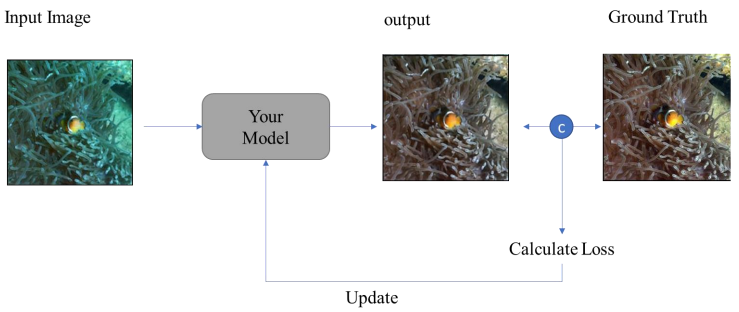
$\tanh(x)$

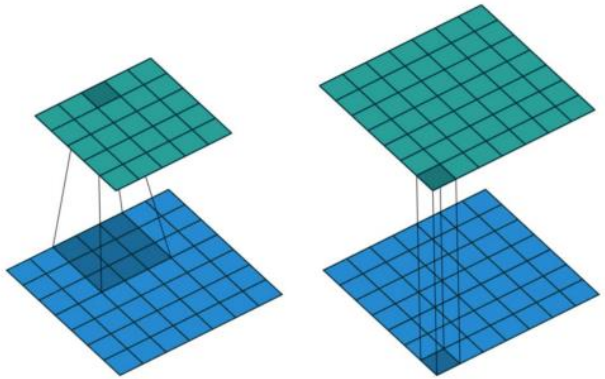
ReLU

$\max(0, x)$



x≤0, f'(x)=0



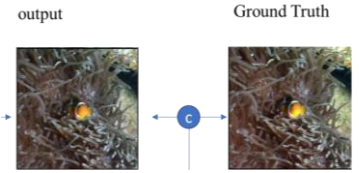


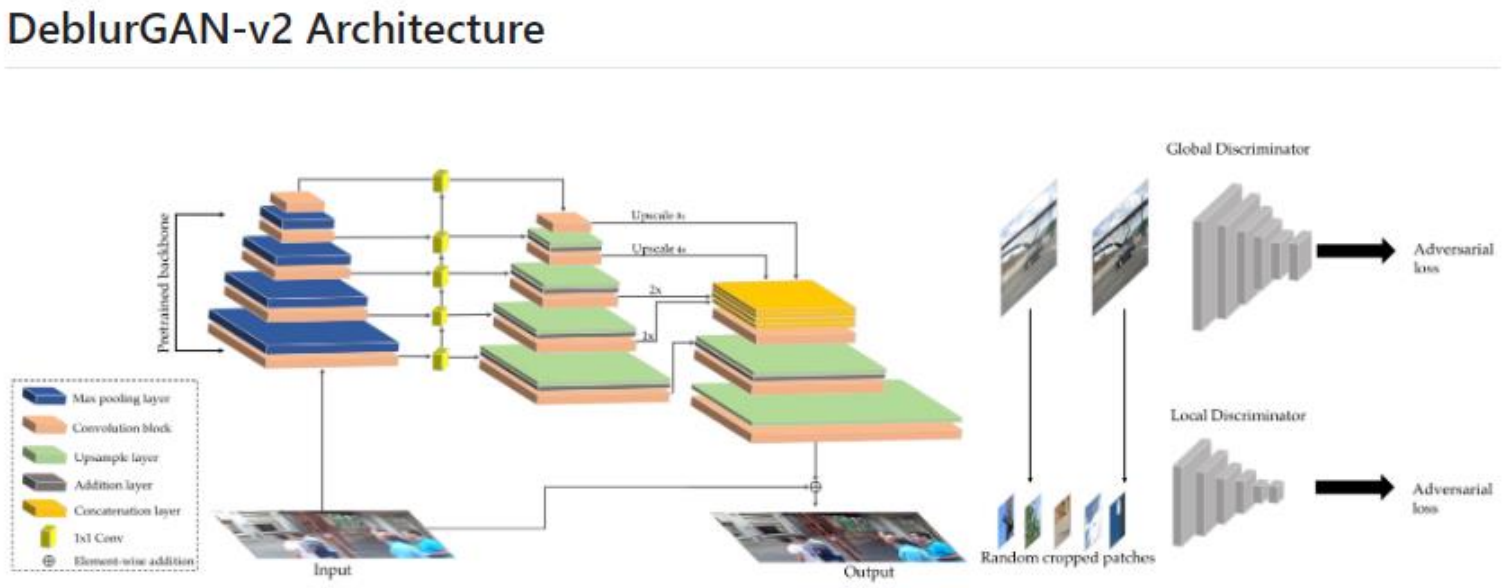
left: **with kernel of size 3x3**
right: **with kernel of size 1x1**

Underwater image deblurring

Results

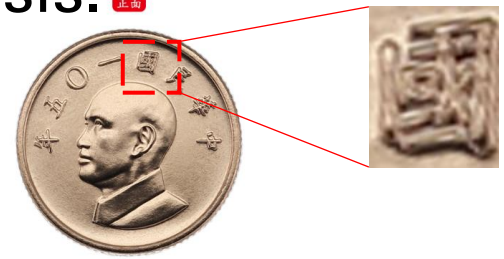
1. SSIM : range[0, 1] , SSIM=**0.8**
2. PSNR : range[20dB, 40dB] , PSNR=**26dB**

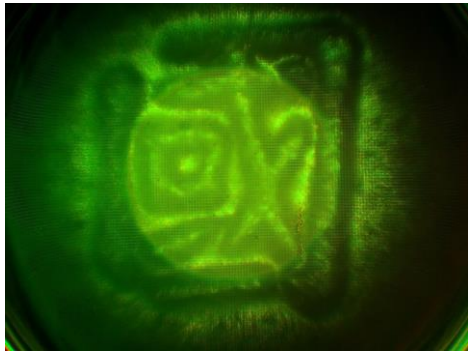




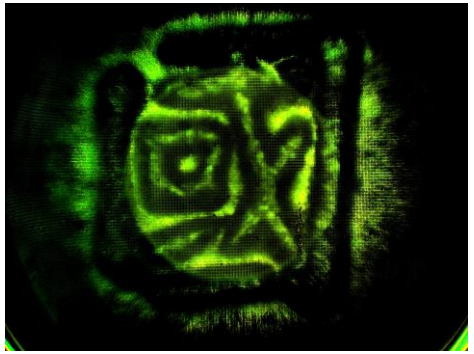
Ground Truth

Future work on my master thesis.





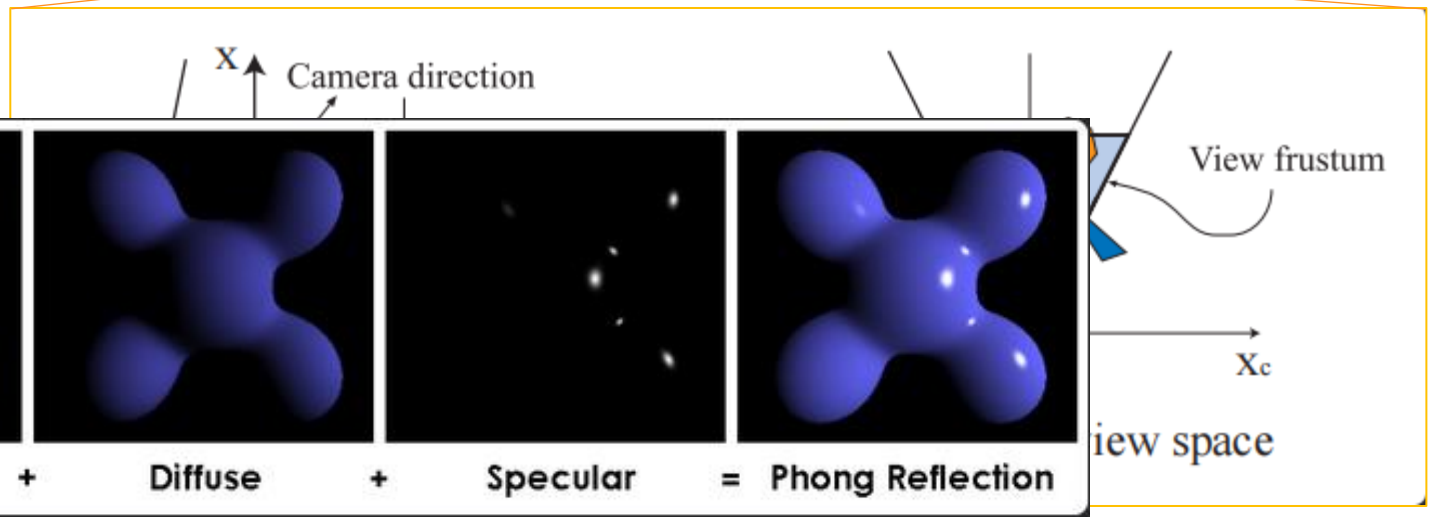
Original Image

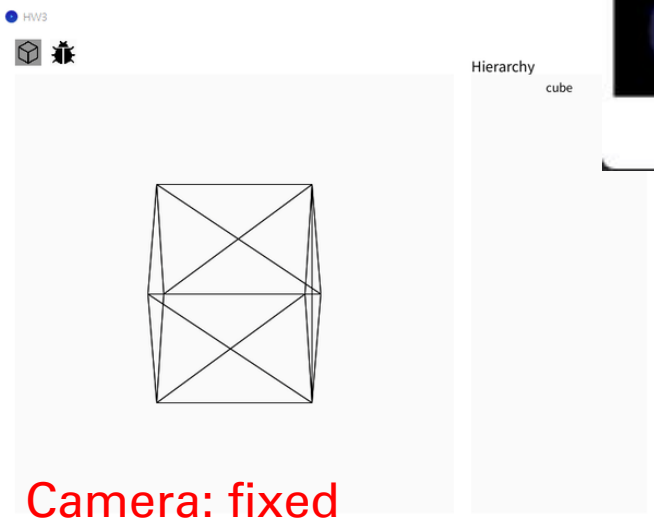


Output Image

Computer Graphics 3D rendering

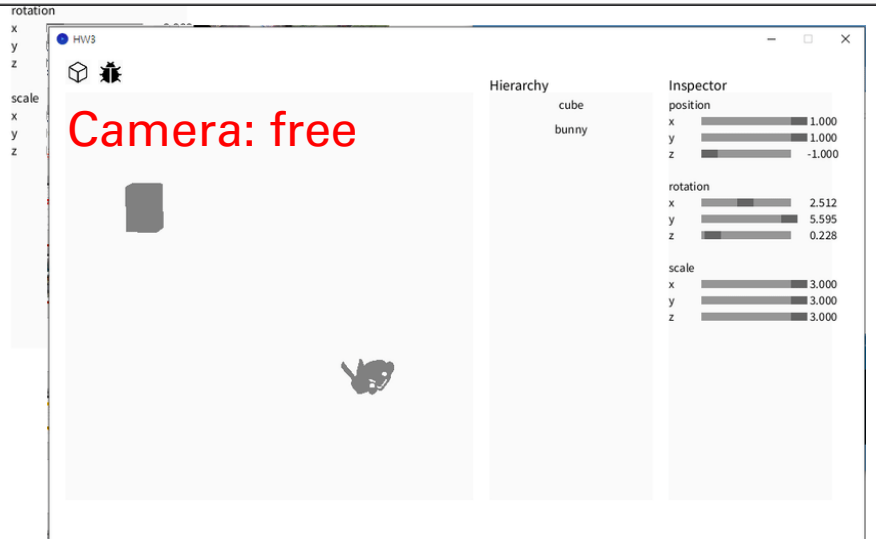
Local → world → view → screen

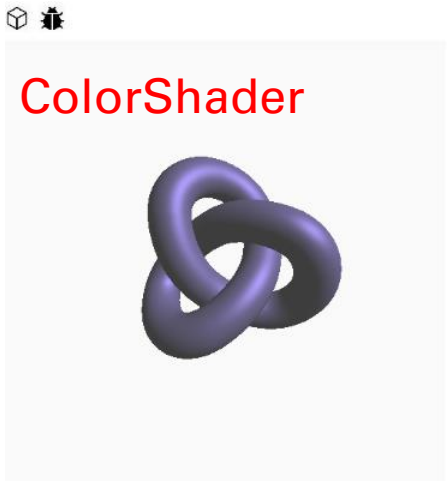




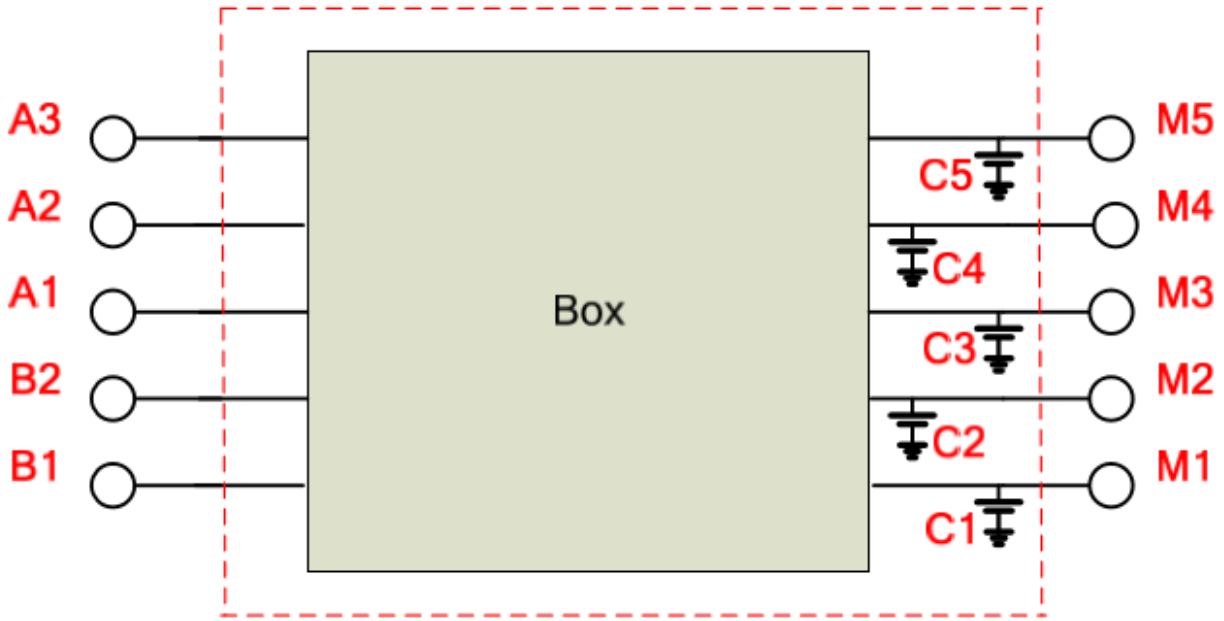
Camera: fixed

Object: xyz Geometric (translation、rotation、scale)





Digital IC Design Practice



圖二 Mulitplier3x2 內部電路圖

$$
\begin{array}{r}
 & A3 & A2 & A1 \\
* & & B2 & B1 \\
\hline
 & & C1 & \\
 & C2 & A3B1 & A2B1 \quad A1B1 \\
C3 & A3B2 & A2B2 & A1B2 \\
\hline
M5 & M4 & M3 & M2 \quad M1
\end{array}
$$

$$M5 = C3(M4\ 進位)$$

$$M4 = C2(M3\ 進位) + A3B2$$

$$M3 = C1(M2\ 進位) + A3B1 + A2B2$$

$$M2 = A2B1 + A1B2$$

$$M1 = A1B1$$

方程式一 電路計算方程式

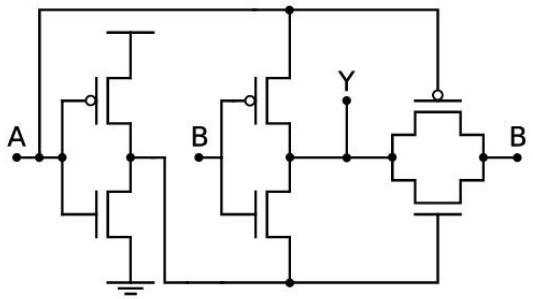
Total:
And: 6
Half_adder:2
Full_adder:1

Half_adder
Full_adder
Half_adder

Digital IC Design Practice

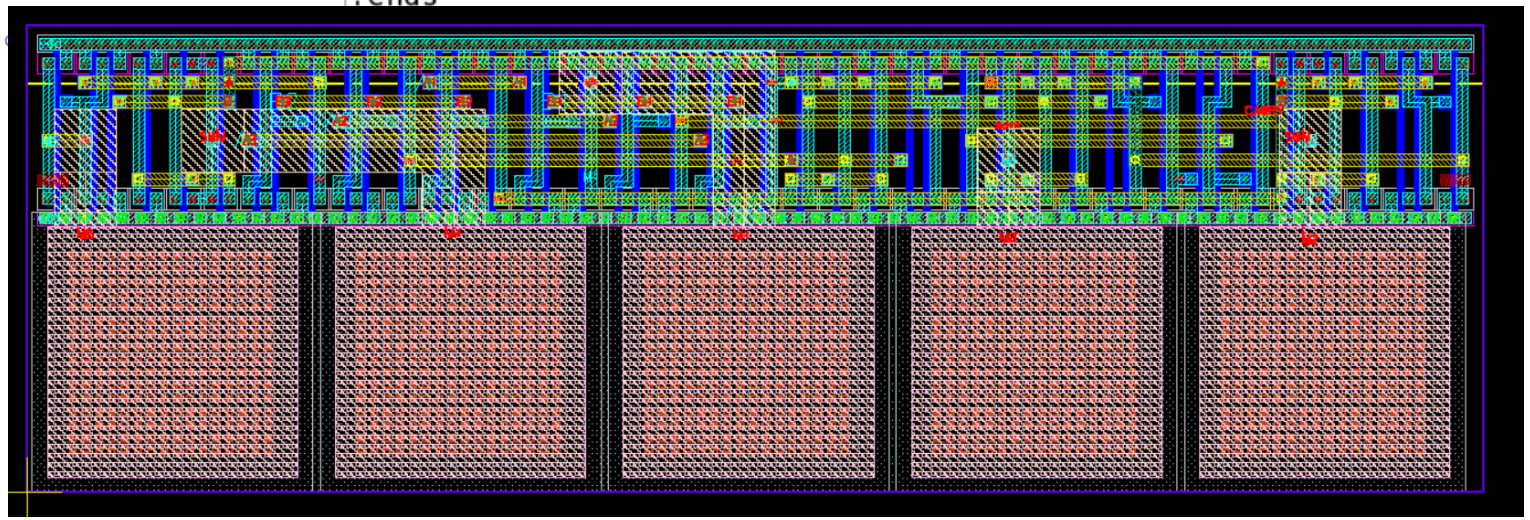
Model: Mulitplier3x2

- **Verilog**
- **Hspice**
- **Results**
  1. ***Layout***
  2. ***Presim & Posim***
  3. ***Drc & Lvs***



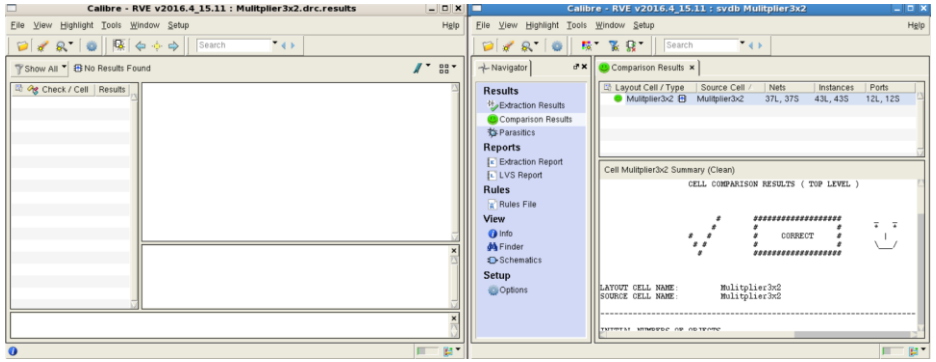

```
module mulitplier3X2( A3, A2, A1, B2, B1, M5, M4, M3, M2, M1);

    input A3, A2, A1, B2, B1 ;
    output M5, M4, M3, M2, M1 ;

    wire P0, P1, P2, P3, P4, P5;
    wire S1, S2, S3;
    wire C1, C2, C3;

    assign P0 = A1 & B1;
    assign P1 = A2 & B1;
    assign P2 = A1 & B2;
    assign P3 = A3 & B1;
    assign P4 = A2 & B2;
    assign P5 = A3 & B2;

    // M1
    assign M1 = P0;

    // M2 = P1 + P2 half_adder
    assign S1 = P1 ^ P2;
    assign C1 = P1 & P2;
    assign M2 = S1;

    // M3 = P3 + P4 + C1 Full_adder
    assign S2 = P3 ^ P4 ^ C1;
    assign C2 = (P3 & P4) | (P3 &
    assign M3 = S2;

    // M4 = P5 + C2 half_adder
    assign S3 = P5 ^ C2;
    assign C3 = P5 & C2;
    assign M4 = S3;

    // M5 = C3
    assign M5 = C3;

endmodule
```

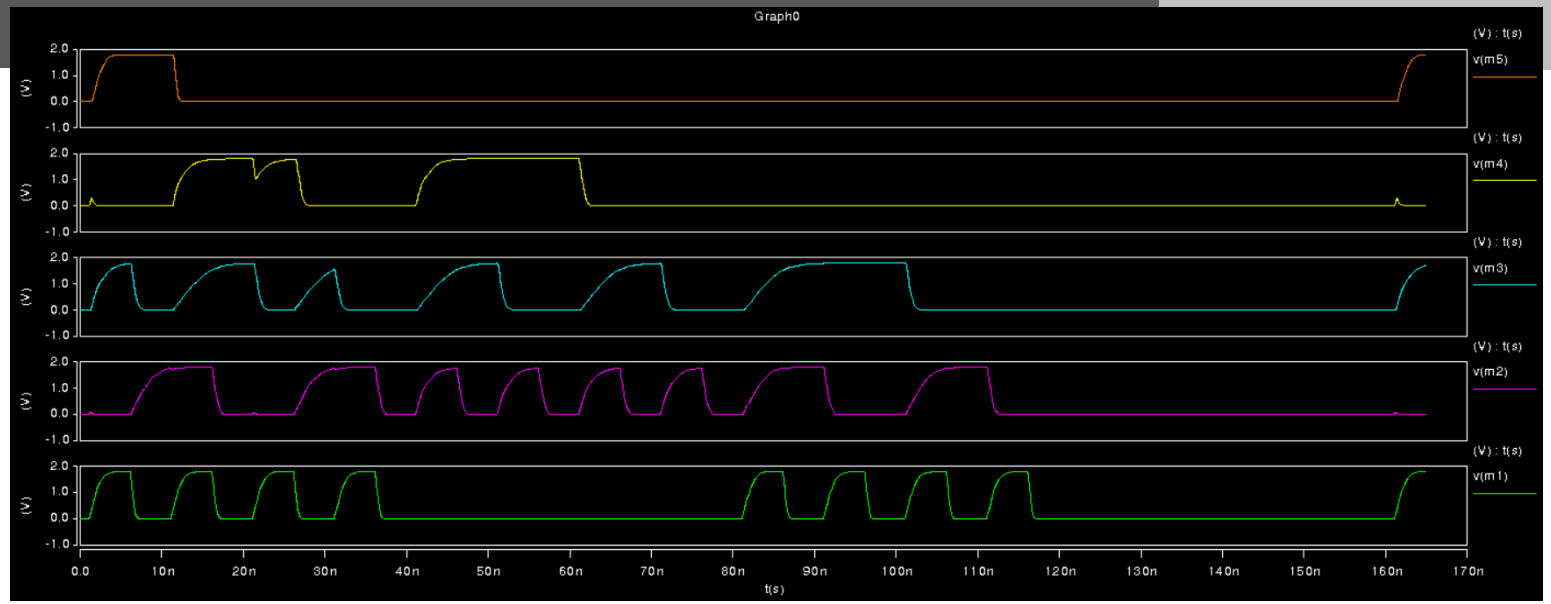
```
.subckt Mulitplier3x2  A1 A2 A3 B1 B2 M1 M2 M3 M4 M5 vdd gnd
Cl1 M1 GND 0.1P $[MIMCAPS]
Cl2 M2 GND 0.1P $[MIMCAPS]
Cl3 M3 GND 0.1P $[MIMCAPS]
Cl4 M4 GND 0.1P $[MIMCAPS]
Cl5 M5 GND 0.1P $[MIMCAPS]
x1 A1 B1 M1 vdd gnd / and
x2 A1 B2 a vdd gnd / and
x3 A2 B1 b vdd gnd / and
x4 a b M2 C1 vdd gnd / half_adder
x5 A3 B1 c vdd gnd / and
x6 A2 B2 d vdd gnd / and
x7 c d C1 M3 C2 vdd gnd / fall_adder
x8 A3 B2 e vdd gnd / and
x9 e C2 M4 M5 vdd gnd / half_adder
.ends
```

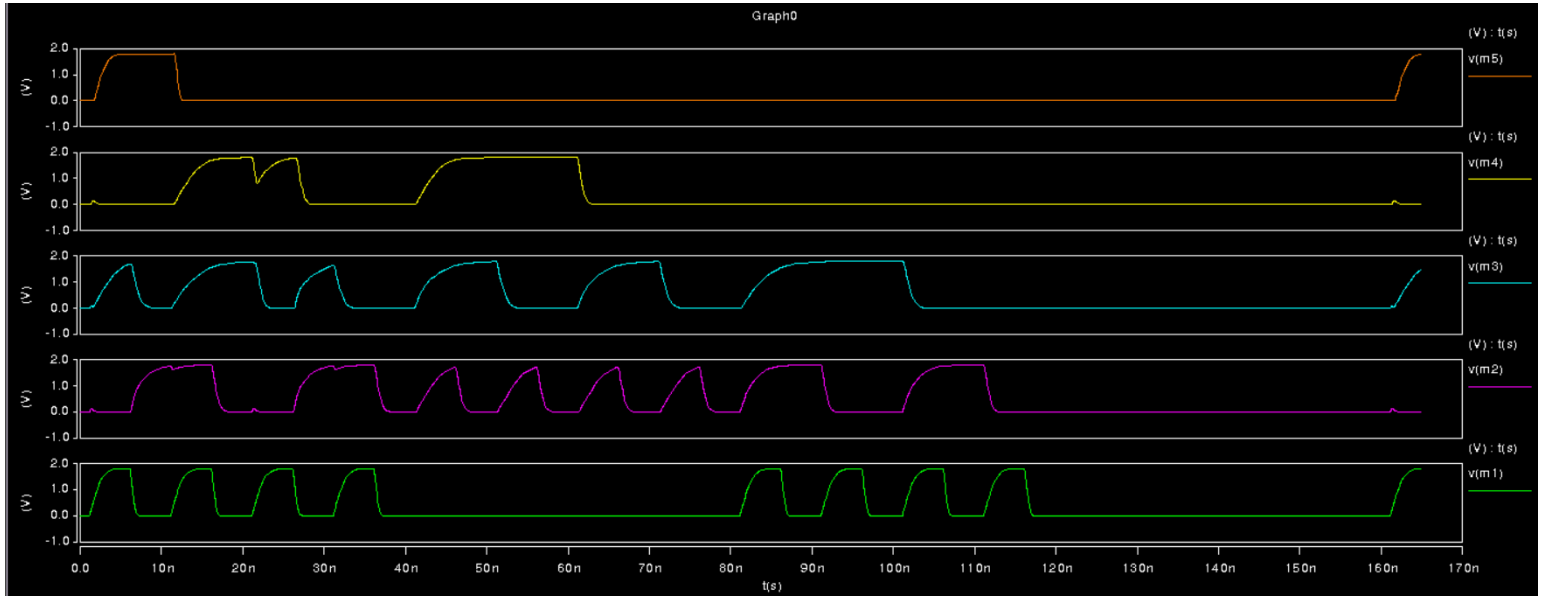


Digital IC Design Practice

- **Results**
  1. ***Layout***
  2. ***Presim & Posim***
     - ***Presim:*** $P_{avg} = 63uW$,$T_{emp} = 27℃$
     - ***Posim:*** $P_{avg} = 75uW$,$T_{emp} = 27℃$
  3. ***Drc & Lvs***

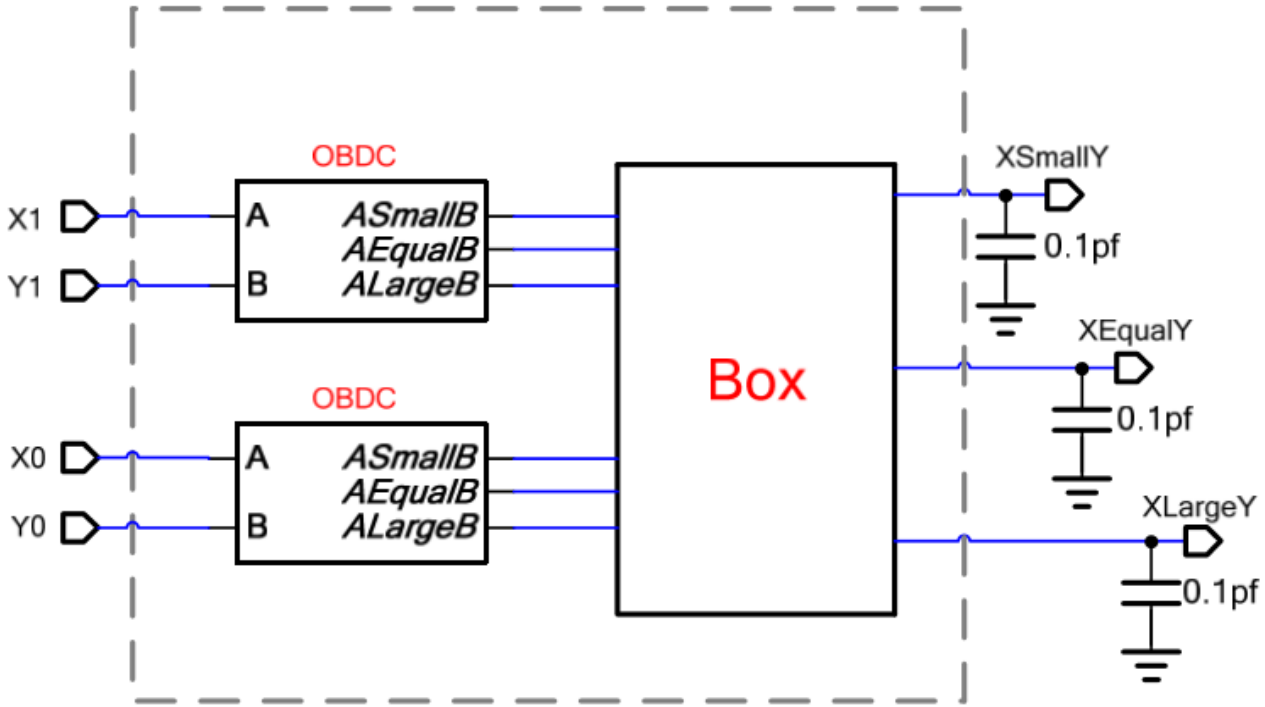




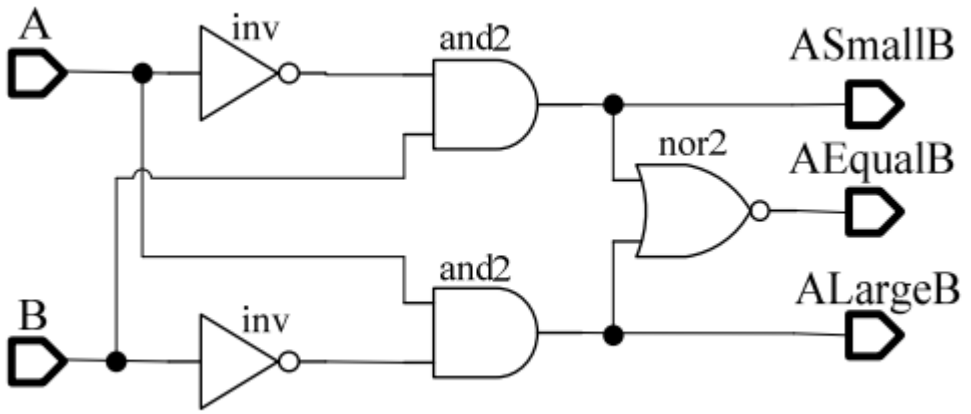


Digital IC Design Practice

Model: 2-Bit Digital Comparator



TBDC內部電路圖



圖三 OBDC 內部電路圖

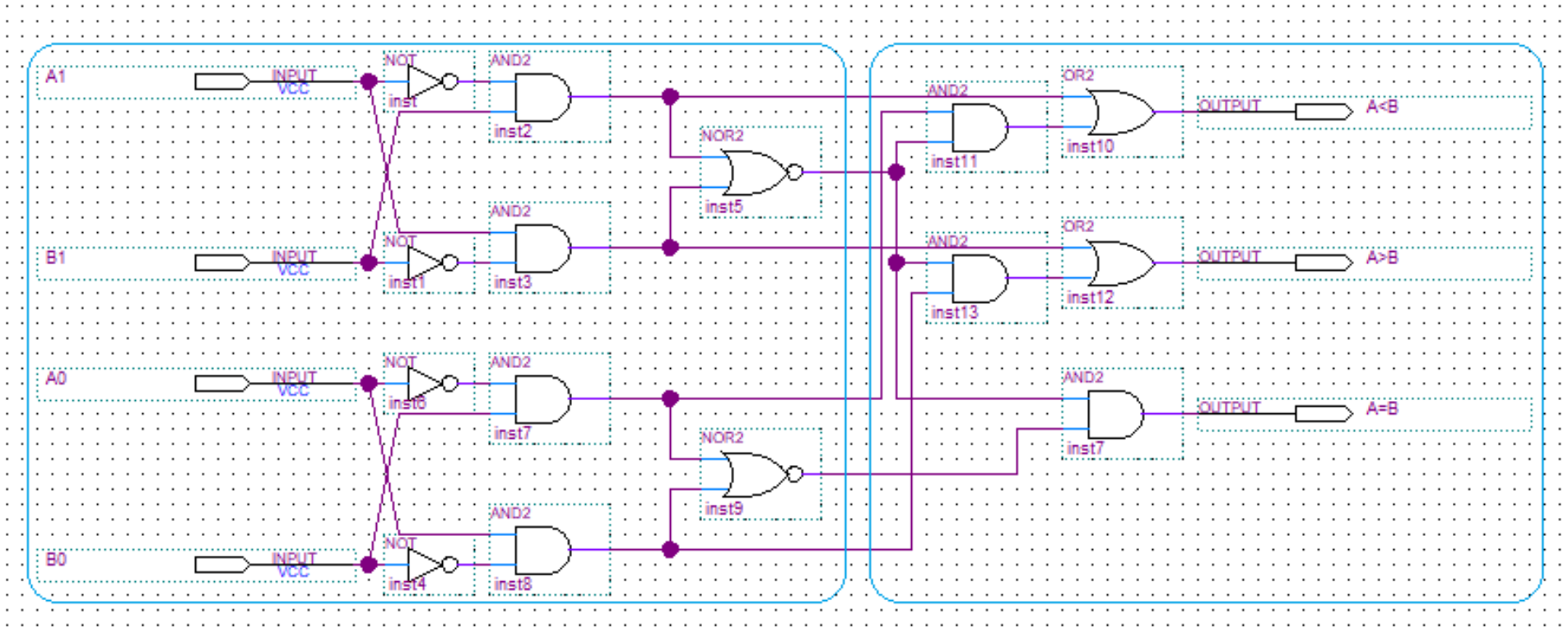
Digital IC Design Practice

比較A1A0與B1B0，高低位元逐次比較。

A<B:(A1<B1) || [(A1=B1) && (A0<B0)]

A>B:(A1>B1) || [(A1=B1) && (A0>B0)]

A=B:(A1=B1) && (A0=B0)



OBDC

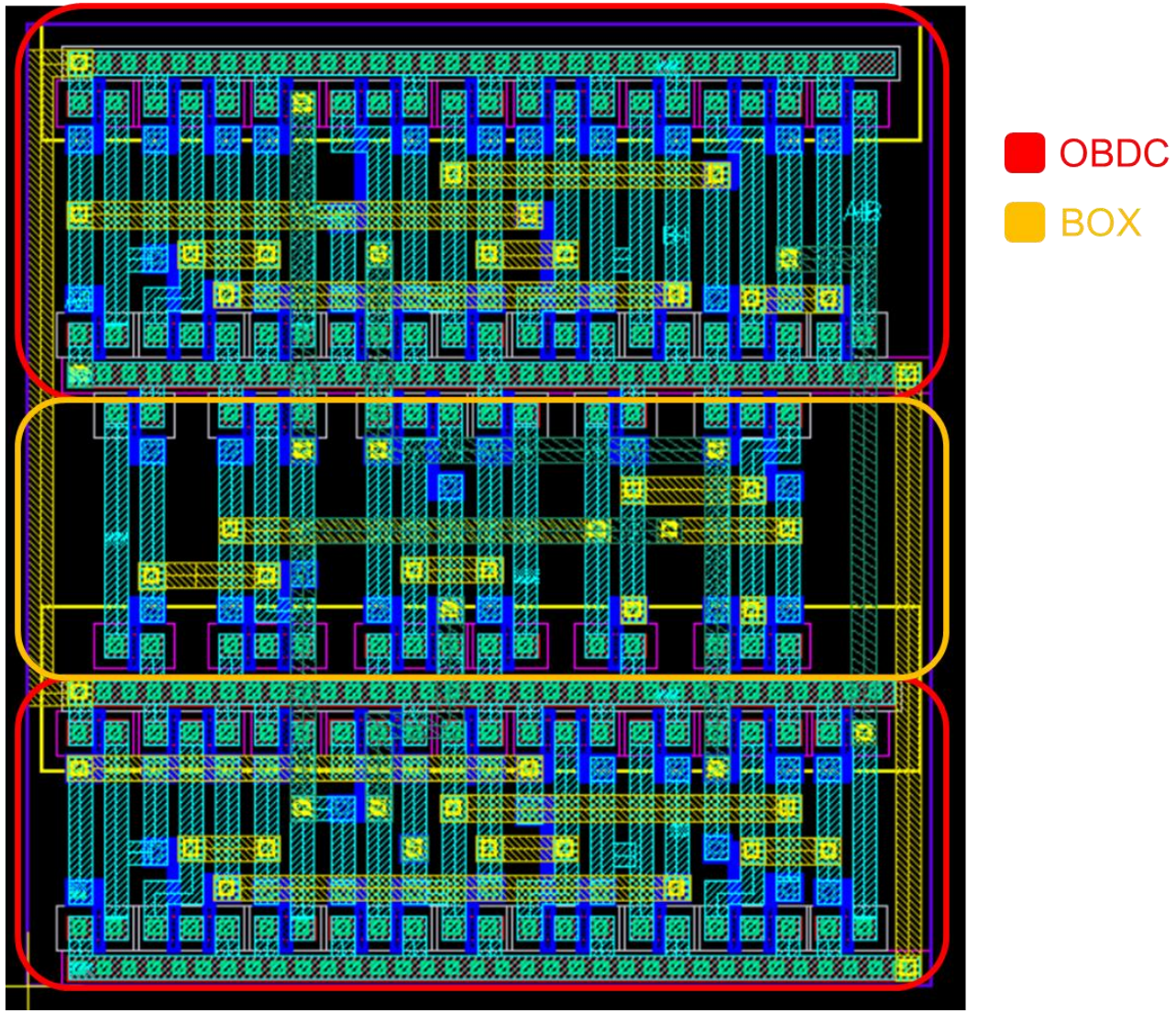
BOX

Digital IC Design Practice

Model: 2-Bit Digital Comparator

- **Hspice**
- **Results**
  1. ***Layout***
  2. ***Posim***

```
.subckt Compare A1 B1 A0 B0 AsB AeB AlB vdd gnd
x1 A1 z vdd gnd / inv
x2 B1  b vdd gnd / inv
x3 A0 f vdd gnd / inv
x4 B0 g vdd gnd / inv
x5 z B1 c vdd gnd / and
x6 A1 b d vdd gnd / and
x7 f B0 h vdd gnd / and
x8 A0 g i vdd gnd / and
x9 c d e vdd gnd / nor
x10 h i j vdd gnd / nor
x11 e h k vdd gnd / and
x12 e i l vdd gnd / and
x13 c k AsB vdd gnd / or
x14 e j AeB vdd gnd / and
x15 d l Alb vdd gnd / or
.ends
```



Digital IC Design Practice

- **Results :*Posim***