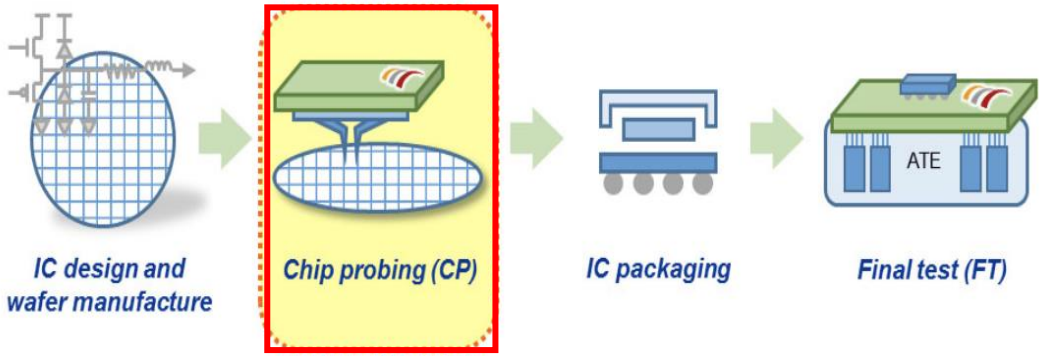
Outline

- Internship — Assistant Test Engineer of Wafer at **KYEC** (***Wafer chip probing***)
- Course Record — Convolution Neural Network, Computer Graphics 3D Rendering (***Algorithm development***)
- Master thesis — Portable Low-Cost Confocal Microscope Based on Pinhole Array and Smartphone (***Image processing by MATLAB and ImageJ***)
- Personality

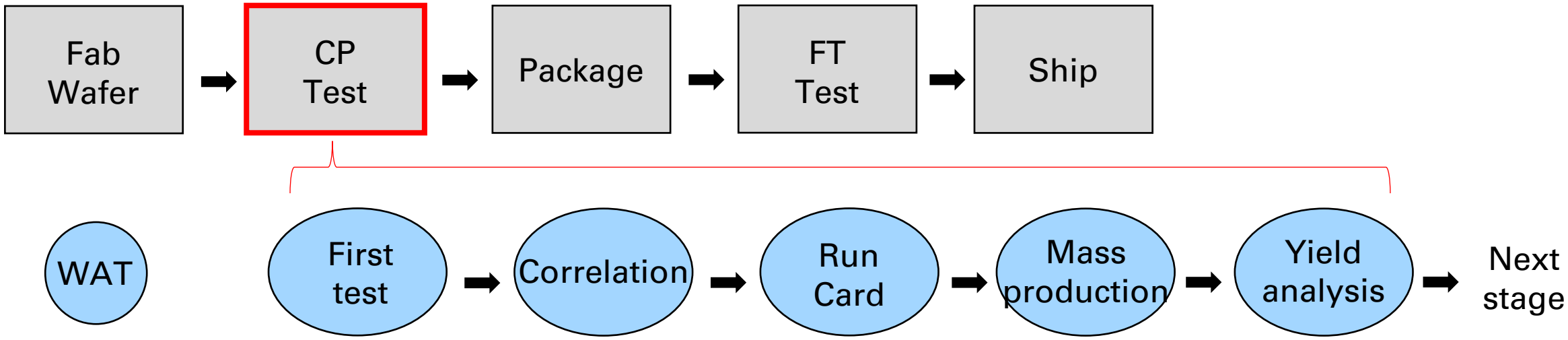
Internship

Wafer chip probing

Semiconductor Industrial chain:



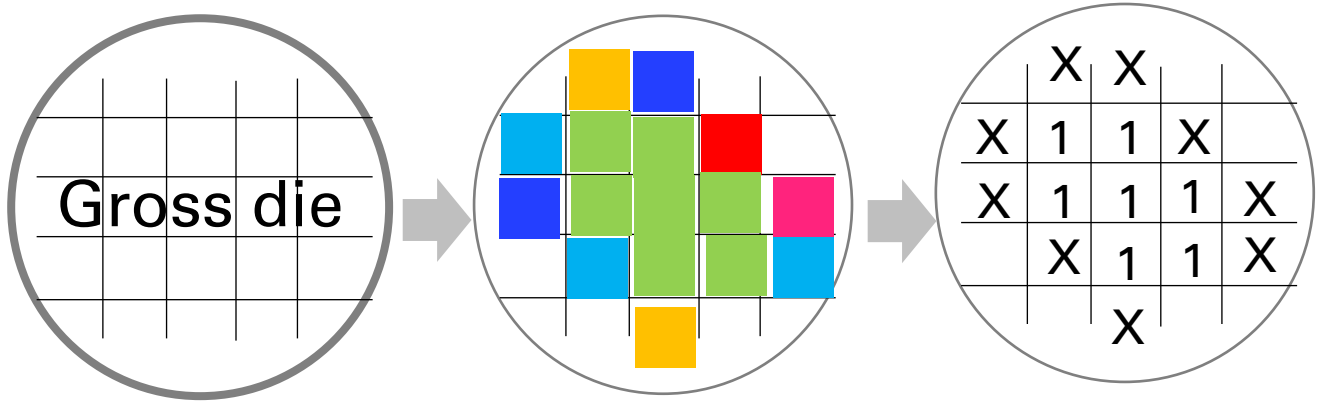
Test flow chart:



Internship

Wafer chip probing

1.Test Program



Soft Bin Wafer Map

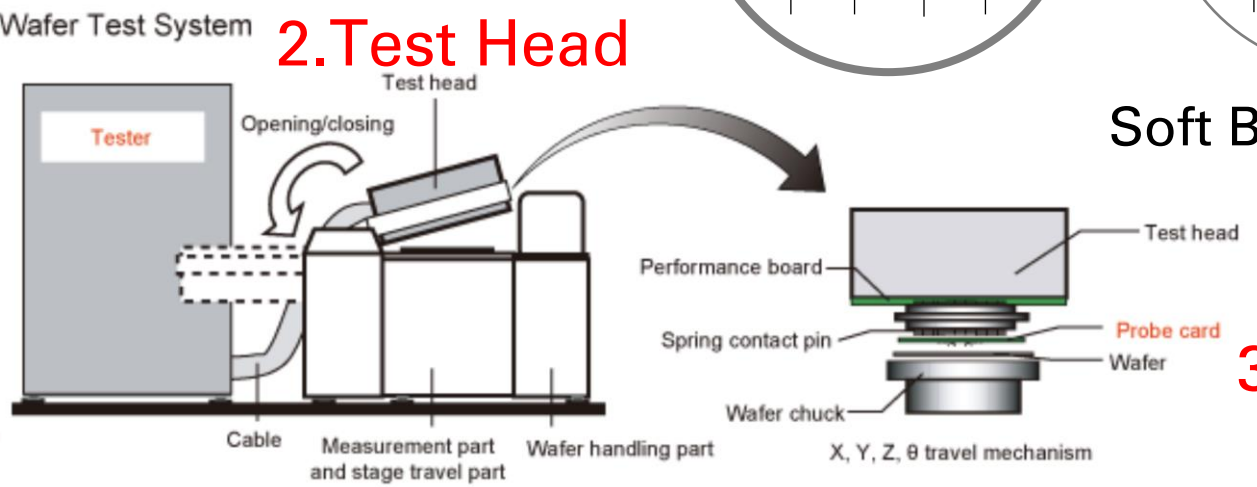
Bin1:PASS
Bin2:Fail function test
Bin3:Fail DC test

Inkless Map

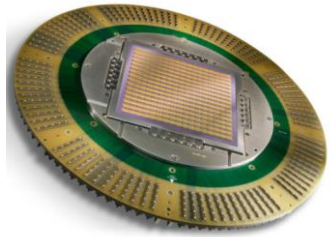
Bin1:PASS die
X: Fail die

2.Test Head

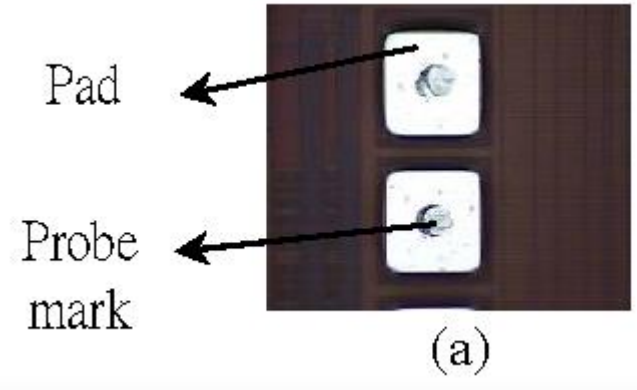
Tester ADVANTEST
: HP93000



3.Probe Card



Probe card



4.Prober

Prober(TSK)
: UF3000-EXE

Internship

Jul. 2020- Jun 2021

Test Plan

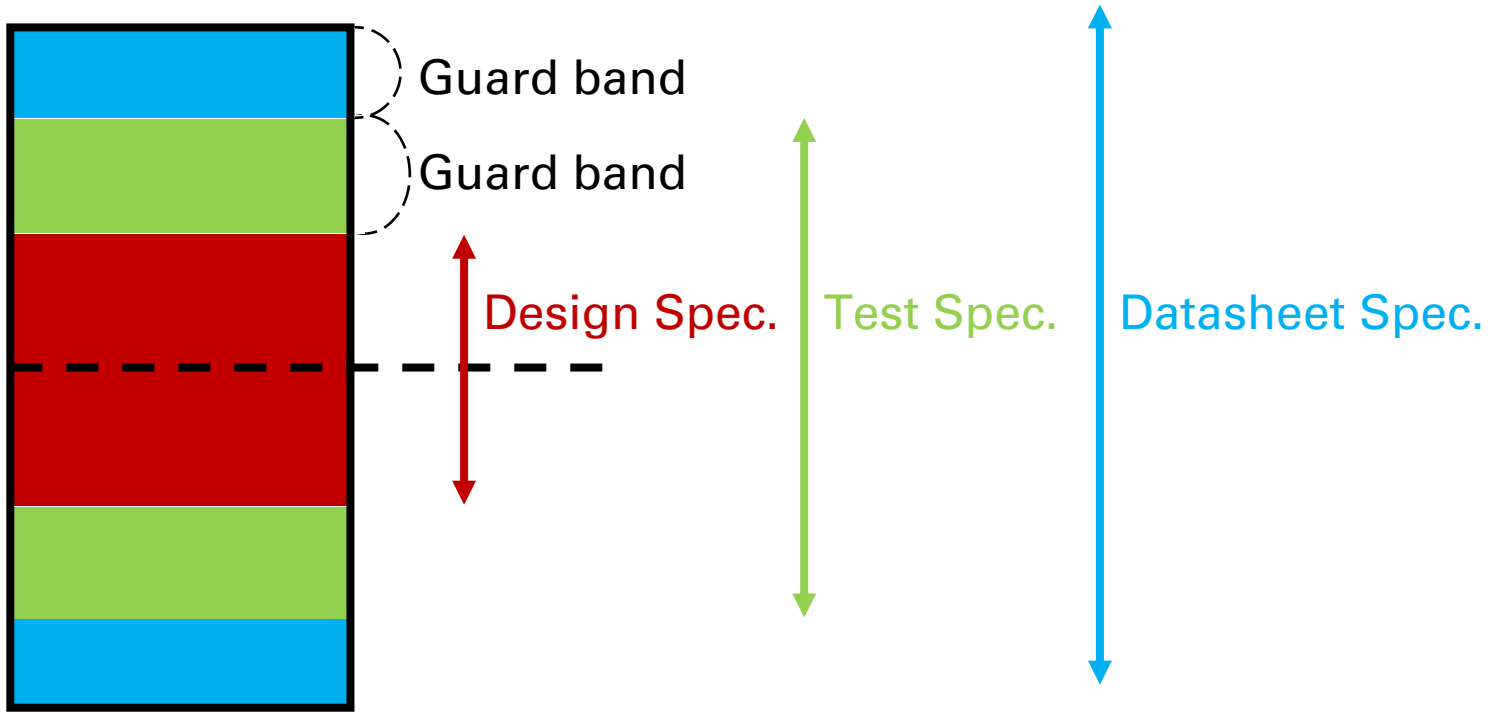
- Test pattern
- Test spec
- DC & AC range limit
- Probe card making

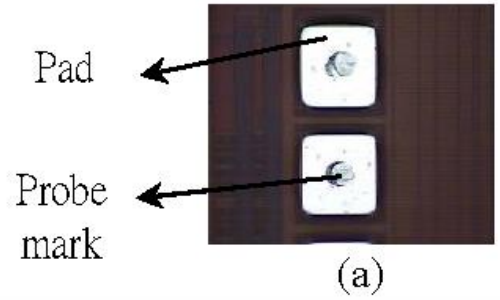
Test program

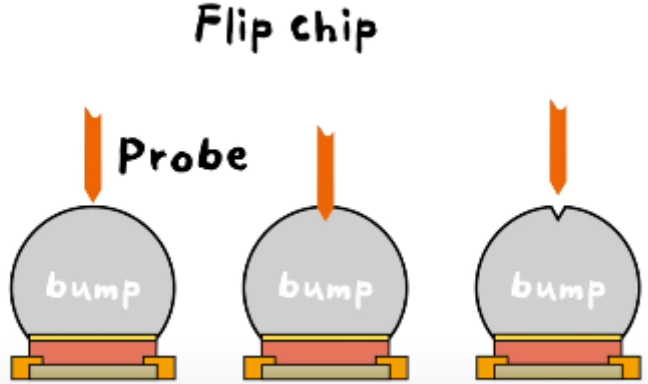
- DC (open/short, power/short)
- Function test.
- AC test.

Data sheet

- Test Temperature
- Wafer PAD or Bump







Internship

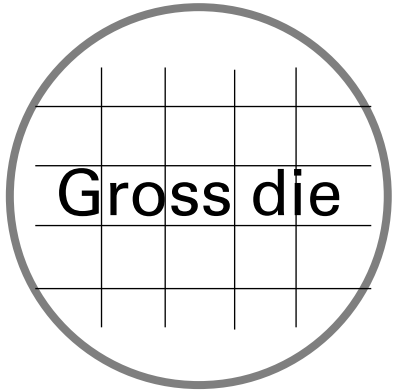
Jul. 2020- Jun 2021

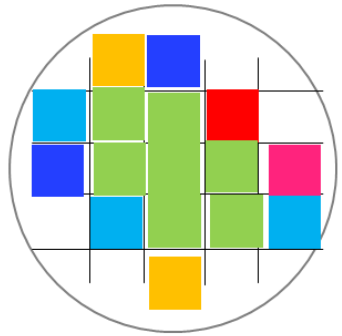
CP test → Release lot to next stage

1. **NPI**
   - Wafer yield and lot yield analysis
   - Release

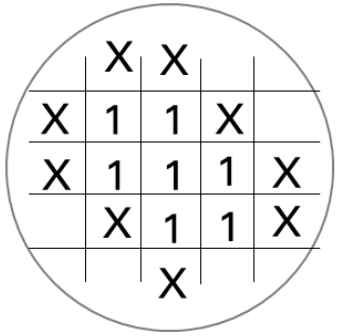
     Equipment & probe card & test program
   - Run Card
2. **Mass production**

   If lot yield is high and no any issue, we will release lot.





Soft Bin Wafer Map



Inkless Map

Verification / Yield analysis

1. Overkill → retest
2. Specific Bin → Clean needle