

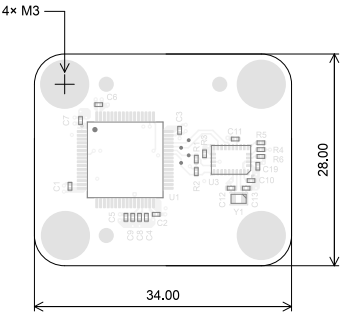
Board Name Fabrication Document

Layer Stack Legend

	Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste				Paste Mask	
	F.Silkscreen				Legend	GBR
	F.Mask		0.02mm	Solder Resist	Solder Mask	GBR
	Copper	L1 (Sig, PWR)	0.035mm (1oz)		Signal	GBR
	Prepreg		0.1855mm	FR4_7628	Dielectric	
	Copper	L2 (GND)	0.035mm (1oz)		Plane	GBR
	Prepreg		1.1mm	FR4	Dielectric	
	Copper	L3 (GND)	0.035mm (1oz)		Signal	GBR
	Prepreg		0.1855mm	FR4_7628	Dielectric	
	Copper	L4 (Sig, PWR)	0.035mm (1oz)		Signal	GBR
	B.Mask		0.02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen				Legend	GBR
	B.Paste				Paste Mask	

Total thickness: 1.651mm  
Note: external layer thicknesses are specified after plating

Top Fabrication (Scale 1:1)



Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0.2032	0.28	L2

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.  
  
DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.  
  
SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 4) SURFACE FINISH: IMMERSION GOLD
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR BLACK.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING YELLOW NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:

A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
B. Tg 170 C OR EQUIVALENT.  
C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY COMPANY.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

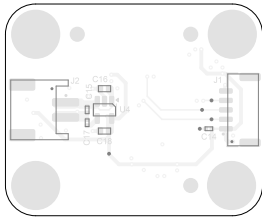
BOARD SIZE34.000 × 28.000 mm  
BOARD THICKNESS1.651 mm  
TRACE WIDTH0.200 mm  
TRACE TO TRACE0.200 mm  
MIN. HOLE (PTH)0.250 mm  
MIN. HOLE (NPTH)N/A mm  
ANNULAR RING0.150 mm  
COPPER TO HOLE0.254 mm  
COPPER TO EDGE0.250 mm  
HOLE TO HOLE0.254 mm
- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

All dimensions are in millimeters unless otherwise specified.

	Comments:	Company:		Variant:	Git Hash:	
		Company Name		CHECKED	866166e	
		Board Name:			Project Name:	
		Board Name			Project Name	
	Sheet Title:	File Name:	Designer:	Date:	Revision:	
Top Fabrication (Scale 1:1)	KiBot_Project_Test.kicad_pcb	Author	2024-04-13	+ (Unreleased)		
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Board Name Fabrication Document

Bottom Fabrication (Scale 1:1)



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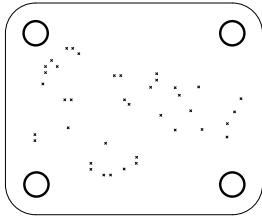
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		KiBot_Project_Test.kicad_pcb	Author	2024-04-13	+ (Unreleased)
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Board Name Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
X	39	0.25mm (9.84mils)	PTH	Round	L1 (Sig. PWR) - L4 (Sig. PWR)	Via
O	4	3.20mm (125.98mils)	PTH	Round	L1 (Sig. PWR) - L4 (Sig. PWR)	Pad
	Total 43					

Drill Drawing L1 - L4 (Scale 1:1)

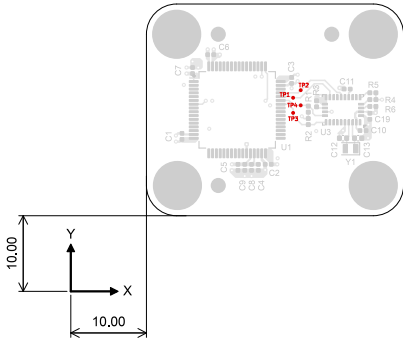


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		KiBot_Project_Test.kicad_pcb	Author	2024-04-13	+ (Unreleased)
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Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
TP1	IMU_INT	29.40	25.60
TP2	IMU_RESET	30.40	26.60
TP3	I2C2_SDA	29.40	23.60
TP4	I2C2_SCL	30.40	24.60



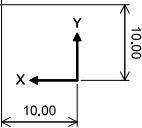
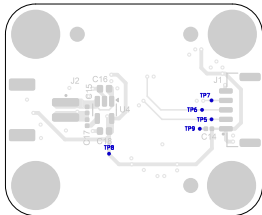
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# Board Name Fabrication Document

Bottom Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
TP5	SWDIO	16,75	22,75
TP6	SWCLK	18,00	24,00
TP7	NRST	16,75	25,25
TP8	+3V3	30,30	18,20
TP9	GND	18,30	21,50

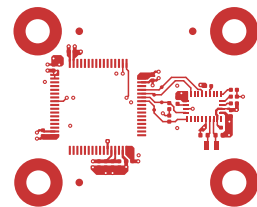


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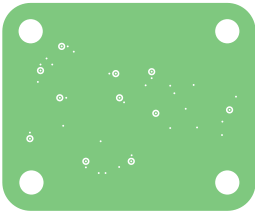
L1 (Sig, PWR) (Scale 1:1)



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Board Name Fabrication Document

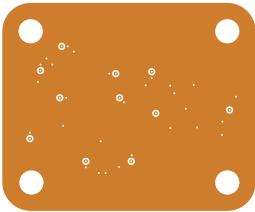
L2 (GND) (Scale 1:1)



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	L2 (GND) (Scale 1:1)	KiBot_Project_Test.kicad_pcb	Author	2024-04-13	+ (Unreleased)
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L3 (GND) (Scale 1:1)

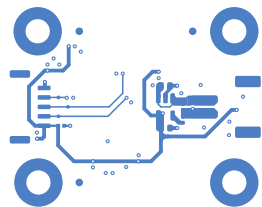


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L4 (Sig, PWR) (Scale 1:1)



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			File Name: KiBot_Project_Test.kicad_pcb	Designer: Author	Date: 2024-04-13	Revision: + (Unreleased)
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