FPGA Design for PCANet Deep Learning Network

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***Abstract*—In recent years, deep learning has attracted lots of research interests for pattern recognition and artificial intelligence. PCA Network (PCANet) is a simple deep learning network with highly competitive performance for texture classification and object recognition. When compared to other deep neural networks such as convolutional neural network (CNN), PCANet has much simpler structure, which makes it attractive for hardware design on an FPGA. In this paper, an efficient, high-throughput, pipeline architecture is proposed for the PCANet classifier. The implementation on an FPGA is more than 1,000 times faster than software execution on a general purpose processor. When evaluated using the MNIST handwritten digits dataset, the PCANet design results an accuracy of about 99.46%.**

***Index Terms*—Deep Learning, PCANet, FPGA, MNIST**

I. PCANet Structure

Deep learning networks are able to discover multiple levels of representations of a target object [1]. When compared to other deep neural networks such as convolutional neural network, the recently introduced PCA network (PCANet) has much simpler structure [2]. The PCANet architecture mainly consists of the following components: patch-mean removal, PCA filter convolutions, binary quantization and mapping, block-wise histograms, and an output classifier. We choose a linear support vector machine (SVM) as the classifier. Note that this work is focused on the implementation of PCANet classifier and the training procedure is not implemented in hardware. Coefficients of the PCA filters and SVM classifier are pre-trained offline using dataset from the target application.

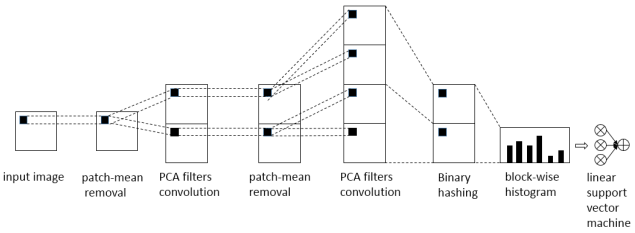

Figure 1. General structure of PCANet deep learning network

II. Result

The PCANet has been proved to be effective when applied on several image classification tasks [3]. In this paper, we evaluate the PCANet using MNIST dataset. MNIST database contains handwritten digits from 0 to 9. Example images from the database are shown in Fig. 2. Some digits are not positioned upright, which makes them harder to be recognized. The proposed PCANet design results an accuracy of about 99.46%.

Figure 2. Examples of number digits from MNIST Dataset

The hardware design is target on a Xilinx Virtex-7 980T FPGA. For the pipeline architecture, it takes about 1,800 clock cycles to produce the final result for an input image. The FPGA synthesis yields a maximum frequency of 237.2MHz. Thus, it only takes 7,588 ns to process an image, which is equivalent to a frame rate 131,790 frames per second (fps). We also develop the C code of the PCANet on a 2.4GHz Quad-Core i7 CPU. It takes 0.012 second for the CPU to process a single frame, which is equivalent to a frame rate of about 83 fps. By comparison, the FPGA design achieves a speedup of 1,582 over the CPU. If considering the pipeline delay, the absolute response time is 2,913 clock cycles, which is about 12.28 us. The resource usage of our PCANet implementation is listed in Table I. We have used almost all available DSP resources on a large FPGA. In the future work, we will reduce the utilization of DSP slices through trade-off between throughput and hardware resource usage.

Table I
FPGA resource usage of PCANet implementation

	Used	Available	Utilization
Slice Registers	358848	1224000	29%
Slice LUTs	265460	612000	43%
RAMB36E1	64	1500	4%
RAMB18E1	9	3000	1%
DSP48E1s	3599	3600	99%

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978-1-4799-9969-9/15 $31.00 © 2015 IEEE
DOI 10.1109/FCCM.2015.45