Lab Programming Assignment #1

Points Possible: 20

Due Date: Sunday, February 9 by 11:59 pm

Instructions:

Submit just one file: **Programming Assignment 1-<Name of Submitter>.txt**. Example: Programming Assignment 1-John Doe.txt assuming John Doe is the person submitting the file on BeachBoard. Only submission via BeachBoard will be accepted.

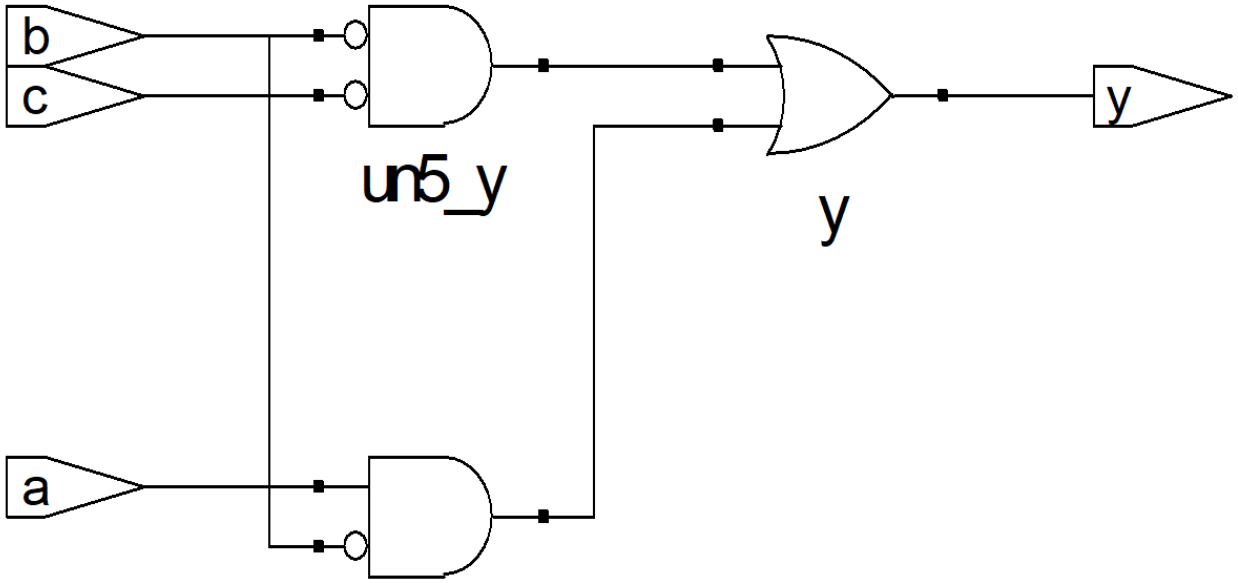
In addition, as a comment at the top within your code, provide the EDA Playground URL for your saved code, so that I can directly access and execute it.

Be sure to also type in your name within the file, at the top as a comment.

Failure to do any of the above will result in point deductions. No exceptions.

Requirements:

Note the following logic circuit:



It can be simulated using the following Verilog Design code:

```
module example(a, b, c, y);
        input a, b, c;
        output y;
        assign y = (~b & ~c) | (a & ~b);
endmodule
```

Using the EDA Plaground, create its corresponding test bench such that you can test three inputs and see its output. Both the input variables and the output should be displayed in the console. Example console output of what I expect to see is:

```
testbench.sv:4: warning: Some modules have no timescale. This may cause
testbench.sv:4:        : confusing timing results.  Affected modules are:
testbench.sv:4:        :   -- module example declared here: design.sv:3
a = 0
b = 0
c = 1
y = 0
Done
```

Place your code in a text file and also include the URL for the code within the file (as a comment), per the instructions above.