CECS 225 – Spring 2020

Lab Programming Assignment #3

Points Possible: 20

Due Date: Wednesday, March 11 by 11:59 pm

Instructions:
Submit two files (do not zip them):
Programming Assignment 3-<Name of Submitter>-Design.txt
Programming Assignment 3-<Name of Submitter>-Testbench.txt.

Only submission via BeachBoard will be accepted.

In addition, as a comment at the top within your code for each file, provide the EDA Playground URL for your saved code, so that I can directly access and execute it.

Be sure to also type in your name within each file, at the top as a comment.

Failure to do any of the above will result in point deductions. No exceptions.

Requirements:

Consider the following Boolean equation:

$$Y = \overline{A}\,\overline{C} + A\overline{B} + AC$$

Using the EDA Playground, create its corresponding design and test bench. Test all possible truth table cases in your test bench and output the results. Submit both the design and test bench, each being in separate text files (see the instructions above for further details).

Note: You should only use three registers and one wire in your code.

Example console output of what I expect to see is the following (note that the below only shows three test cases, whereas I expect to see all eight test cases):

```
[2020-03-01 21:13:50 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp
a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:        : confusing timing results.  Affected modules are:
testbench.sv:3:        :   -- module equation declared here: design.sv:2
VCD info: dumpfile dump.vcd opened for output.
Test Case 1
a = 0
b = 0
c = 0
y = 1
Test Case 2
a = 0
b = 0
c = 1
y = 0
Test Case 3
```

Instructor: Ali Sharifian

```
a = 0
b = 1
c = 0
y = 1
```