CECS 225 – Spring 2020

Lab Programming Assignment #2

Points Possible: 20

Due Date: Sunday, February 23 by 11:59 pm

Instructions:

Submit a zip file containing two files within it:
Programming Assignment 2-<Name of Submitter>-Design.txt
Programming Assignment 2-<Name of Submitter>-Testbench.txt.

Zip file name should be **Programming Assignment 2-<Name of Submitter>.zip**

Only submission via BeachBoard will be accepted.

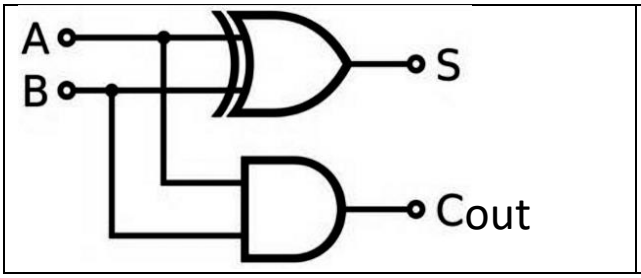
In addition, as a comment at the top within your code, provide the EDA Playground URL for your saved code, so that I can directly access and execute it.

Be sure to also type in your name within the file, at the top as a comment.

Failure to do any of the above will result in point deductions. No exceptions.

Requirements:

The following logic circuit is for a half adder:



S = A xor B

Cout = A and B

Using the EDA Playground, create its corresponding design and test bench. Test all possible truth table cases in your test bench and output the results. Submit both the design and test bench, each being in separate text files (see the instructions above for further details).

Example console output of what I expect to see is the following (note that the below only shows one test case, whereas I expect to see all four test cases):

```
[2020-02-09 01:17:01 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp
a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:        : confusing timing results.  Affected modules are:
testbench.sv:3:        :   -- module halfadder declared here: design.sv:2
VCD info: dumpfile dump.vcd opened for output.
Test Case 1
a = 0
b = 0
```

```
s = 0
cout = 0
```