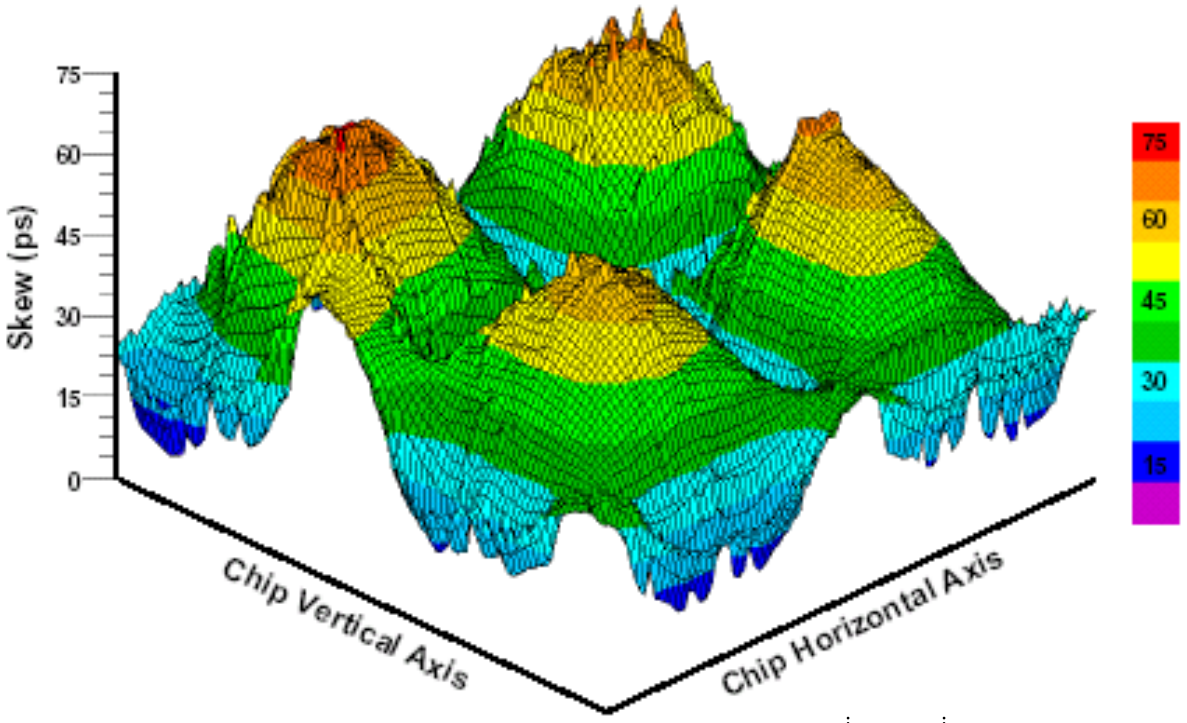
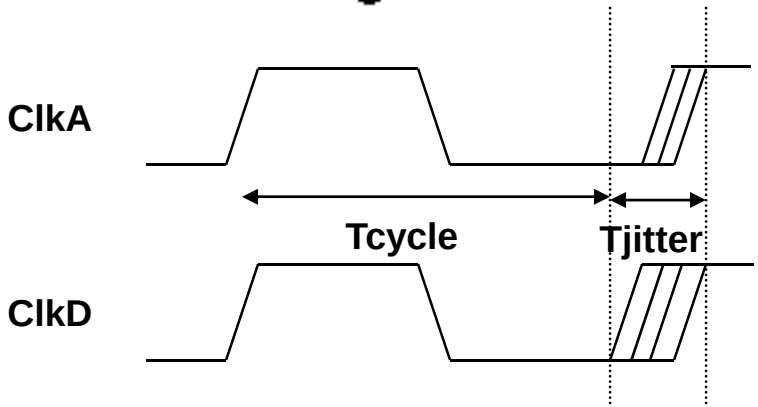
EE 382M

VLSI–II

Global Clocking





Héctor Sánchez
Mark McDermott

Class Agenda

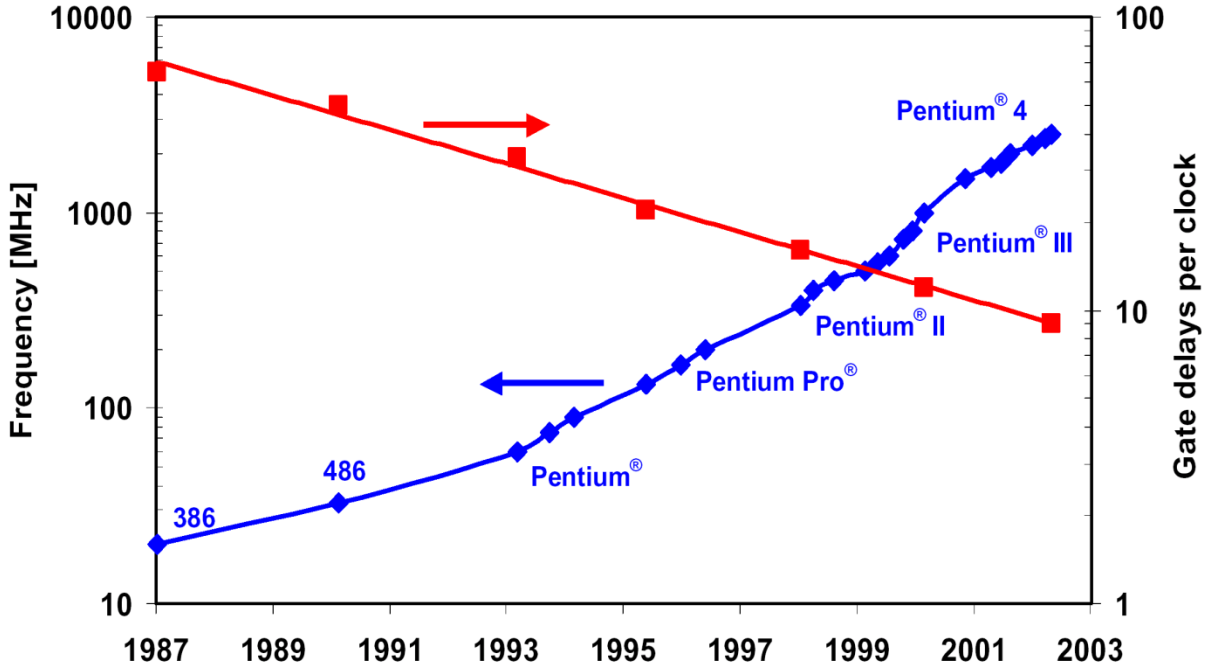
- Clocking Overview
- Clock Generation
- Clock Distribution
- Clock Uncertainty
  - Clock Skew
  - Clock Jitter
- Clock Regeneration
  - Tunable global clock buffers
  - Local clock buffers
- Clocking with SOI Technology
- Key learning's
- Future Clocking Issues

Clocking Overview

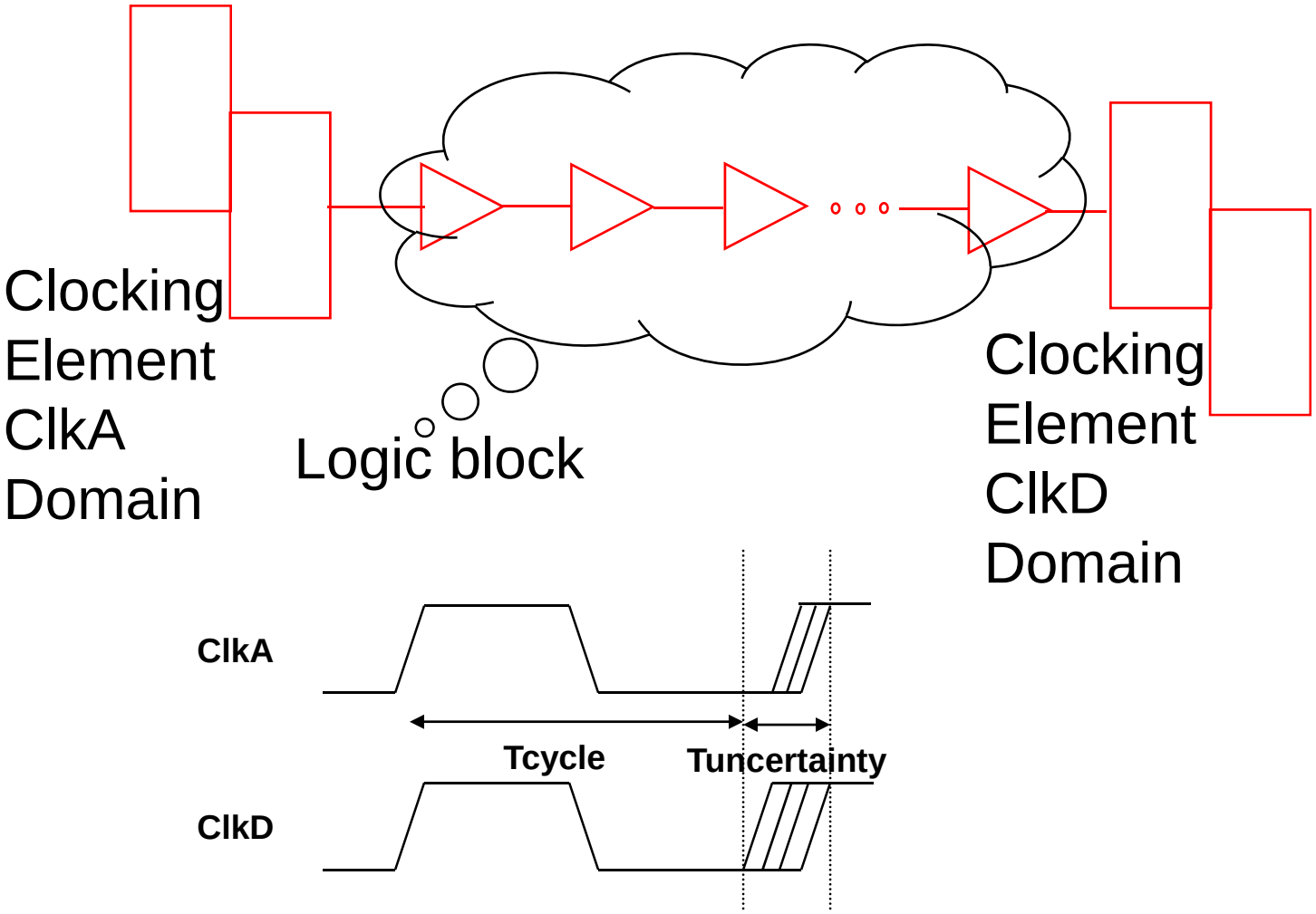
- Most high speed digital systems use clocks to synchronize data transactions.
- The maximum clock frequency determines the rate at which the data can be processed.
- The clocking style is dependent on the circuits used to implement the logic elements and storage elements.
- There are three main components to clocking:
  - Generation: Crystal Oscillators, PLLs or DLLs.
  - Distribution: Trees, grids, etc.
  - Re-generation: LCB, GCB

Clocking Overview

- There are a number of issues with clocking a high performance digital system. These include:
  - Clock uncertainty: skew and jitter.
  - Frequency dependent failures
  - Frequency independent failures.
  - Clock Distribution Power



Logic Transactions and CLK Dependence



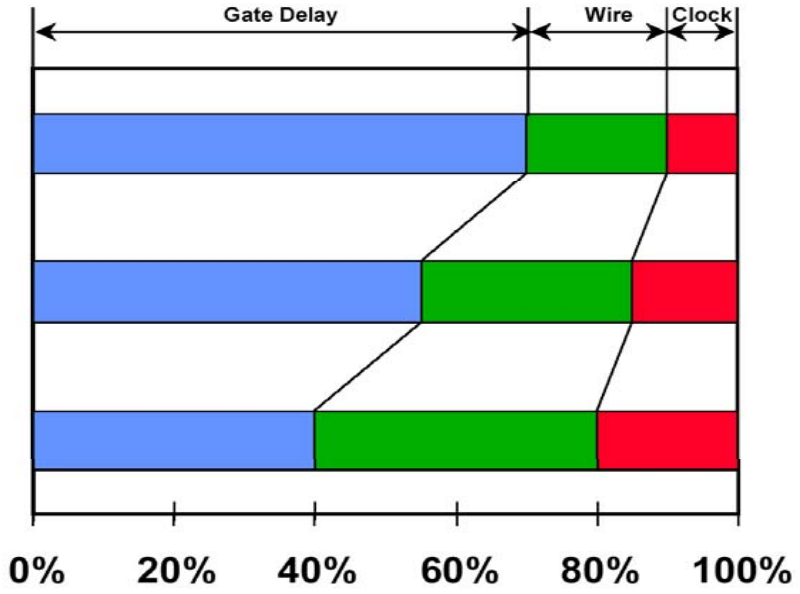
Skew and Jitter: Definition

- Skew and Jitter are the enemy of a clocking system.
- Skew is the “static” time difference between any 2 electrical nodes.
  - Typically with reference to clock signals that should in theory switch simultaneously.
  - There are techniques to reduce or eliminate skew.
  - Skew can be “managed” to your advantage (i.e. intentional skew can be used to provide “cycle-stealing” capability)
- Jitter is a “dynamic” time difference of a signal with respect to an ideal signal.
  - Jitter can not be typically “designed-out”.
  - Jitter can result from various time-dependent noise events.

Clocking Overview

- **Clocking overhead (skew and jitter) is growing as we move to nanometer processes. Careful design of the clock generation and distribution circuits is now required for all high performance processor designs.**

Process	*Frequency*	*Inv/Cycle*
0.5u	250MHz	>20
0.18u	1.5GHz	~14
0.06u	8.0GHz	~8



Source: D. Luick, "Beyond Superscalar RISC", ISSCC'98

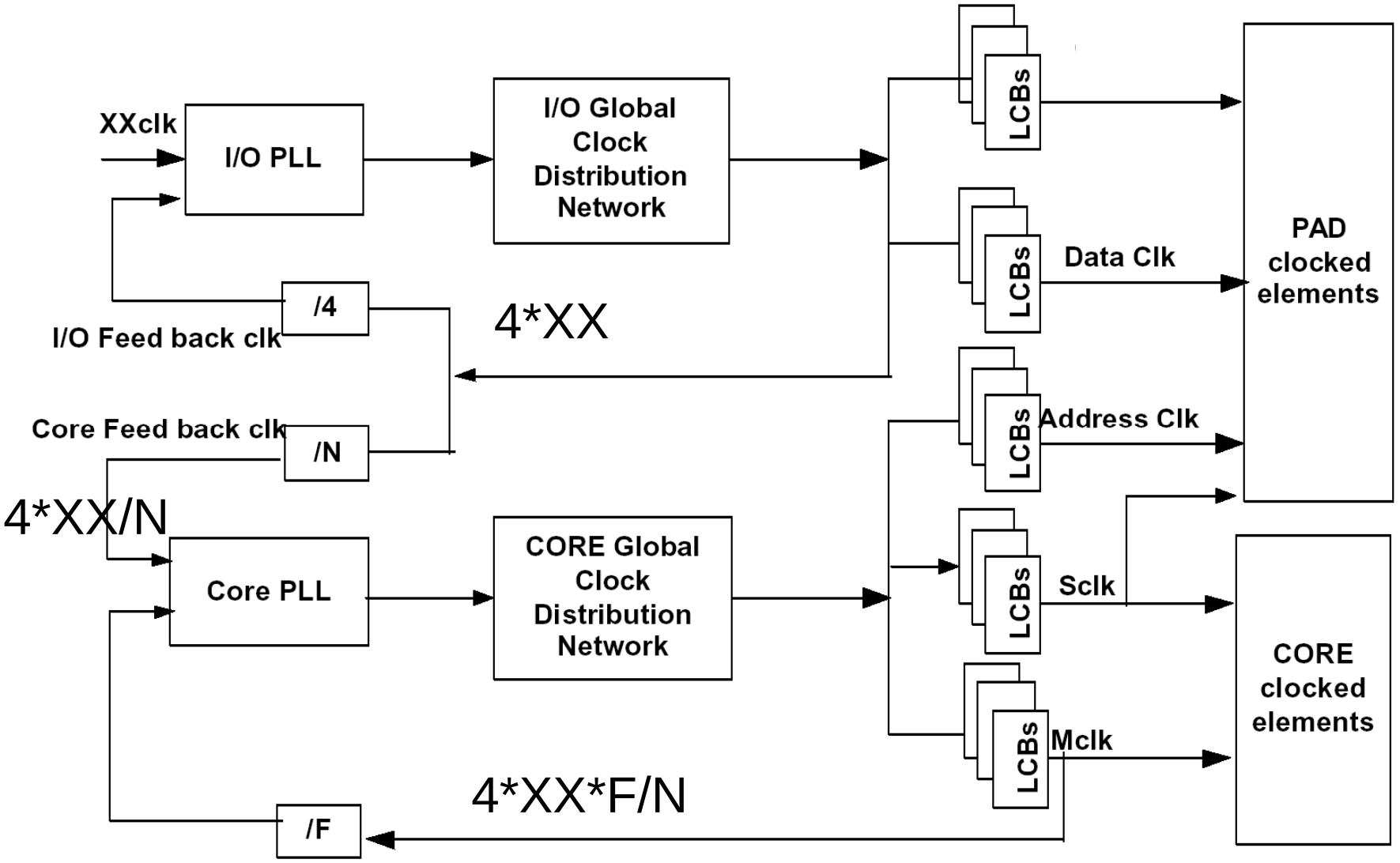
Clock Generation

- There are two techniques used to synchronize the clocks in a high performance system: Phase Locked Loop (PLL) or a Delay Locked Loop (DLL)

- The PLL is used to "phase" synchronize (and probably multiply) the system clock WRT to a reference clock (internal or external).
  - PLL features:
    - Frequency Multiplication to run processor at faster speed than memory interface.
    - Skew reduction. The reference clock is "aligned" to the feedback clock.
    - Possible "stability" issues with PLL due to 2nd or 3rd order loop behavior.

- The DLL is used to "delay" synchronize the system clock to a reference clock.
  - DLL Features:
    - DLL's typically do not multiply an input clock, although high performance DLL's have been designed to implement limited frequency multiplication.
    - DLL's are inherently stable. Think of "only" trying to align delay not delay and frequency as in a PLL.
- Some high performance systems use a combination of both to generate the various clocks in a multiple clock domain design.
  - SOC designs can have many multiple frequency clock domains.

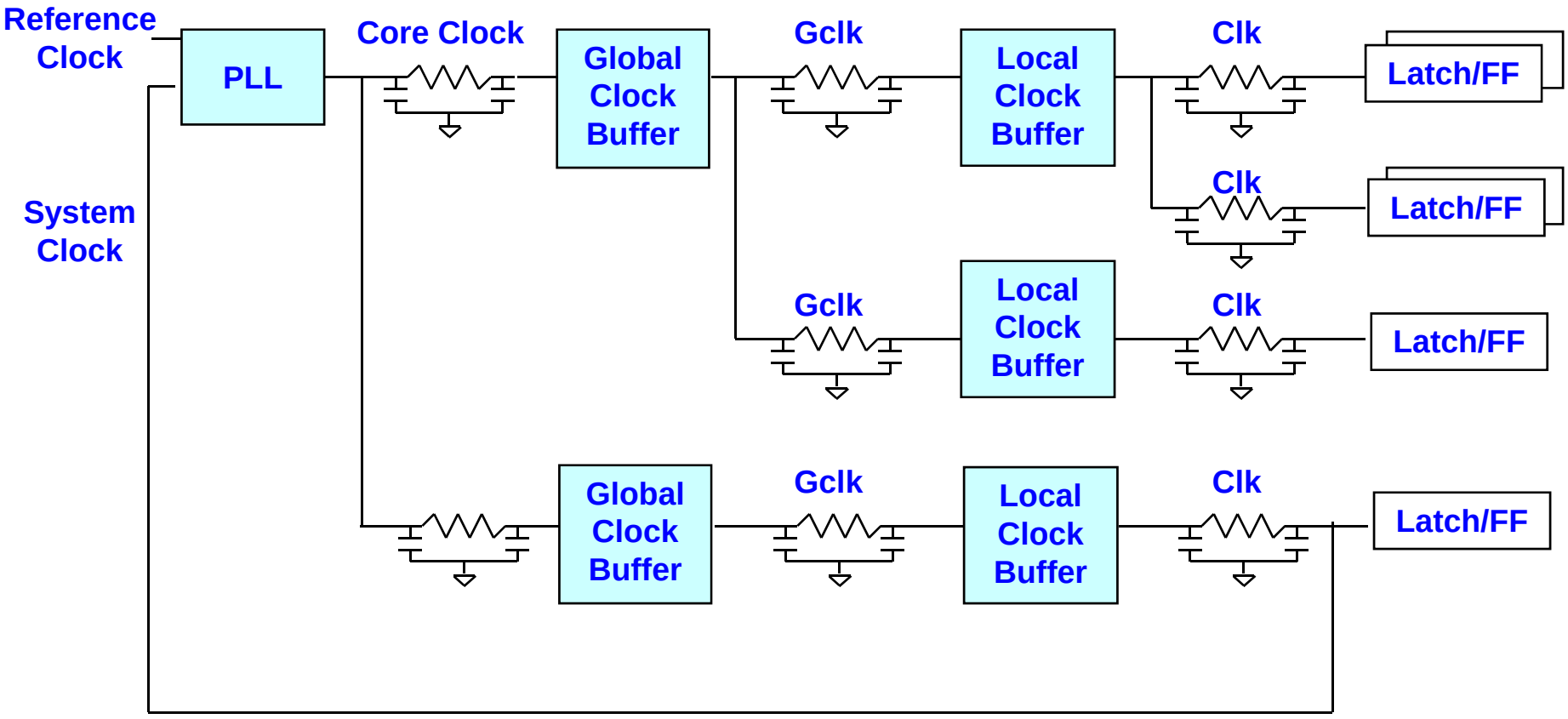
High Performance Processor Clock Network



Clock Distribution

- Clock distribution is one of the most critical areas in the design of high performance VLSI chips.
  - Poor clock distribution can result in excessive clock skews between clusters on the chip, reducing the maximum operating frequency.
- In general we need to reduce the effect of clock skew on the chip. This requires:
  - Reducing the wire delay and RC effects by making the effective delay small and balancing the delays of all the paths. (This changes a total delay problem to a matching delay problem.)
  - Matching the clock buffer delay
  - Reducing the process variations sensitivities by careful placement and design of the of clock buffers.
- A side effect of long clock distribution delays is increased jitter due to supply voltage variations. This adversely affects the PLL used to generate the chip clock frequency.

Schematic of a typical clock distribution tree



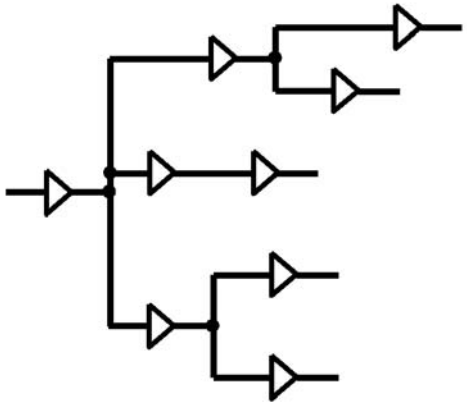
Clock Distribution

- There are four basic types of clock distribution networks used in high performance processor designs:
  - Tree: IBM and Motorola Power-PC, HP PA-RISC
  - Grid: SPARC, Alpha
  - Serpentine: Pentium-III
  - Spine: Alpha, Pentium-4
- Each technique has advantages and disadvantages:

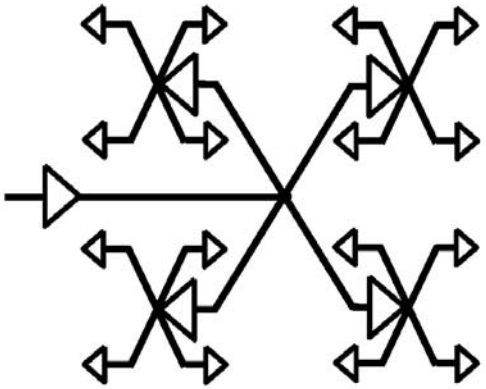
	Wire Cap	Delay	Skew
Grid	High – 15x	Low – sub100 ps	Low-Med
Trees	Low – 1x	High – 100's ps	Low
Serpentine	Very High – 30x	High – 100's ps	Low
Spine	High – 10x	Low-sub100ps	Med

Variations of tree distribution networks

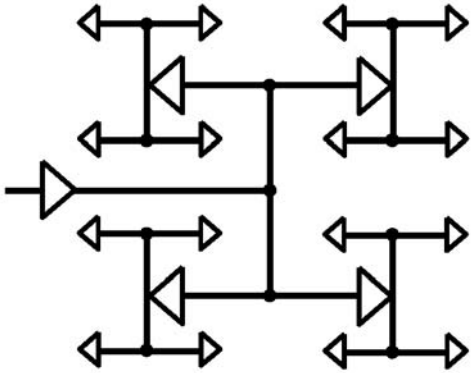
Target: Metallization and Gate topology uniformity



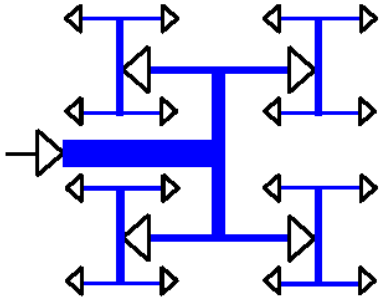
Tree



X-Tree



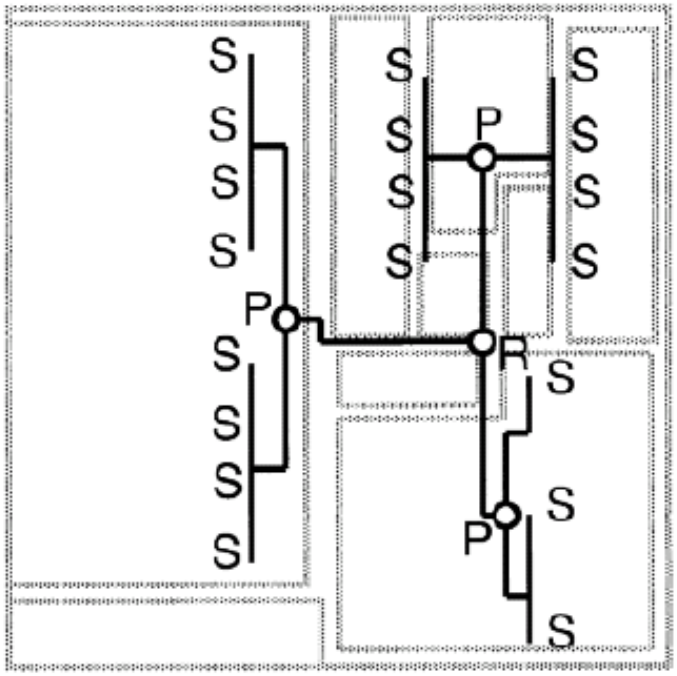
H-Tree



Tapered H-Tree

HP PA-RISC Clock Distribution

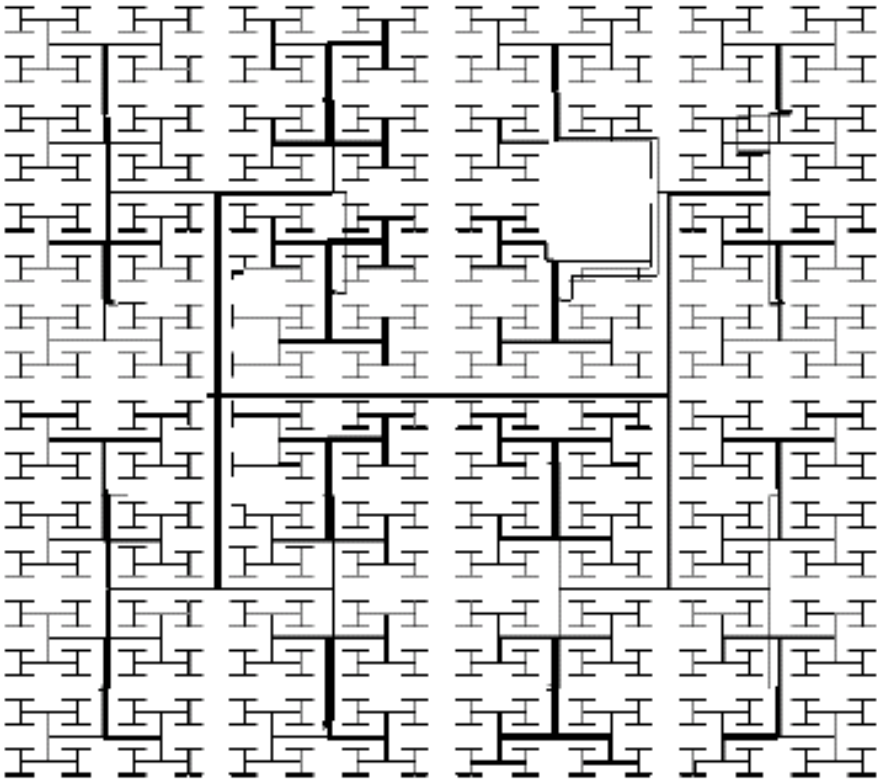
- Plan the clock usage points to minimize the distribution area
- Large caches do not require the clock to be distributed over them
- Example from the HP RISC design:
  - 1 Receiver Buffer (R)
  - 3 Primary Buffers (P)
  - 19 Secondary Buffers (S)
  - Balanced Tree Distribution
  - Die Size 21.3 x 22.0 mm



Source: P. Barnes, A 500MHz 64b RISC CPU with 1.5MB O`n-Chip Cache, ISSCC'99

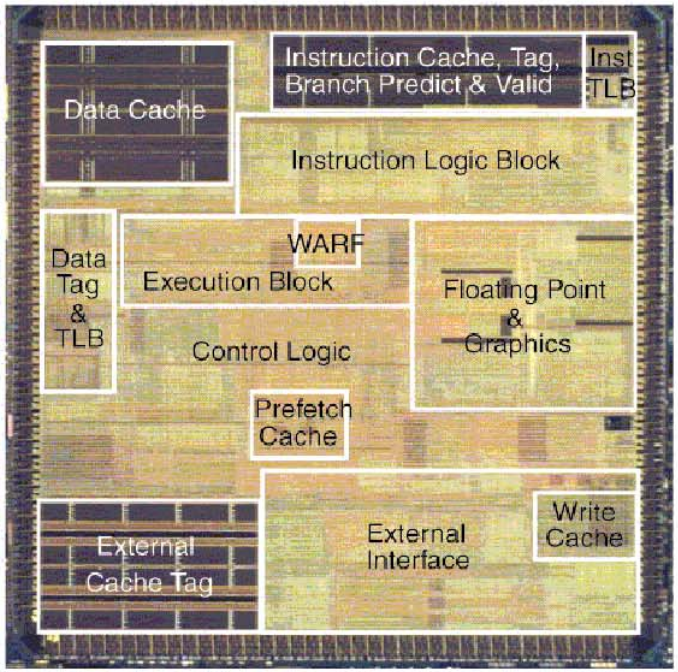
IBM PowerPC Clock Distribution

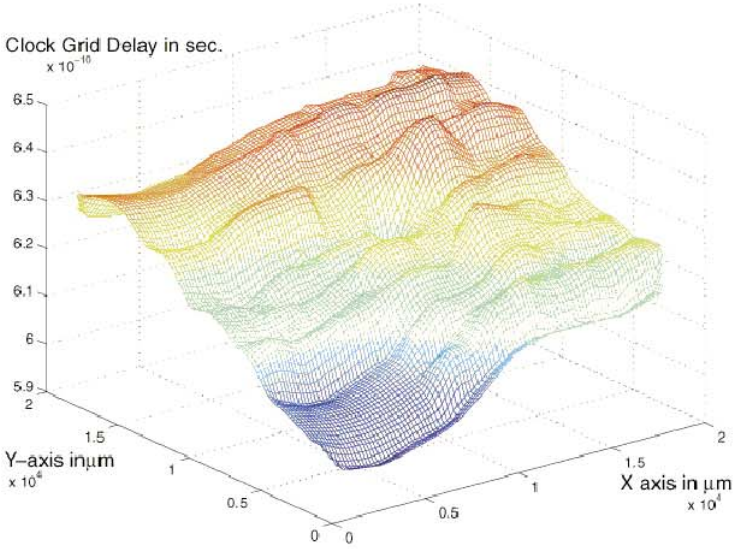
- 0.22µm technology
- 17mm x 17mm die size
- 19M transistors
- 6 level metal with copper interconnect technology
- Clock tree on top 2 metal levels
- 1 GHz clock frequency
- Almost symmetric H-tree
- Simulated clock skew under 15ps



Source: A 1GHz single-issue 64b PowerPC processor, ISSCC'2000

Sun Microsystems UltraSparc III



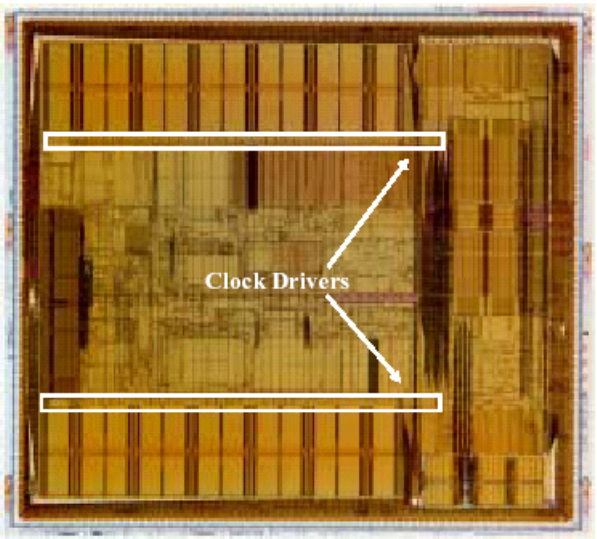


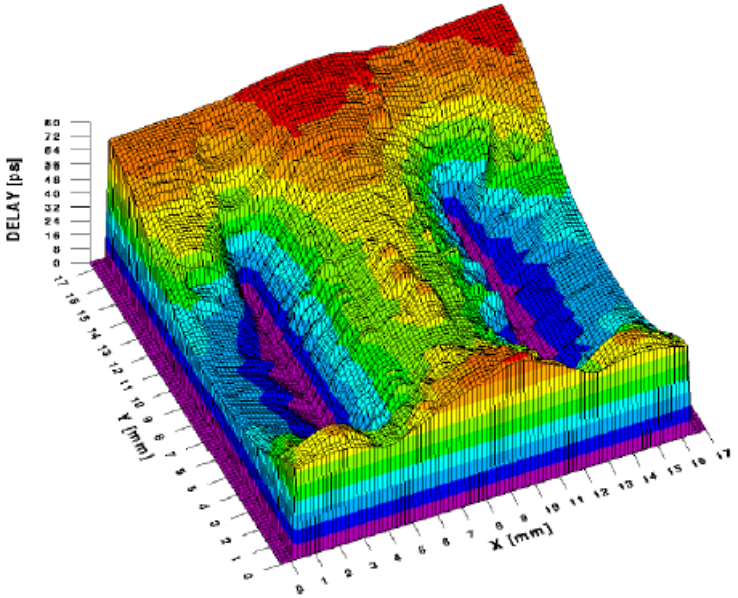
- 15.0 x 15.5 mm die size, 23M transistors
- Overall clock skew <80ps

DEC Alpha 21164 Clock Distribution

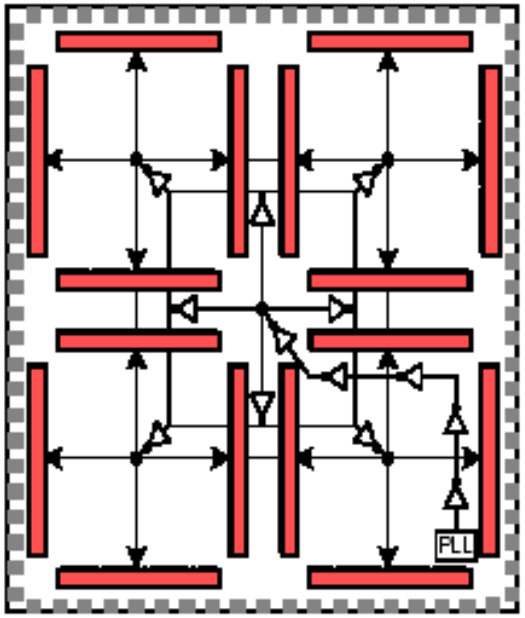
- Clock Frequency: 300MHz
- 9.3 Million transistors
- Total Clock Load: 3.75nF
- Power in Clock Distribution network: 20W (out of 50 total)

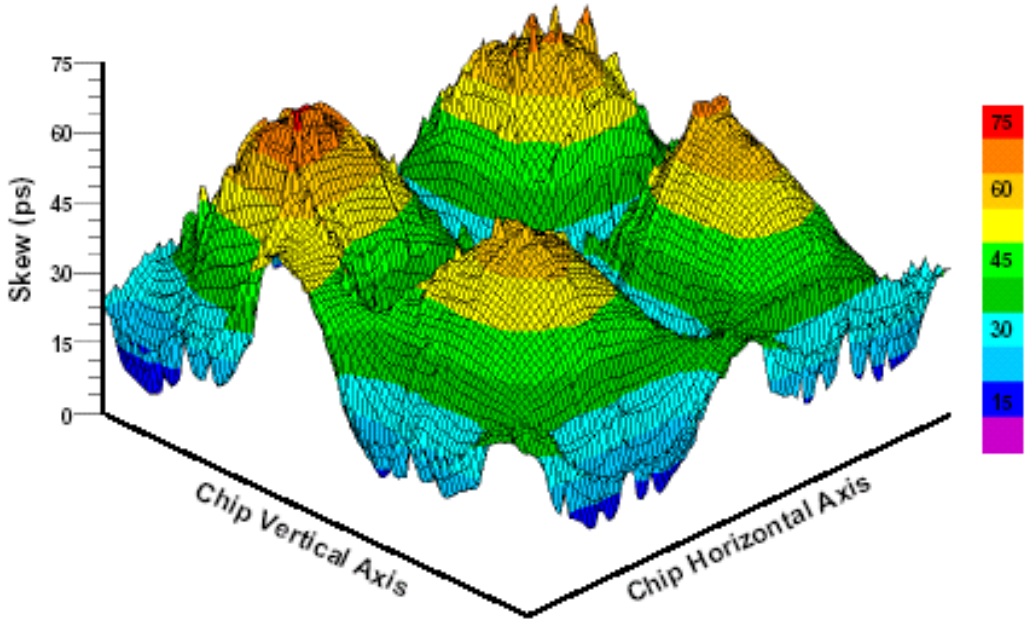
- Uses two level clock distribution
  - Single 6-stage driver at center of chip
  - Secondary buffers drive left and right side clock grid in M3 and M4
  - Total driver size: 58cm !!





DEC Alpha 21264 Clock Distribution



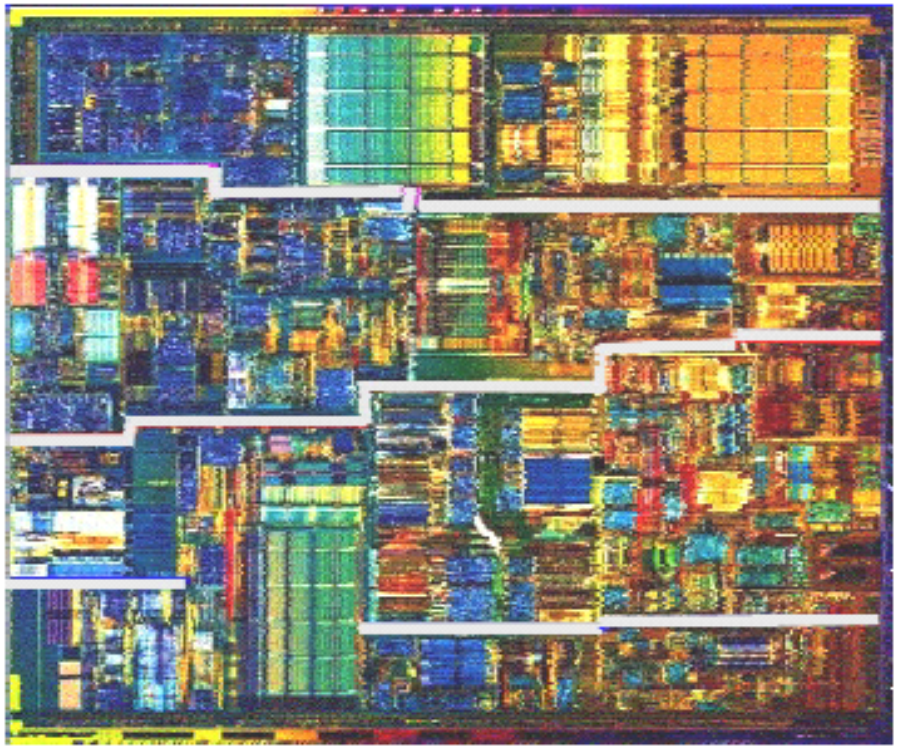


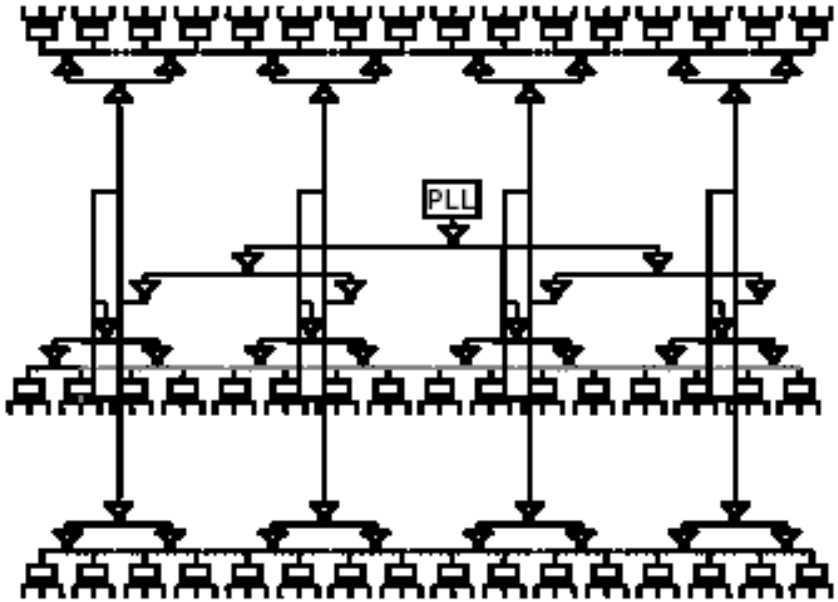
- 600MHz, 9.3M transistors, 0.35μm CMOS, 6 metals, 72W power dissipation at 2.0V
- Total clock load: 2.8nF

Gronowski, JSSC 1998

Pentium® 4 Processor Clock Network

- 2GHz triple-spine clock distribution

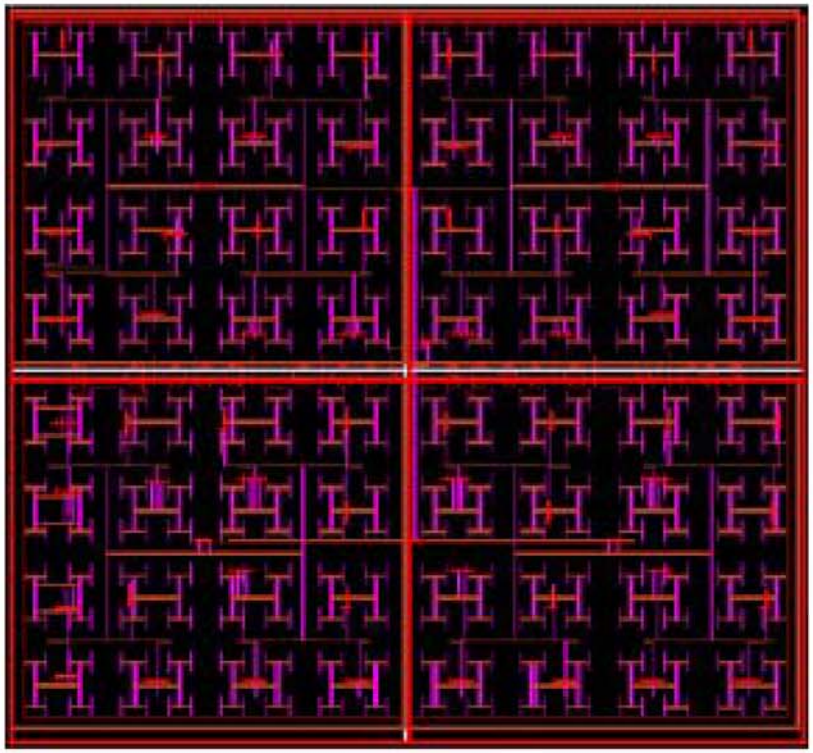


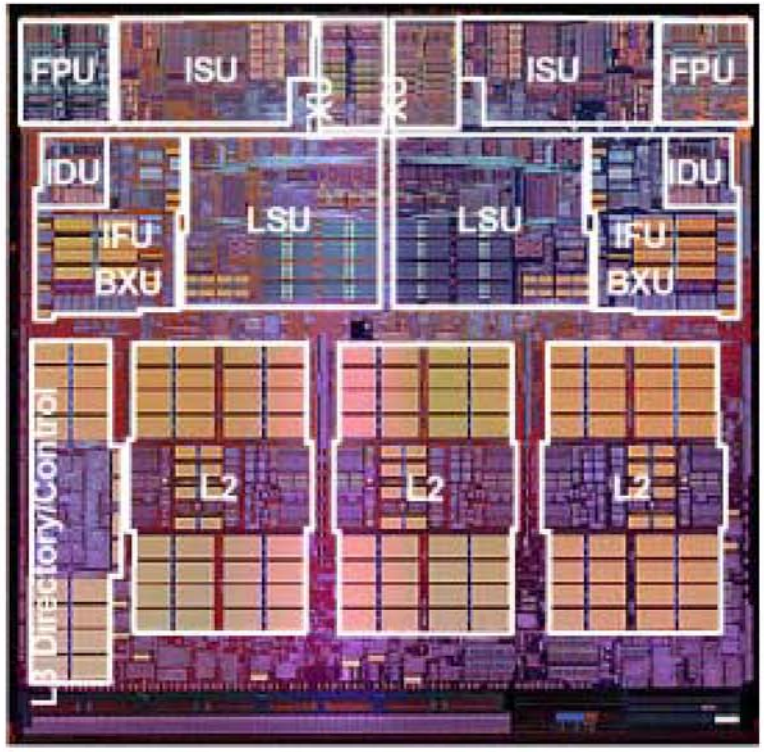


Kurd, JSSC-2001

IBM POWER-4 in .18u SOI

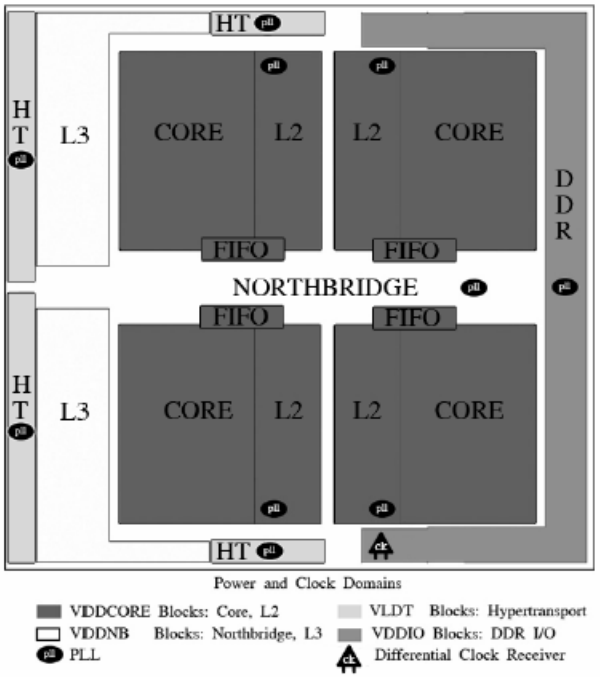
- H-Tree and Grid Distribution
- Clock skew: <25ps
- ~70% power in clock and latches
- Dual core, shared L2
- 174M transistors
- 115W at 1.1GHz, 1.5V

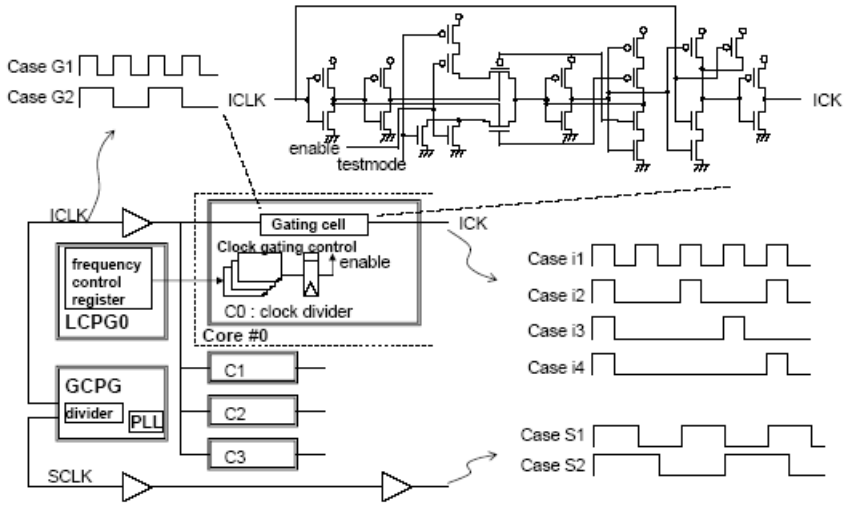




Source: Physical Design of a Fourth-Generation POWER GHz Microprocessor, ISSCC'2001

ISSCC 2007: Multi-Core Clocking Approach Asynchronous Communication and Independent Core Frequencies

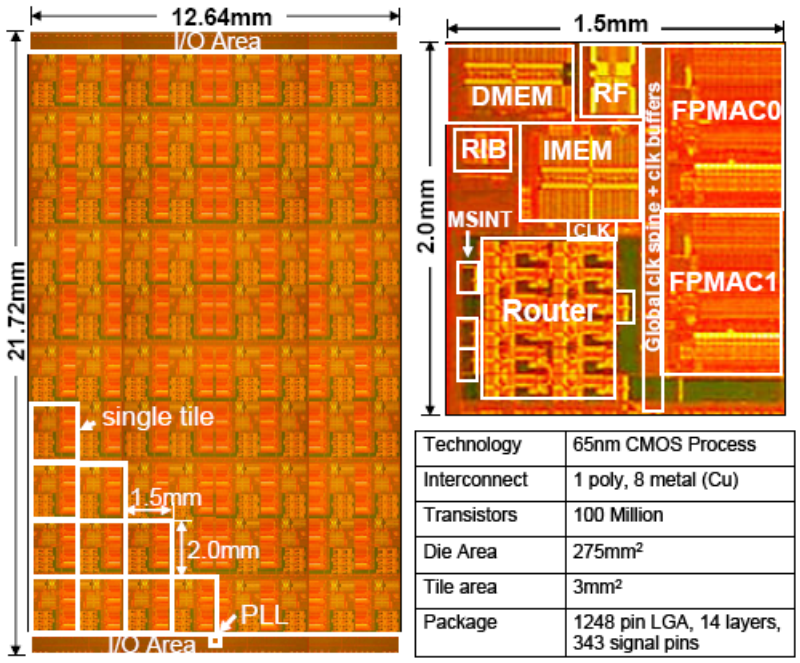




Source: An Integrated Quad-Core Opteron™ Processor ISSCC 2007

Source: A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption, ISSCC 2007

ISSCC 2007: Multi-Core Clocking Approach Asynchronous Communication



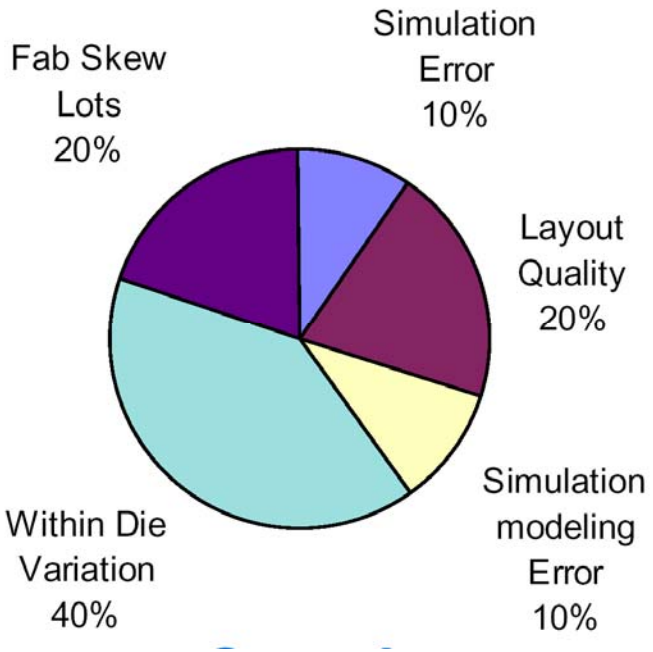
Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm²
Tile area	3mm²
Package	1248 pin LGA, 14 layers, 343 signal pins

Source: An 80-Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS, ISSCC 2007

Clock Uncertainty

- **Clock uncertainty is defined as the uncertainty in time in which a clock edge will appear. It is determined by clock skew, clock jitter and clock overhead.**

- **There are a number of sources which cause clock uncertainty. A typical breakdown of the sources are:**

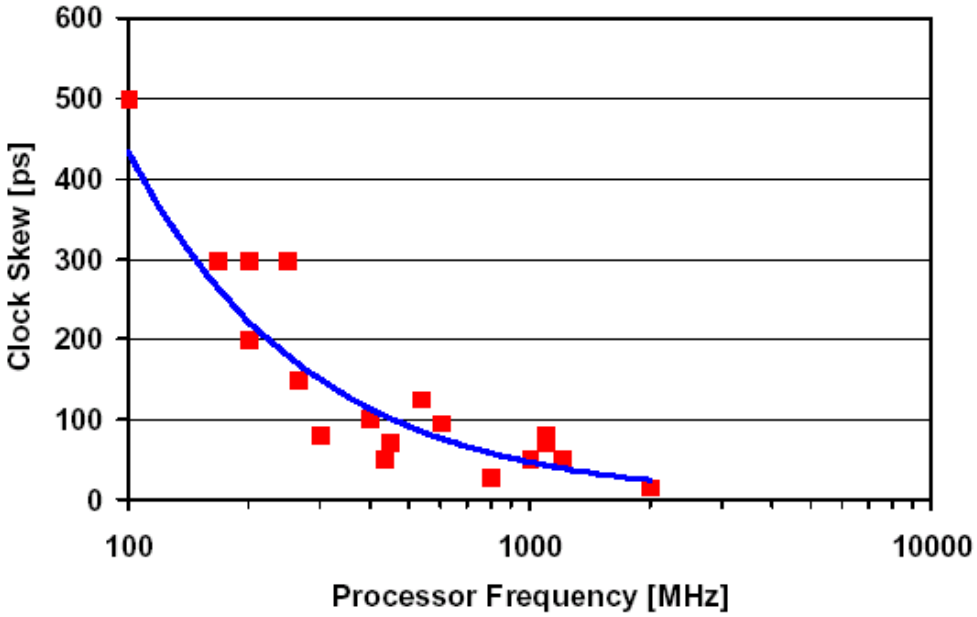


Clock Uncertainty

- An example of static clock uncertainty is clock skew. Clock skew represents the difference in delay of two identical clock signals arriving at two different locations on the chip (spatial separation).
- Clock jitter is the clock edge inaccuracy introduced by the clock signal generation circuitry.
- Clock overhead refers to the time a sequential storage element needs to positively store (or resolve) the incoming data. This time is directly related to the metastability properties of the sequential storage element.
- Clock uncertainty can have detrimental effects on the viability of a design:
  - Min-delay (hold) failures are frequency independent
    - Chip must be discarded
  - Max-delay (setup) failures are frequency dependent
    - Chip can be sold at a lower frequency

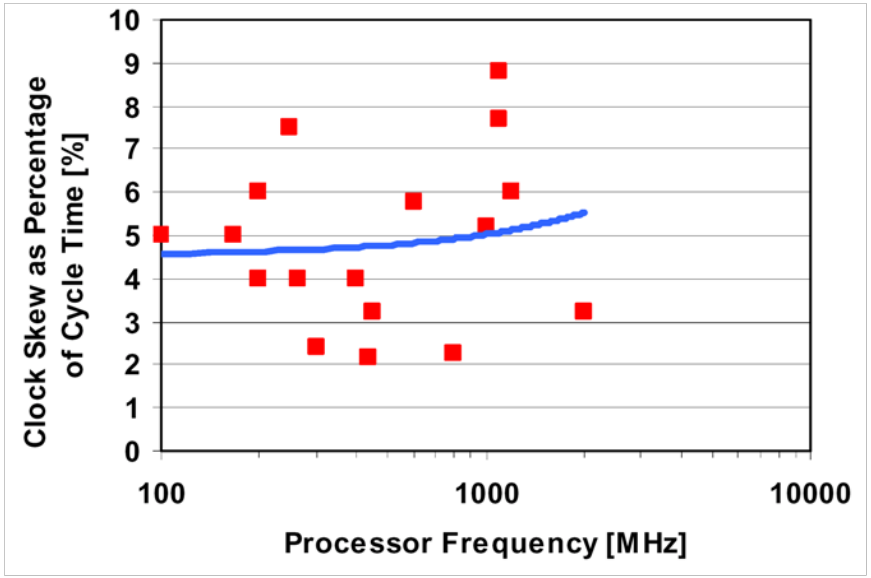
Clock Skew

- Clock skew can be intentional or unintentional. For example, intentional clock skew may be injected in order to fix a race condition in a block of logic. This is typically achieved by the use of a variable delay clock regeneration buffer.
- Clock skew can be positive or negative depending on how the reference clock is chosen.



Clock Skew

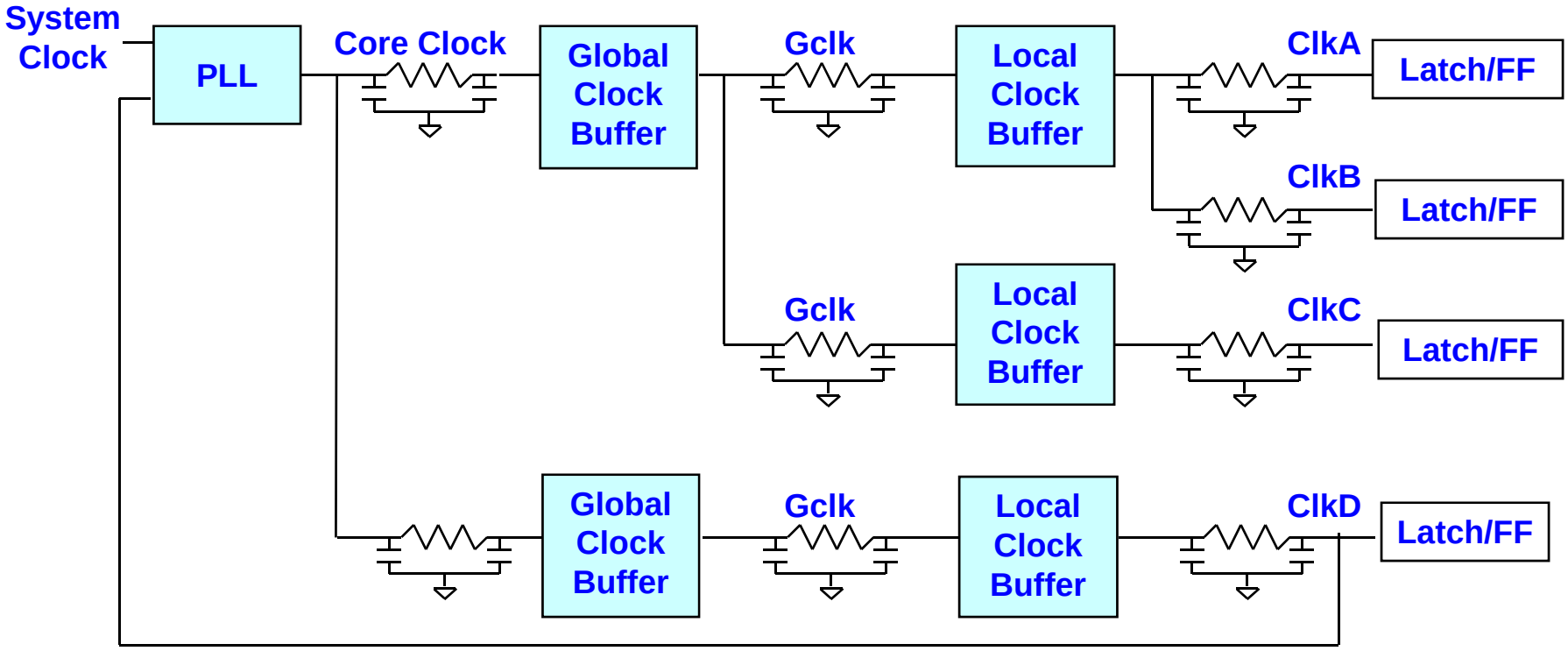
- Clock skew accounts on average for about 5% of the cycle time and is trending higher as frequency increases



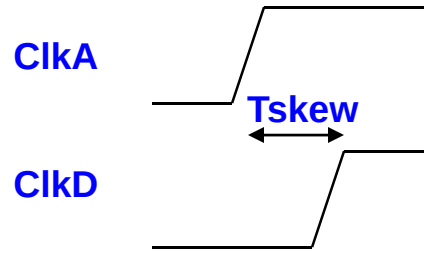
- In general we strive to minimize clock skew, however we must design our circuits to be clock skew tolerant.
  - Good reading on this topic:

    Harris, *Skew Tolerant Circuit Design*, Morgan Kaufmann Publishers

Clock Skew

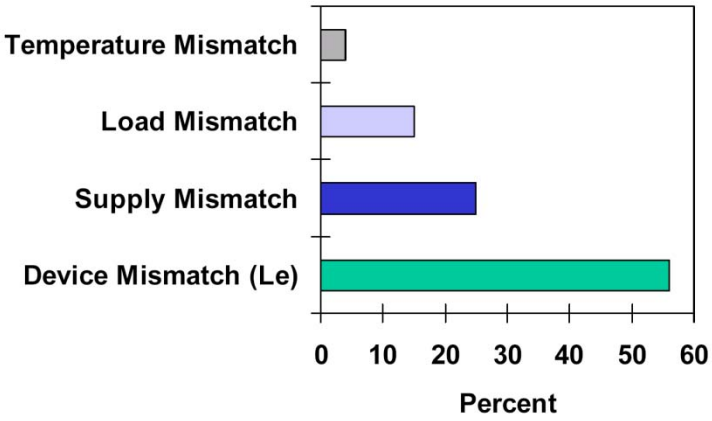


A single transition of the core clock does not arrive at all latches or flip-flops at the same time.



Sources of Clock Skew

- In-die Process, Voltage, Temperature (PVT) variation
  - Different clock buffers with different channel lengths
  - Local drop in voltage leads to increased buffer delay
  - Hot spots lead to increased gate and wire delay
  - Device mismatch across die



- Wire coupling
  - Coupling will be different on different clock routes
- RC mismatch
  - Clock routes not all of equal length
  - Latches not all equal distance from LCB (local clock buffer)
- Inductance of high speed, low resistance lines changes edge-rates. Unequal buffering can cause additional skew due to rise time-dependent delay in buffers.

Industry clock skew data

Processor	Frequency (MHz)	Clock Skew (ps)	Process
Itanium™	800	110ps w/o deskew 28ps w/ deskew	.18µ
PowerPC	1000	15ps with Cu wires	.22µ
UltraSPARC III	800	80ps Al wires, no deskew	.18µ
Alpha	600	72ps Al wires, no deskew	.13µ

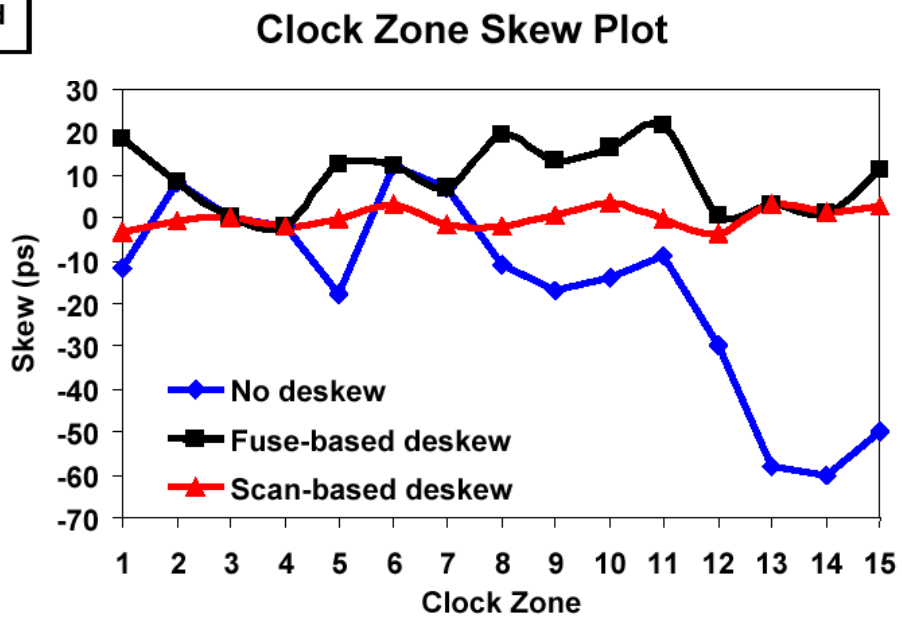
Source: ISSCC Papers

Itanium Clock Distribution Trend

J. Stinson and S. Rusu, ISSCC 2003

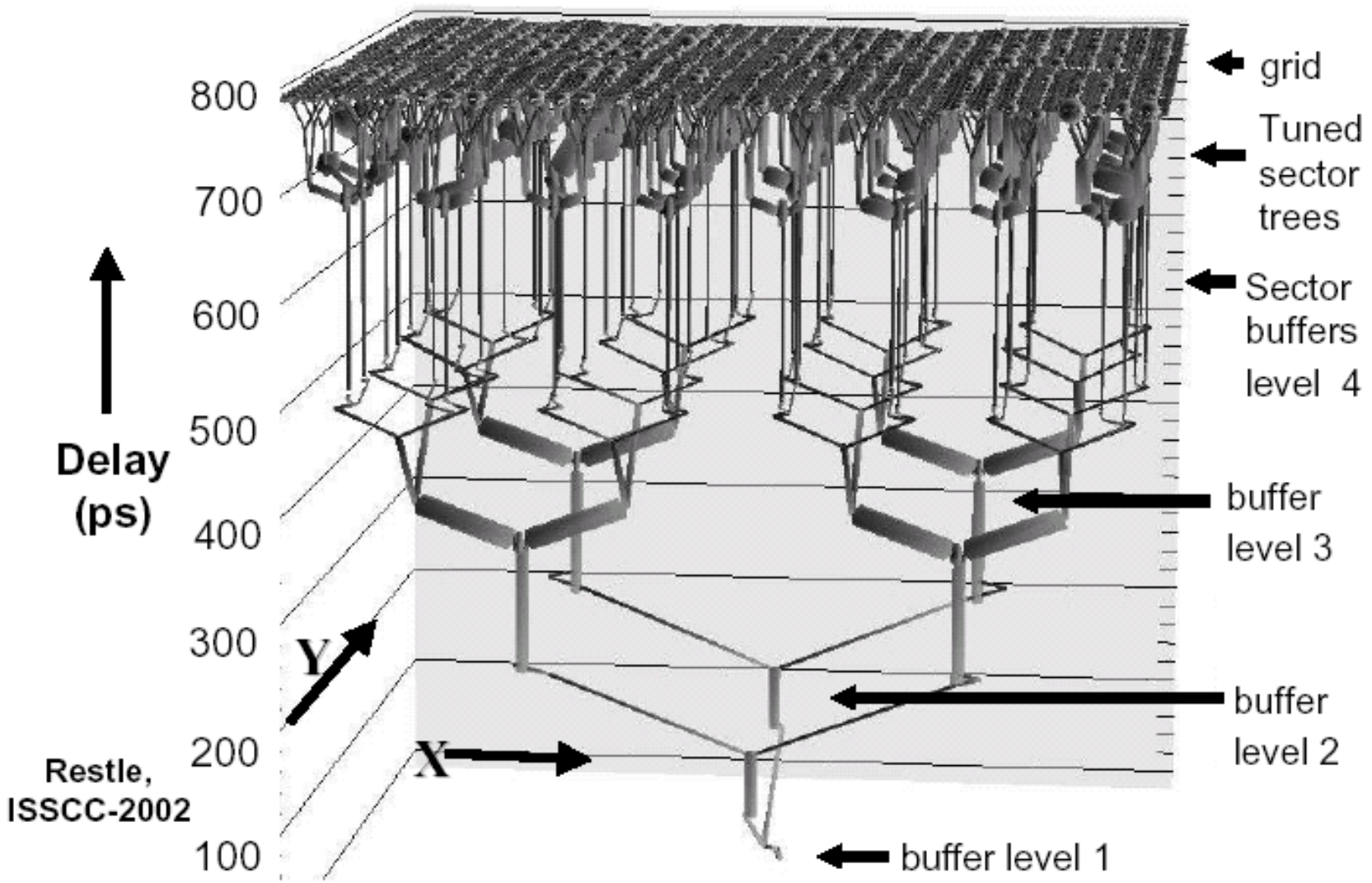
Itanium® Processor Clock Distribution Trends

Attribute	Itanium® Processor	Itanium® 2 Processor	This work
Process/Metal	180nm / Al	180nm / Al	130nm / Cu
Primary tree	Single ended	Differential	Differential
Local distribution	Grid	Tree	Tree
Clock skew [ps]	28ps	62ps	24ps
Deskew Method	Active	On-demand	Fuse-based



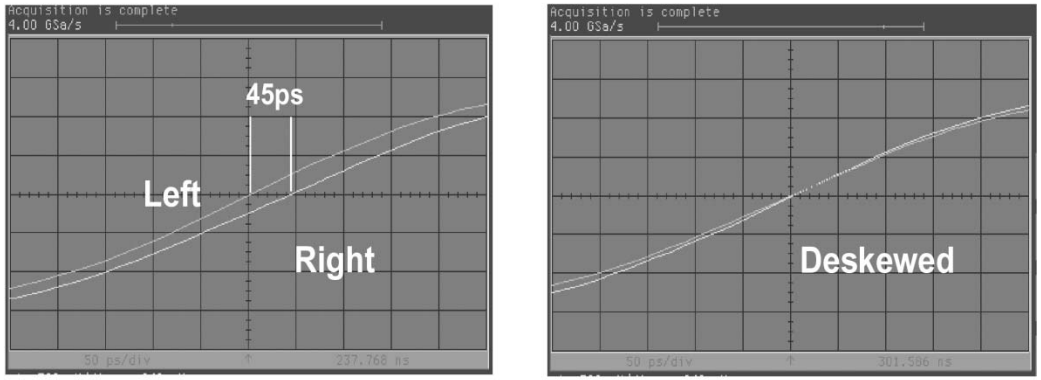
- Worst case clock skew is 24ps in fuse mode and 7ps in scan mode

IBM POWER-4 3D Skew Visulation

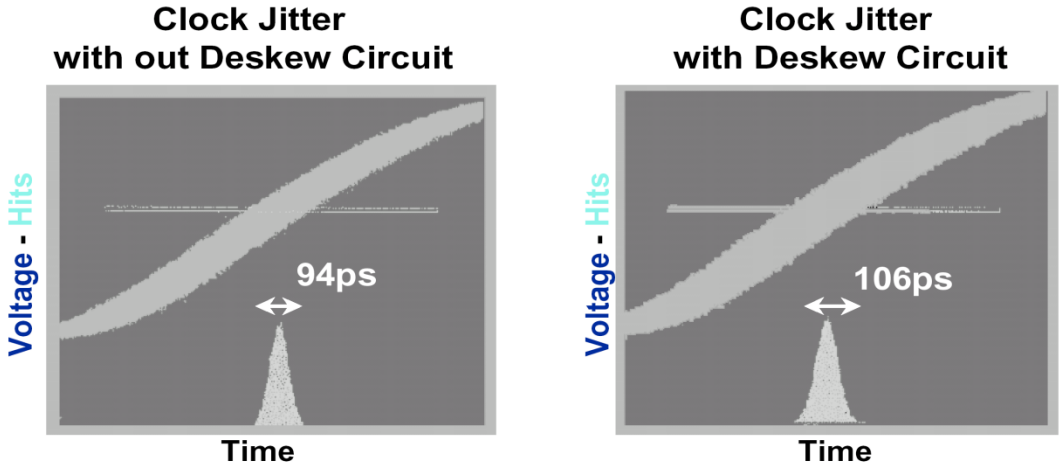


Clock Deskewing

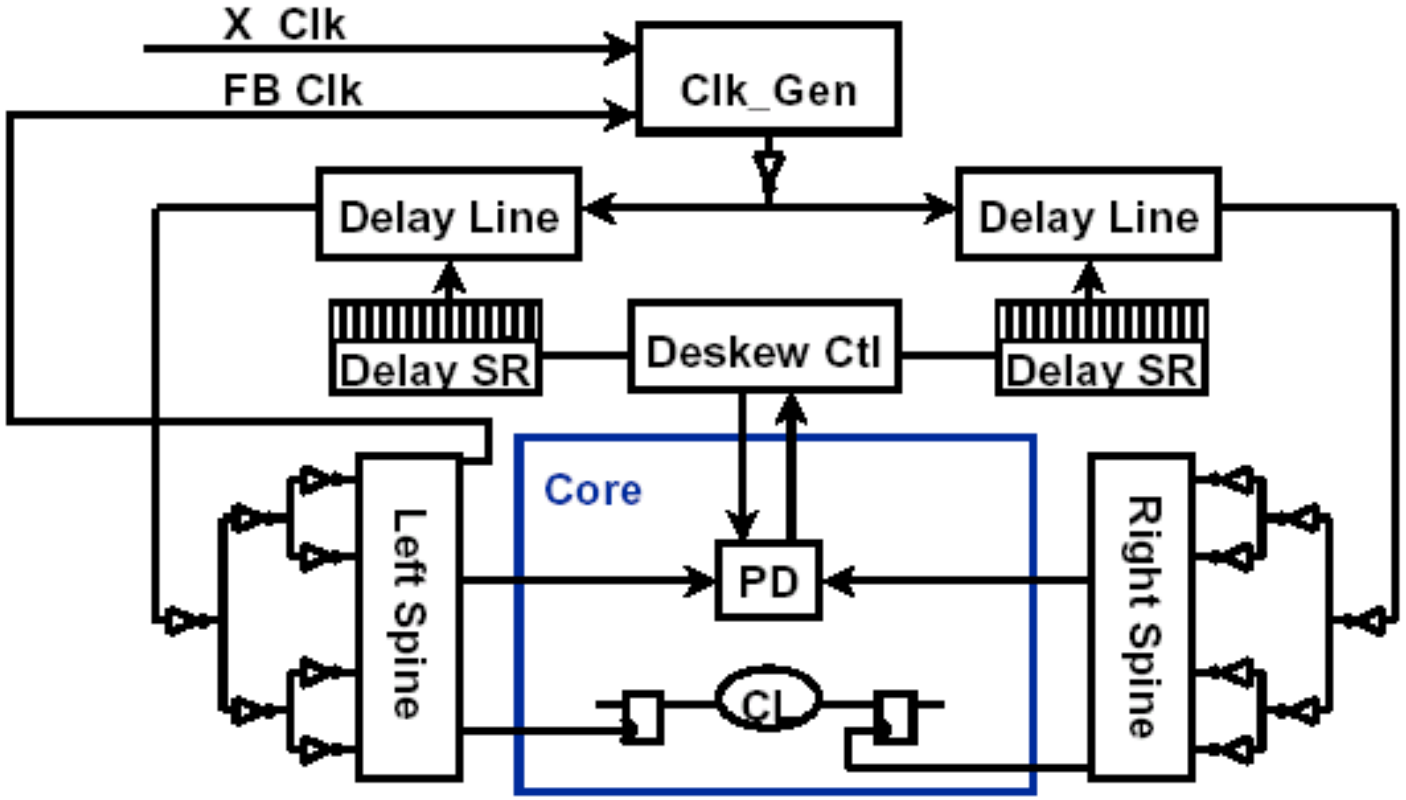
- **Active clock deskewing is accomplished by dynamically delaying the global clock signals.**



- **This can result in clock jitter. Careful analysis is required to validate the benefits.**



Dual Zone Clock De-skew

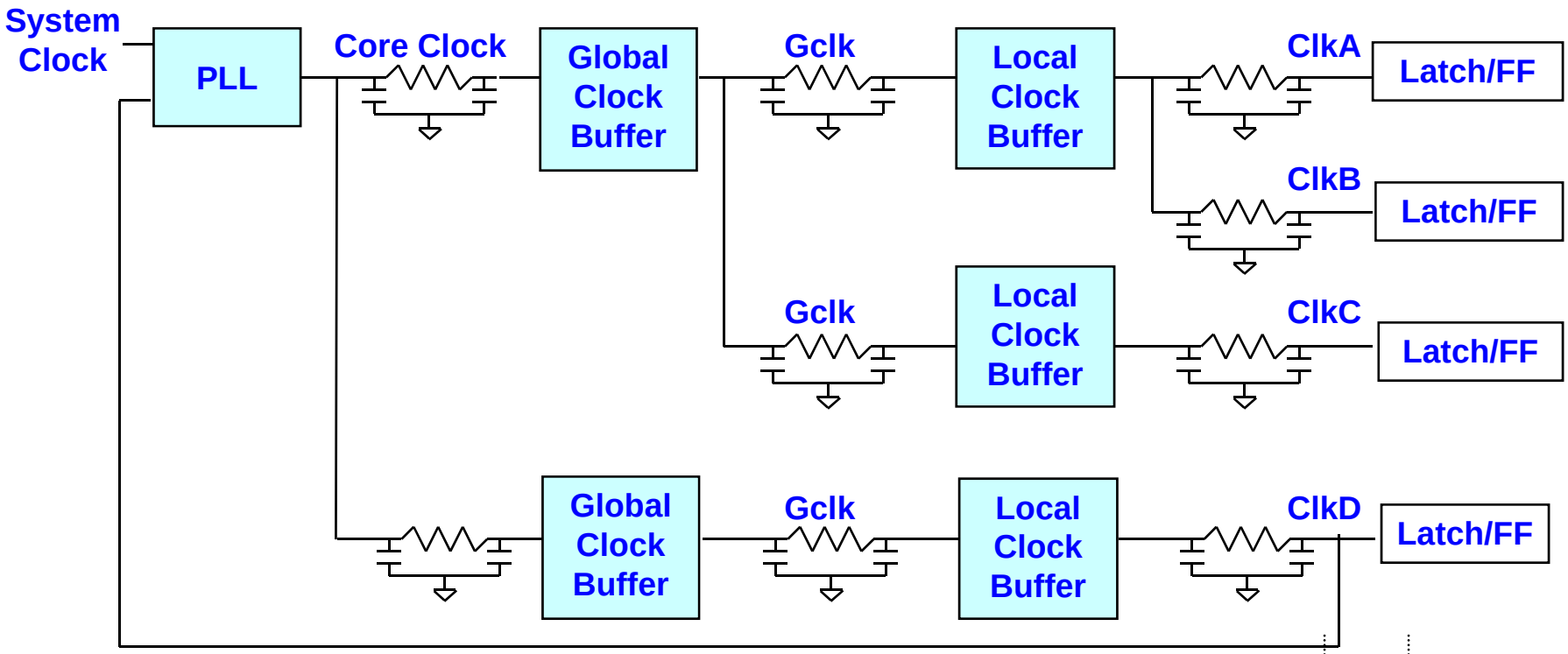


Geannopoulos, ISSCC-1998

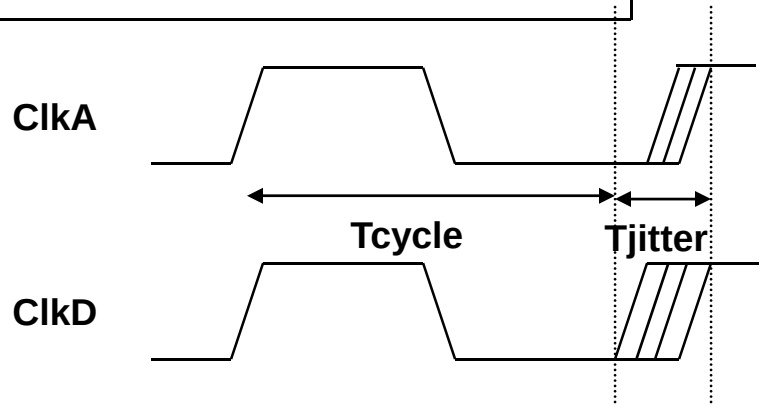
Clock Jitter

- Clock jitter is the clock edge inaccuracy introduced by the clock signal generation circuitry. Clock jitter may be viewed as a statistical variation of the clock period or duty cycle.
- Sources of clock jitter:
  - Temporal power supply variations
    - Changing activity can alter supply voltage in different cycles affecting either the global or regional (local) clock buffers.
  - PLL Jitter
    - Supply variation at PLL can affect oscillator frequency
    - PLL components do not have zero response time
    - Reference clock jitter being multiplied by the PLL
    - Global clock distribution may add jitter to PLL due to supply noise causing the feedback clock signal to seem to jitter.
  - Wire coupling
    - Changing data can alter coupling in different cycles
  - Dynamic Deskewing Circuitry

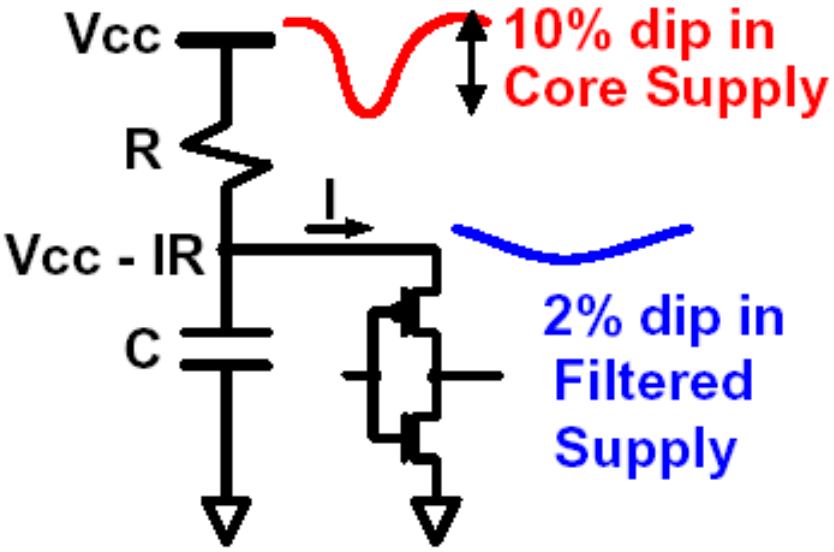
Clock Jitter



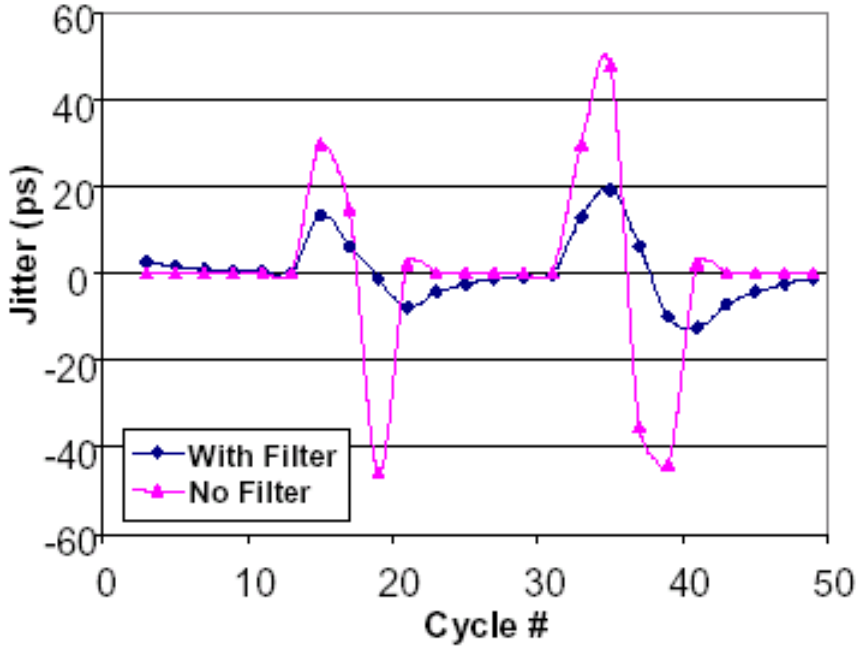
Clock frequency at any point in the clock tree is not constant. The worst case jitter determines usable clock cycle time.



Pentium® 4 Processor Jitter Reduction

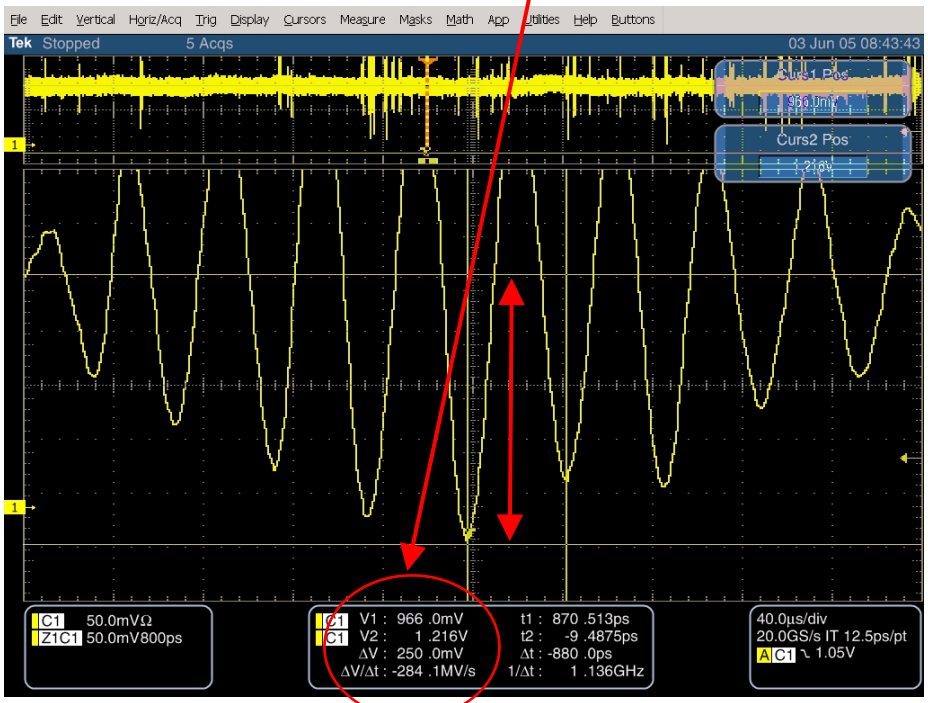


Kurd, JSSC-2001

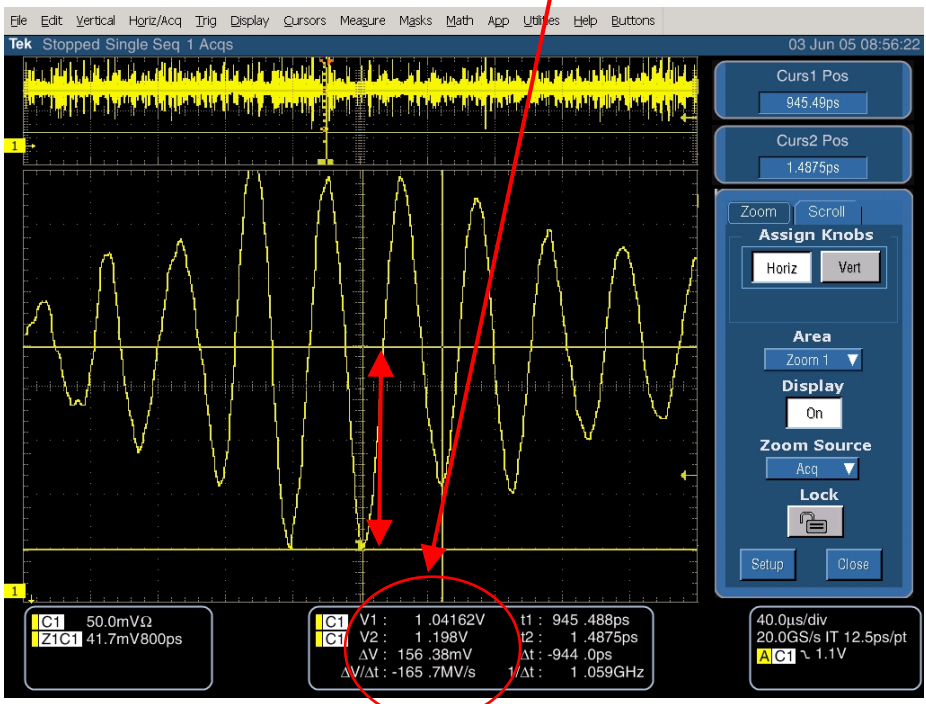


Power Supply Noise Influences Jitter
Voltage Comparison: MIM vs. no MIM
1.2V 90nm SOI microprocessor

No MIM => 250mV noise => -20.6%



8ff/um² MIM => 156mV noise => -13.0%

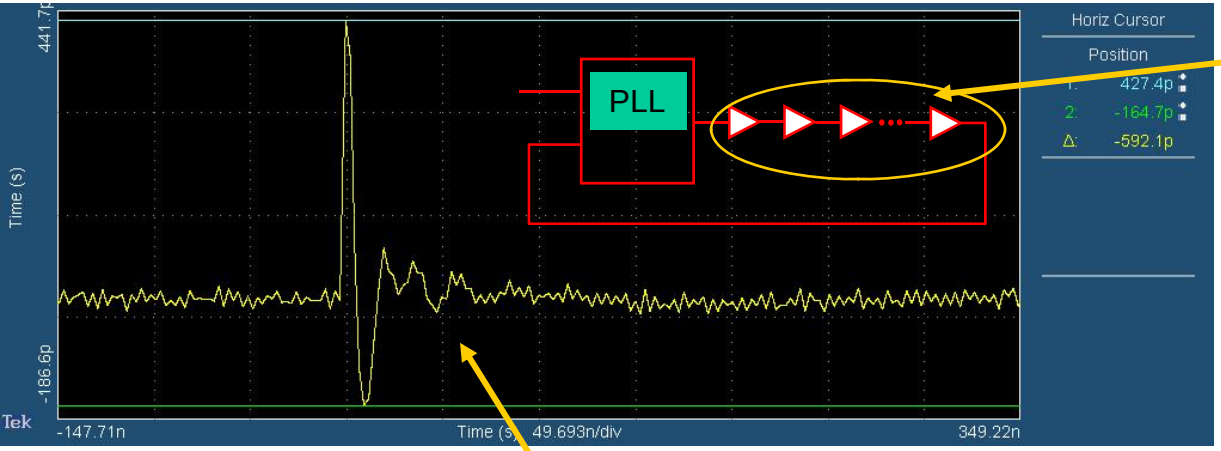


Measured Core Vdd no-MIM vs. with-MIM while running same code

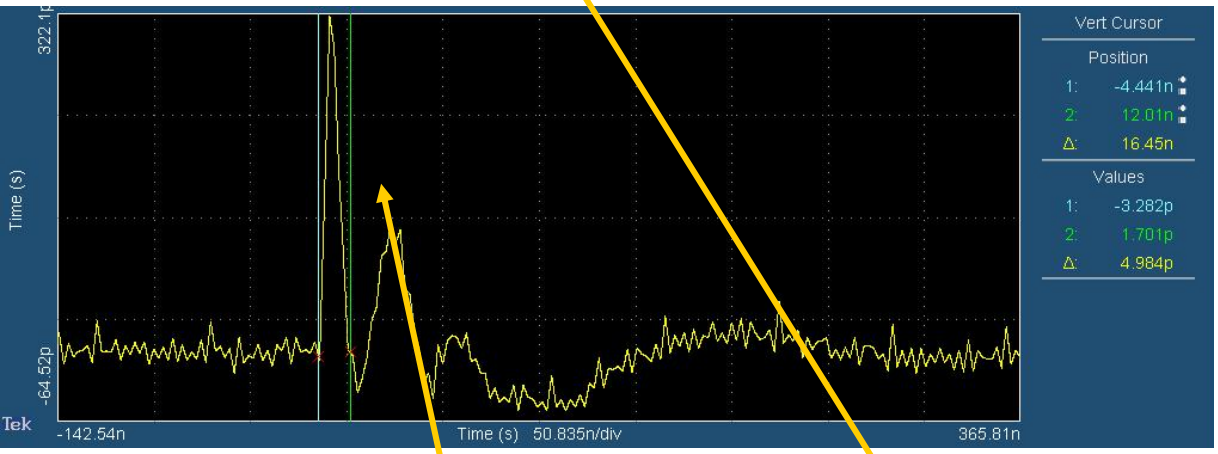
H. Sanchez, ISSCC2006

Supply Noise Clocking Issue: Instantaneous Phase Shifts

H. Sanchez, ISSCC2006



Measured data from highly integrated SoC



TIE of global clock: Non-MIM shifts 592ps as compared to MIM where it is reduced to 388ps.

- **Clock distribution buffers are exposed to Vdd noise**
- **Large di/dt events of microprocessor Core can cause substantial Vdd noise that in turn affects the instantaneous phase relationships of clocks**
- **Addition of MIM decap shows a measured 40% reduction in peak-peak phase change due to large transient currents related to microprocessor Core activity.**

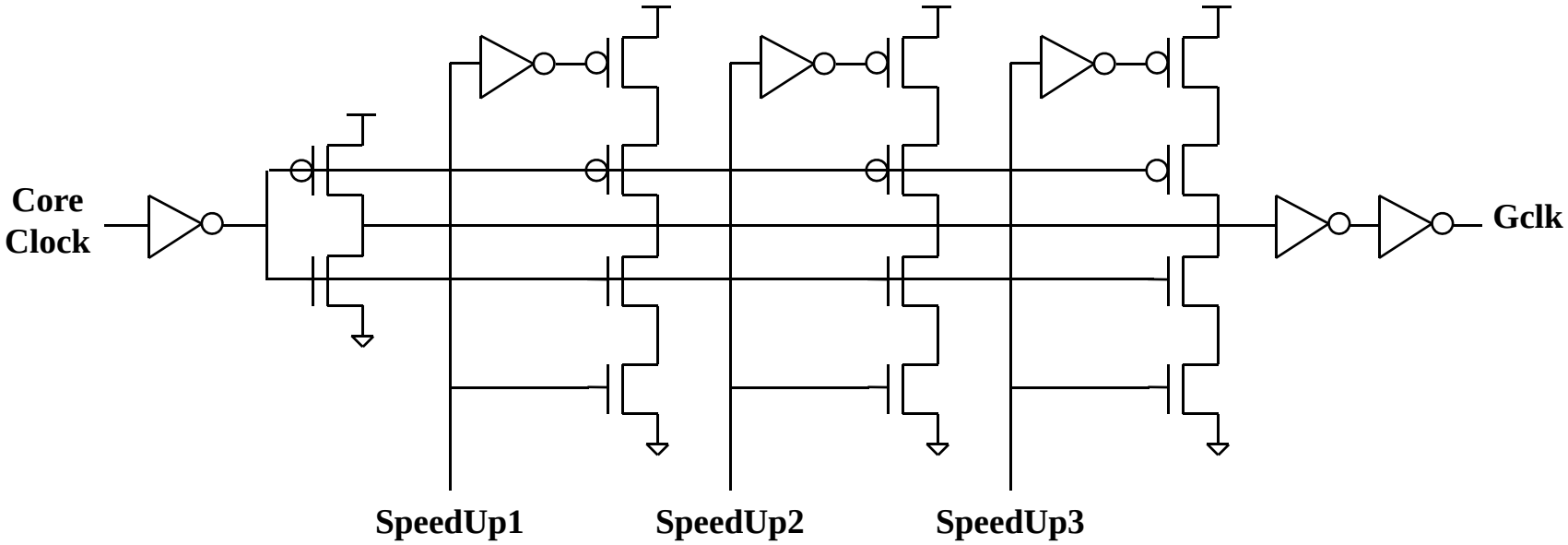
Clock Regeneration

- In the Tree, Grid and Serpentine clock networks it is necessary to buffer (regenerate) the clock signals to ensure satisfactory edge rates and reduce skew.

- The global clock buffers (GCB) are used to regenerate the clock signal(s) to a region or cluster in the chip. They are typically designed with skew adjustment control.

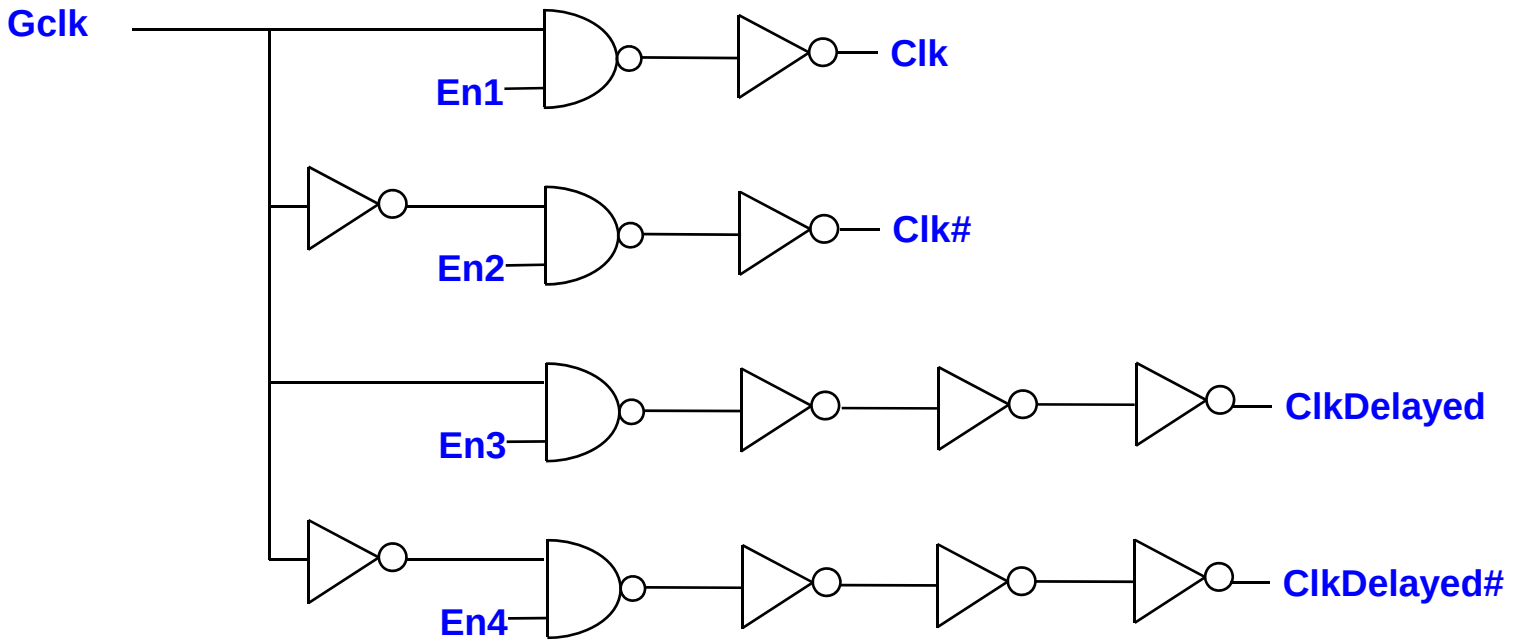
- The local clock buffers (LCB) are used to regenerate the clock signal(s) to functional blocks in each cluster. The LCB usually contains logic which allow the clock signals to be gated on or off to reduce power.

Global Clock Buffer



Global clock buffers can use variable delay to compensate for RC mismatches

Local Clock Buffers

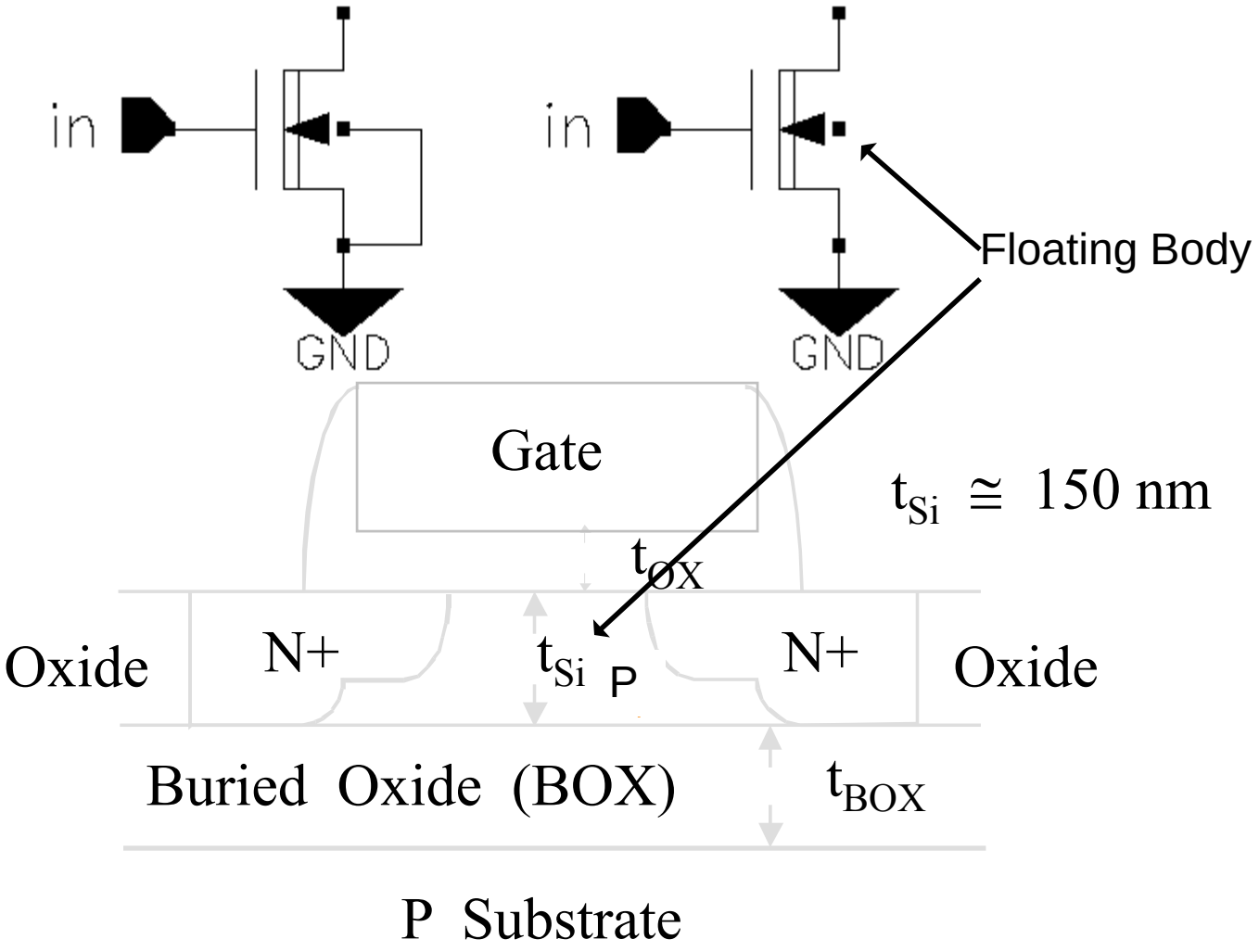


Local clock buffers use enable signals to reduce average power.

Clocking in PD SOI Technology

- Features of Partially Depleted SOI transistors relative to Bulk transistors:
  - Higher Idsat
  - Lower Junction Capacitance
  - Floating Body
  - Worse Self Heating
  - No body effect for stacked transistors
  - Dynamic Id increase due to Gate-Body Coupling
  - Faster switching delays
  - History Effect
    - Delay variation as function of Logic Gate activity
    - Bad for clocking

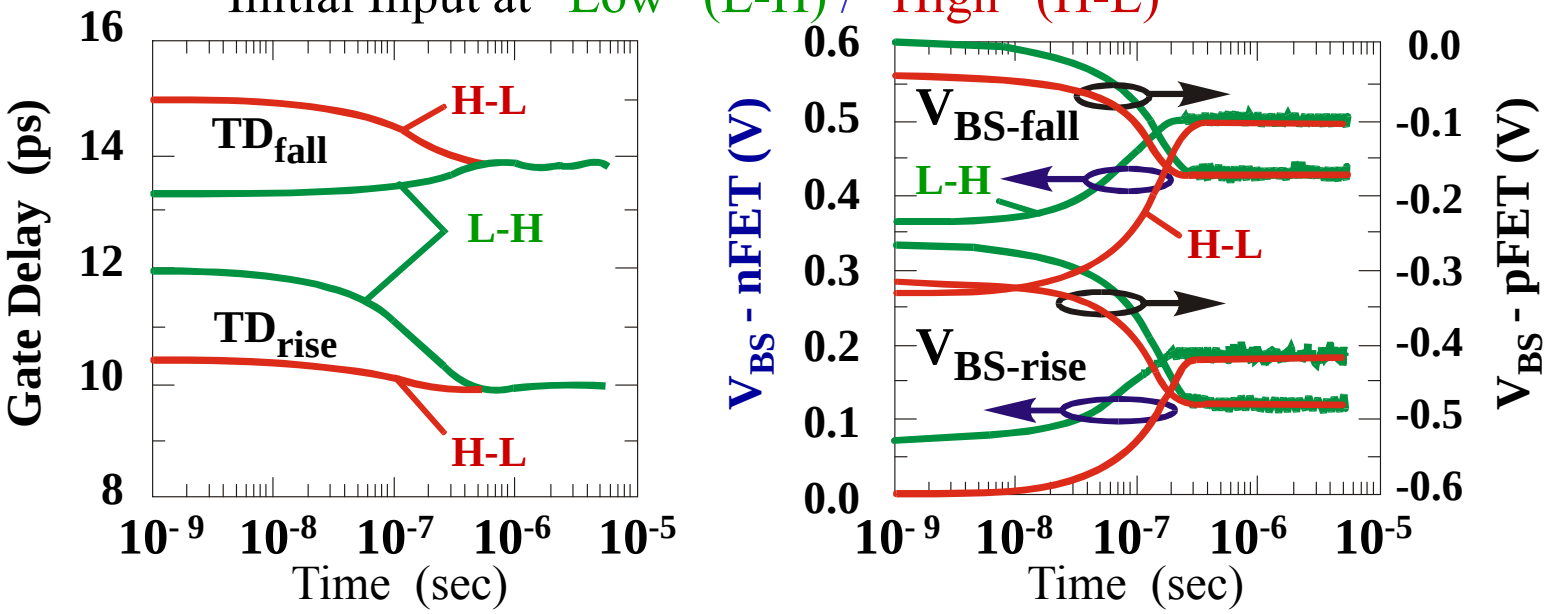
Bulk NMOS and PD SOI NMOS



C. T. Chuang et al., SOI Circuit Design for High-Performance CMOS Microprocessors, 2001 IEEE ISSCC Microprocessor Design Workshop

FB Effect : History-dependent Delay in PD SOI
Non-50% duty cycle clocks at startup !

1.8 V, $L_{eff} = 0.145\ \mu m$, $W_p/W_n = 2$,
1.0 ns Period, 50% Duty Cycle, 100 ps Input Slew
Initial Input at "Low" (L-H) / "High" (H-L)

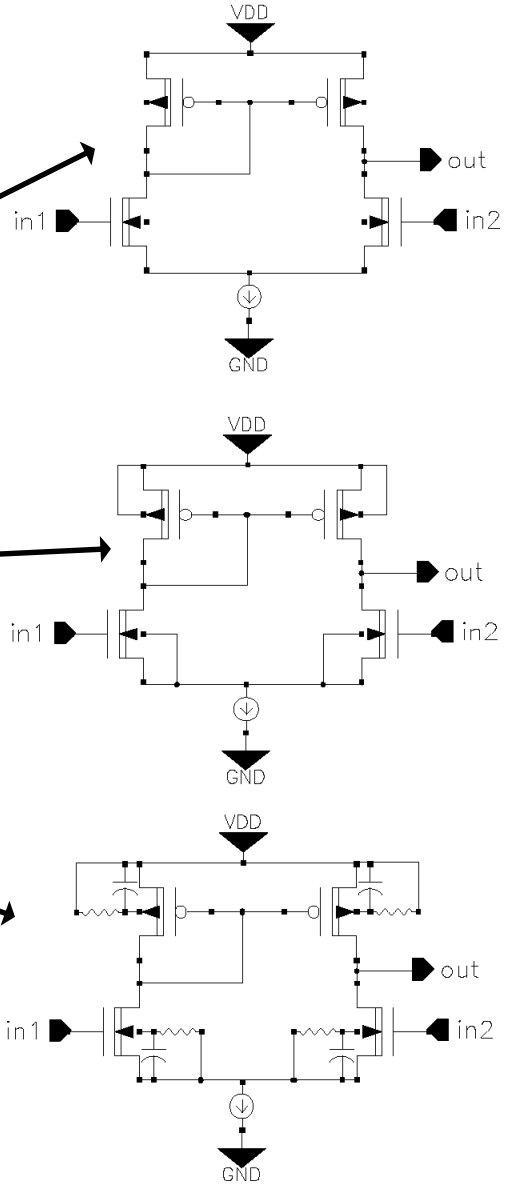


Igate reduces history effect due to control of floating body ! (not shown above)

M. M. Pelella et al., VLSI-TSA, 1999 via
C. T. Chuang et al., SOI Circuit Design for High-Performance
CMOS Microprocessors, 2001 IEEE ISSCC Microprocessor Design Workshop

PD SOI: Differential Amplifiers

- **Diff Amps behave differently …**
  - **Floating Body Diff Amps suffers from inherent Vth mismatch due to FB effect.**
  - **Body Tied, low-frequency, diff amp behave as in Bulk**
  - **Body Tied, high-frequency diff amp can be hard to use.**



H. Sanchez, "Design Challenges of PLL, I/O, and Mixed Signal Circuits in Advanced CMOS/SOI Technologies", IEEE Ckt and Sys Sept 2004 Workshop Dallas

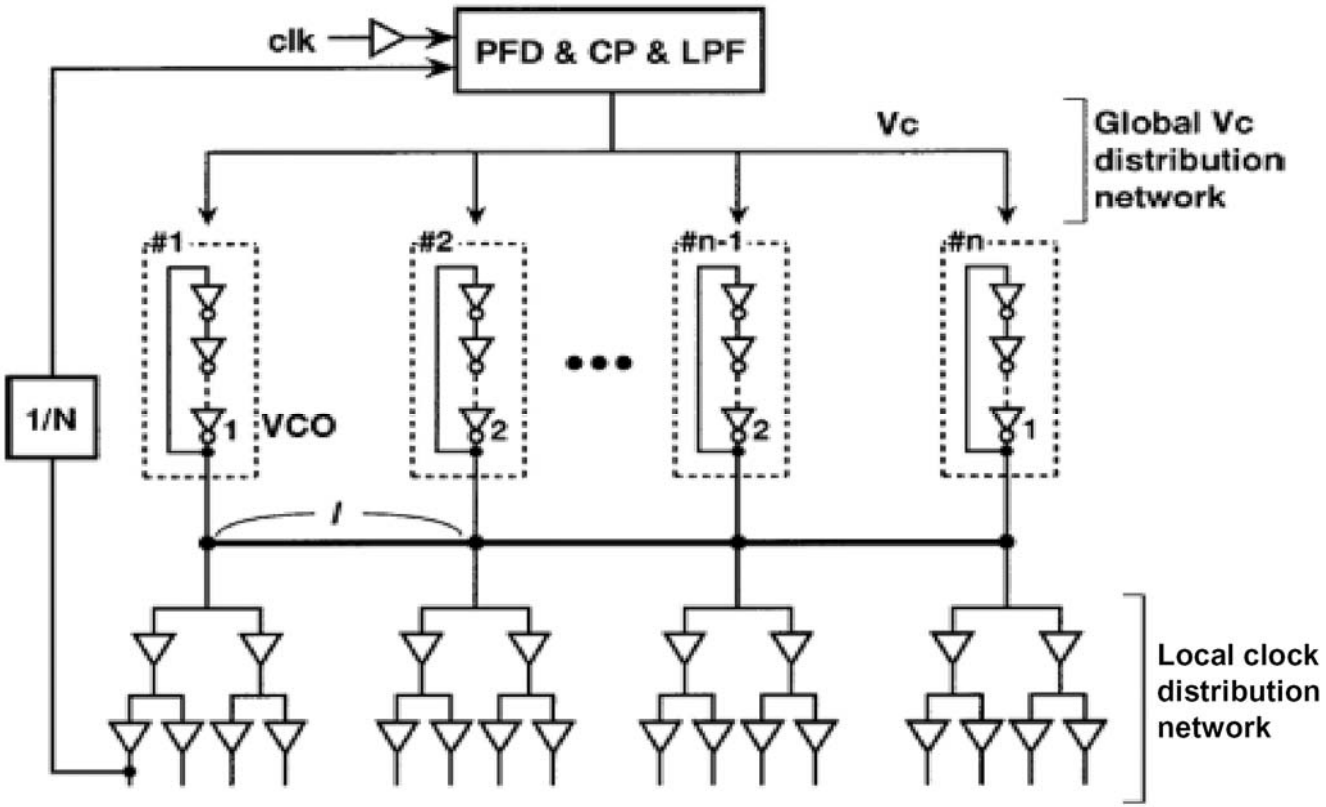
Clocking Issues: Body Ties in PD SOI

- Can body ties help ?
  - Some … If switching signal rate is lower than time constant of contacting the body of transistor then yes (i.e. DC or 100's MHz signals).
    - Charge Pump can use BT devices
  - Not Much … If switching signal rate is in the GHz range.
    - VCOs or high speed buffers suffer history effect with BT devices
  - BT transistors have their own process sensitivities that make them cumbersome to design with (poly head orientation, limited device width for effective body tie , etc).
- PLLs have been designed using both BT and FB PDSOI transistors.
- Designing with BT transistors increases simulation time tremendously.
  - Accurate BT transistor models use multiple segmented transistors to model a single BT transistor, thus for each schematic BT device there may be an effective 3-5 SPICE transistors used to model that single BT device.
- Decision whether to body tie or not may be more driven by faith in ability to *accurately* model and deliver Si that matches model.

Technology Issues: PD SOI

- The BAD thing about PDSOI:
  - Everything varies due to floating body
    - Vth, Cgate, Id
- The GOOD thing about PDSOI:
  - Everything varies due to floating body
    - Vth, Cgate, Id
- WHAT ???
  - Yes, GOOD and BAD.
    - Bad if you are used to thinking that transistors behave like the “lumped” empirical models they are based on.
    - GOOD, because it only prepares you as a designer to accept variability and learn to deal with it. Ultimately, if it’s not PDSOI, it will be some other non-classical device that will require you to learn to “adapt”

Future Directions: Distributed VCOs



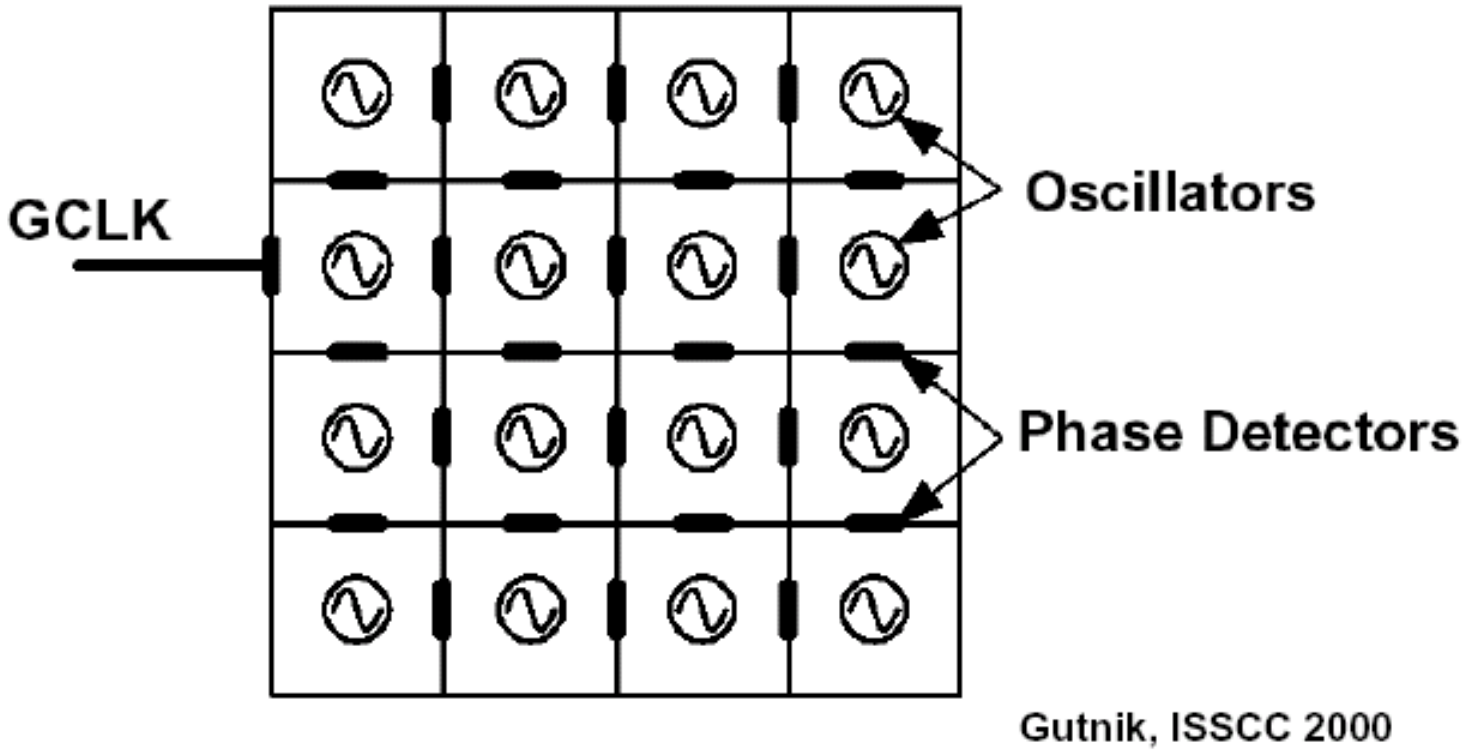
- Generate the clock at multiple points around the grid with distributed voltage controlled oscillators
- Globally distribute the control voltage to local oscillators vs. distributing the clock signal itself

Mizuno, ISSCC 1998

Future Clocking Issues

- Reducing feature size and increasing frequency is the trend for future high performance processors.
  - Reducing feature size means bigger impact of cross die variations.
  - Interconnect delays (RC) do NOT scale well with feature size.
  - RLC effects of the GCDN may require extensive analysis.
  - Reducing cycle time means clock skew budget is a larger percentage of the cycle time.
- Die sizes are getting bigger
  - Longer clock distribution networks resulting in increase skews and jitter.
  - Larger clock loads
- Power consumption increase coupled with decreasing Vdd and increasing noise, pose challenges to multi-GHz clocking schemes known to be industry standards.

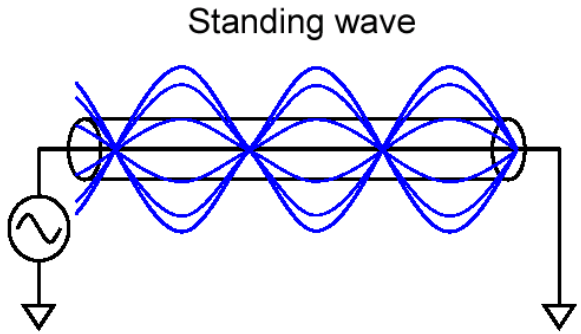
Future Directions: Distributed PLL



Gutnik, ISSCC 2000

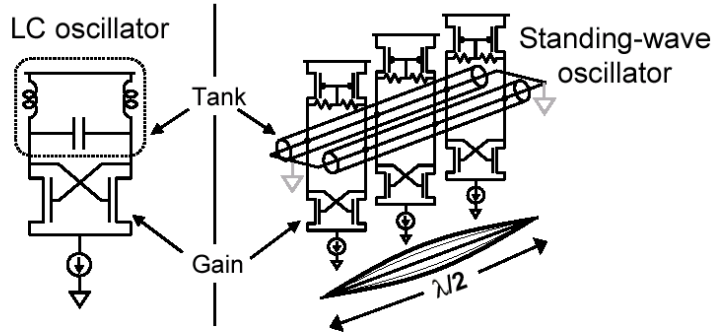
- Synchronized clocks generated at multiple points around the grid
- The PLL filtering compensates for PVT and distribution uncertainties

Future Directions:
Tuned LC tanks, Standing Wave Oscillators



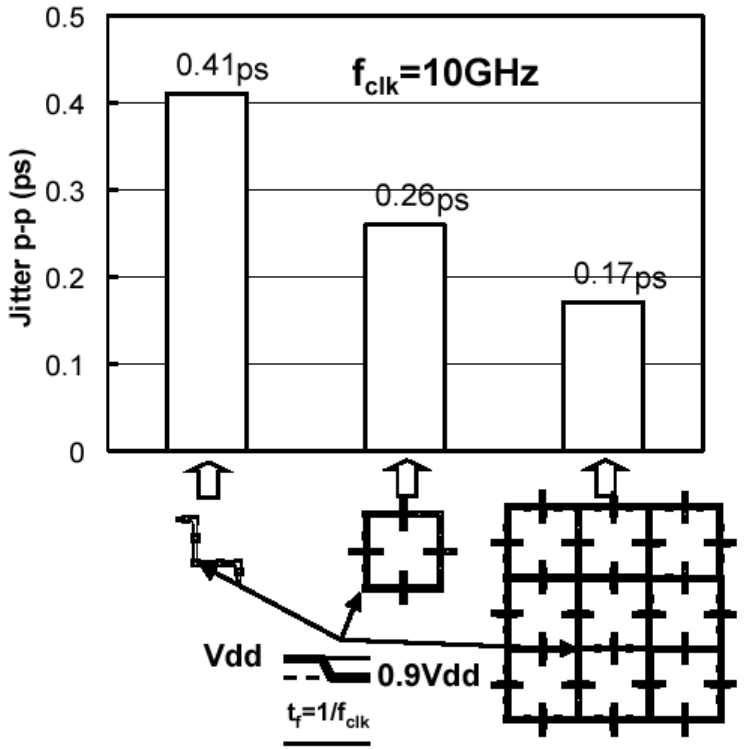
– Wave characteristics
  - Phase is constant with position (with 180° discontinuit
  - Amplitude varies sinusoidally with position

Standing-Wave Oscillator (SWO)



Conditions for oscillation at f_{clk} ⇨ $g_d > \frac{l}{n}\frac{RC}{L}$ and $l = \frac{1}{2f_{clk}\sqrt{LC}}$

Jitter for SWO Grids



- **Frank O'Mahony et al ISSCC 2003**

ISSCC 2005: Itanium2 Clock Distribution

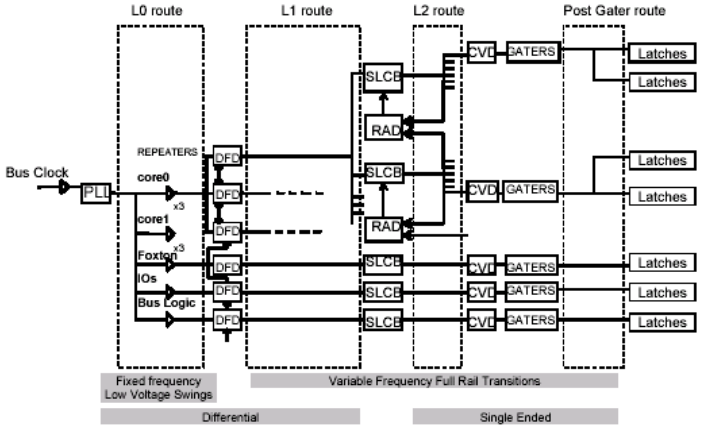
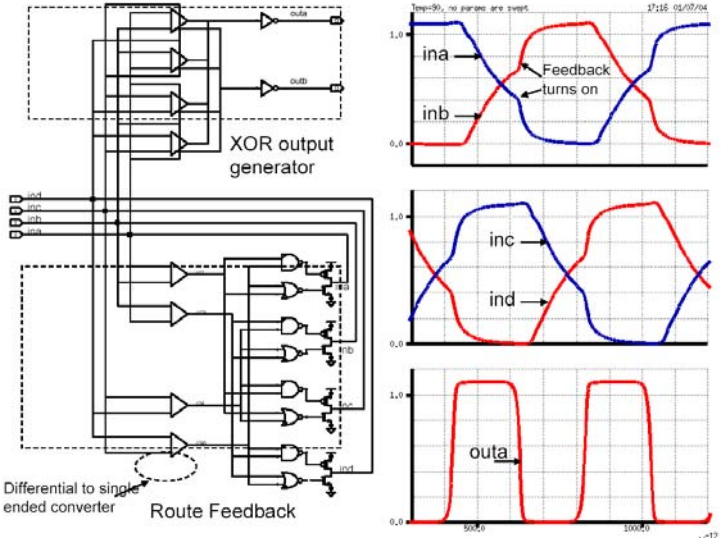


Figure 16.1.1: Clock distribution.



Combine all tricks into 1 distribution: Differential, Single Ended, Global De-Skew, Local De-Skew, Self-Determination of Frequency Based on localized Vdd/Power/Temperature.

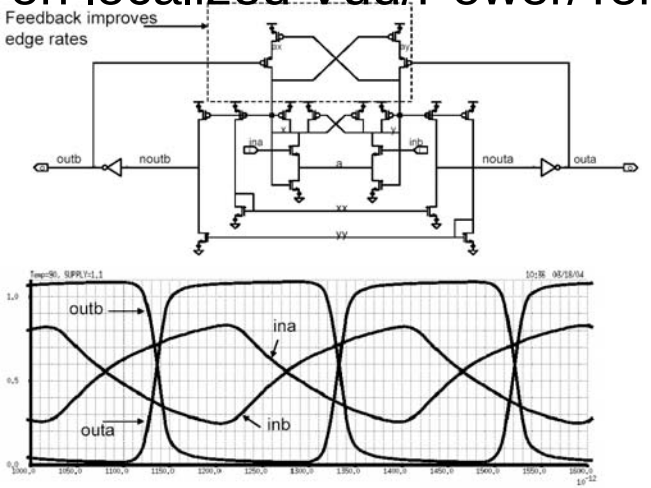


Figure 16.1.2: Level-0 route-repeater design.

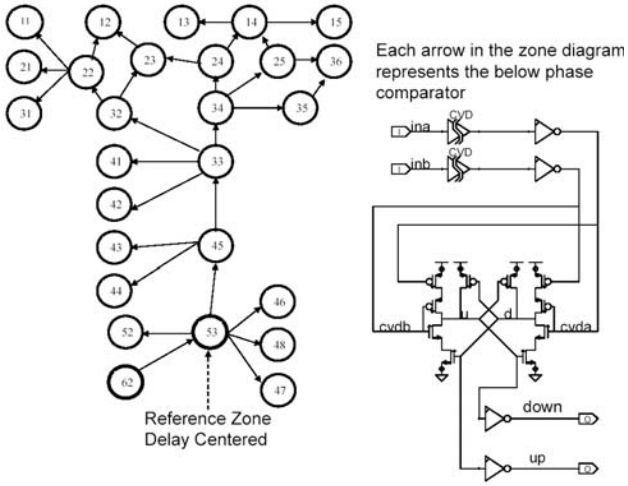
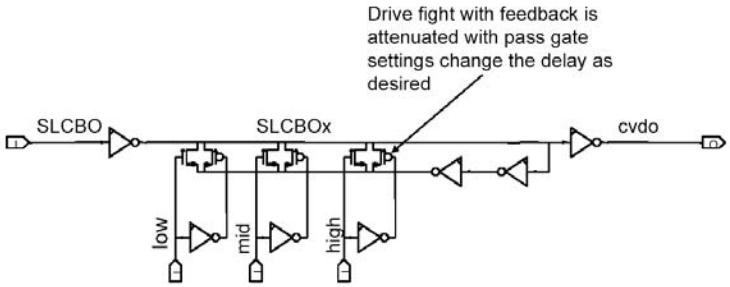


Figure 16.1.4: RAD phase comparator and connectivity.

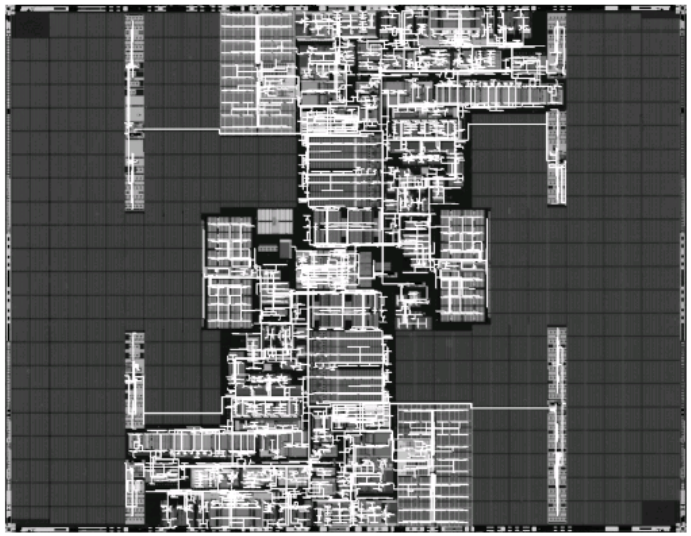
ISSCC 2005: Itanium2 Clock Distribution



Low, mid, and high are scan chain outputs.

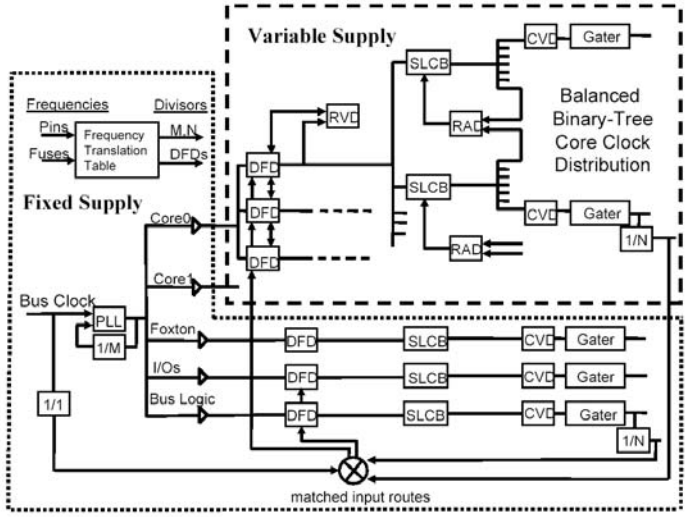
Their values and corresponding delays are binary weighted.

Figure 16.1.5: CVD design.

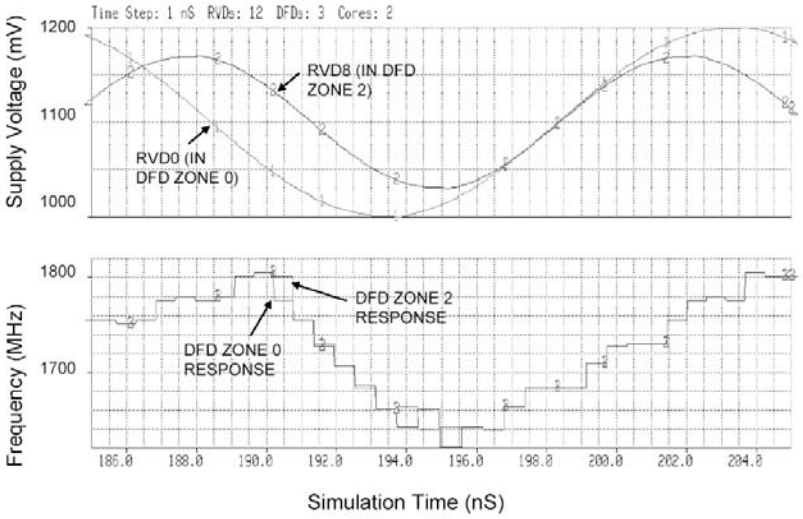


Digest of papers ISSCC 2005
10.1 The Implementation of a 2-core Multi-Threaded Itanium(R) Family Processor
16.1 Clock Distribution on a Dual-core Multi-threaded Itanium(R)-Family Processor
16.2 A 90nm Variable-Frequency Clock System for a Power-Managed Itanium(R)-Family Processor

Route	Terminals	Distance	Power	Delay
L0	14	20mm	600mW	640ps
L1	71	5mm	700mW	215ps
L2	14500	2.0-3.5mm	3.3W	60ps
Post Gater	~5million	0-1.5mm	20W	12ps



ISSCC 2005: Itanium2 Clock Distribution



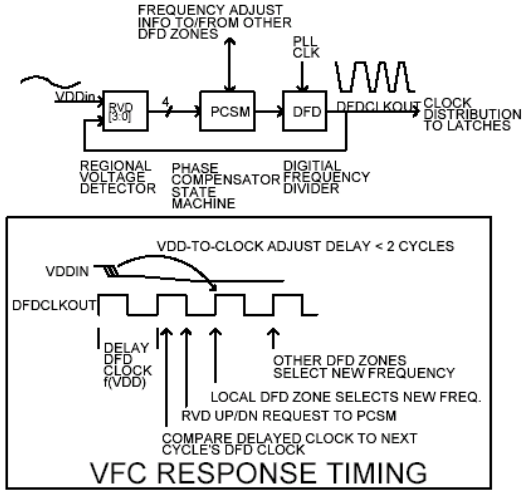
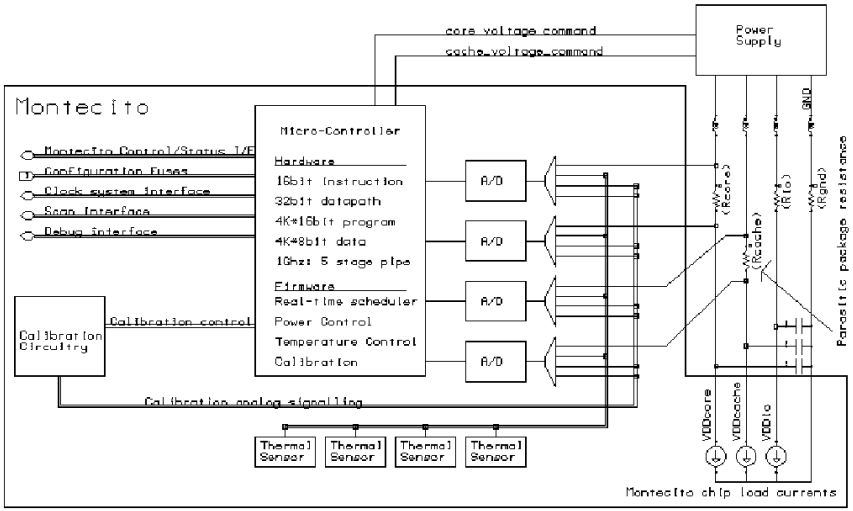


Figure 16.2.3: Voltage-to-frequency converter loop (VFC).



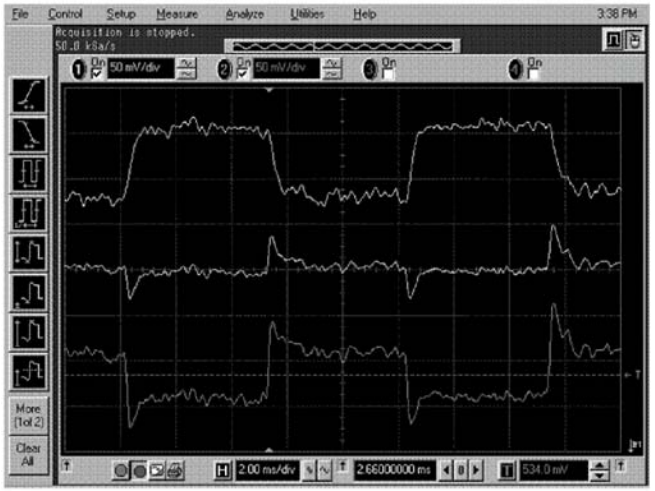


Figure 16.7.2: Voltage, power, and current waveforms.

ISSCC 2005: Clock Routing on Package

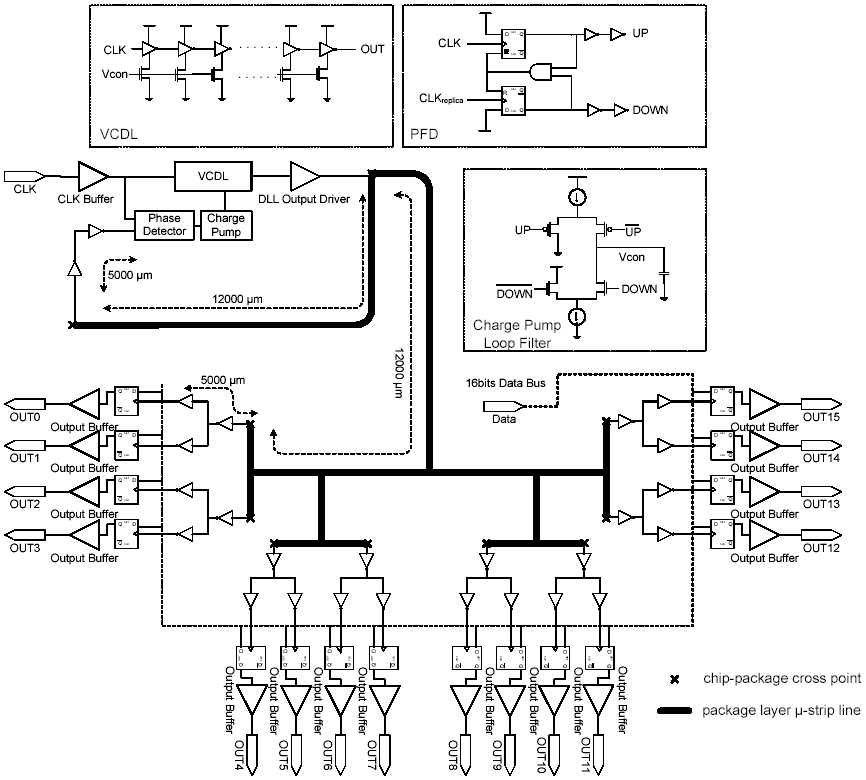
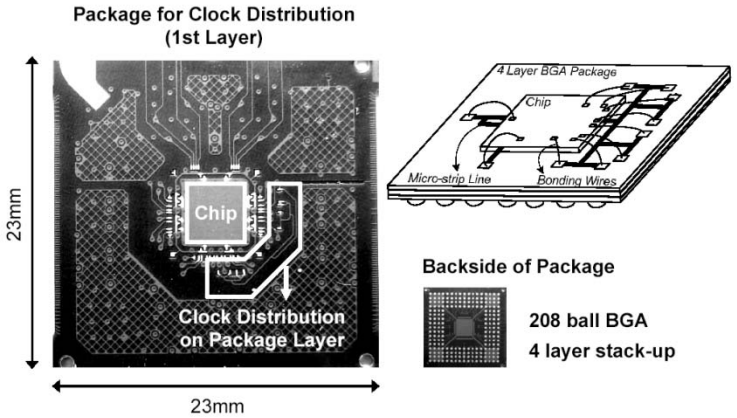
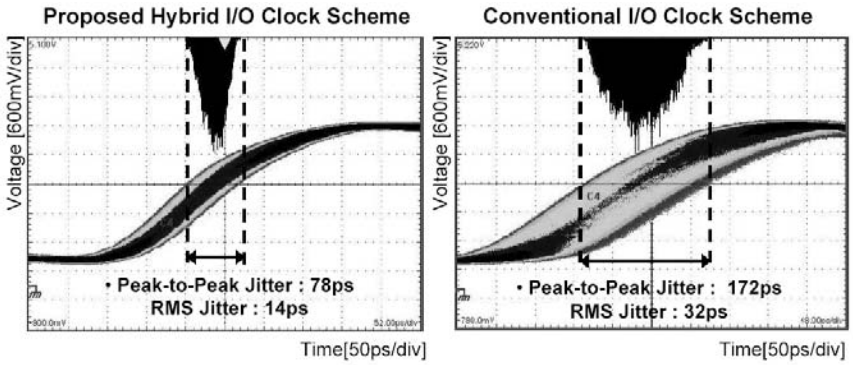


Figure 28.3.1: Schematic diagram of the proposed chip-package hybrid I/O clock scheme.





Digest of Papers ISSCC 2005
28.3 A Chip-Package Hybrid DLL and Clock Distribution Network for Low-Jitter Clock Delivery

Daehyun Chung1, Chunghyun Ryu1, Hyungsoo Kim1, Choonheung Lee2, Jaedong Kim2, Jinyoung Kim2, Kicheol Bae2, Jiheon Yu2, Seungjae Lee2, Hoijun Yoo1, and Joungho Kim1
1KAIST, Daejeon, Korea
2Amkor Technology Korea, Seoul, Korea

ISSCC 2005: Variable Frequency Resonant Clock Distribution

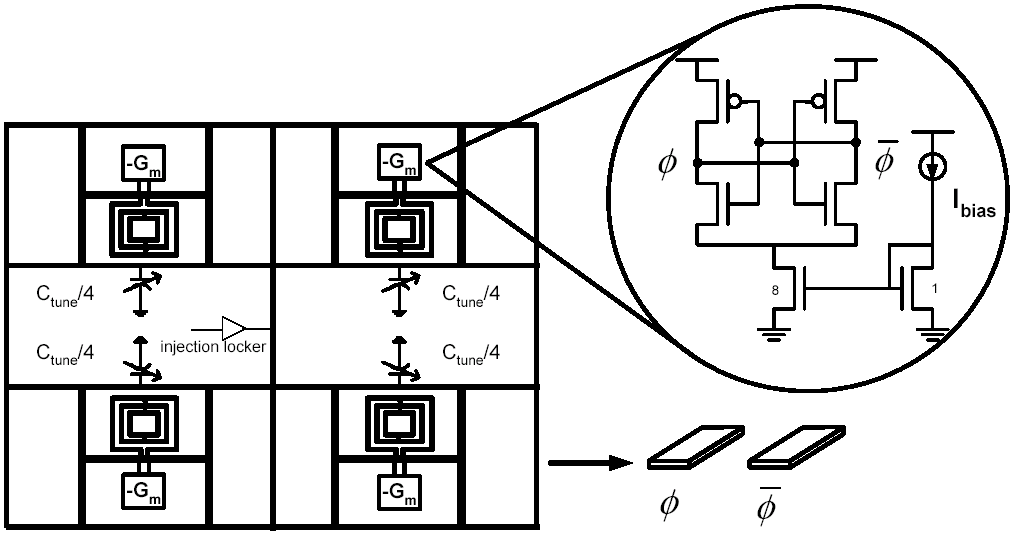


Figure 28.5.1: A distributed differential oscillator global clock network.

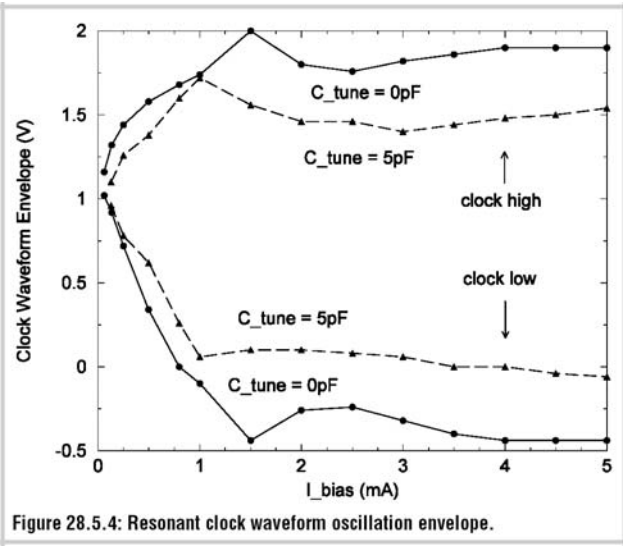


Figure 28.5.4: Resonant clock waveform oscillation envelope.

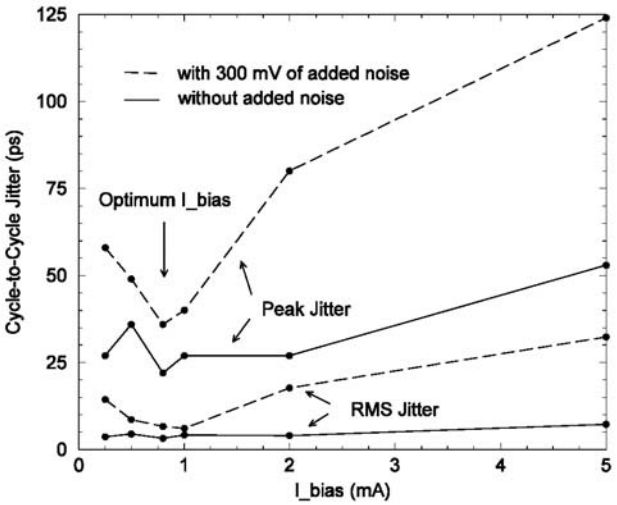
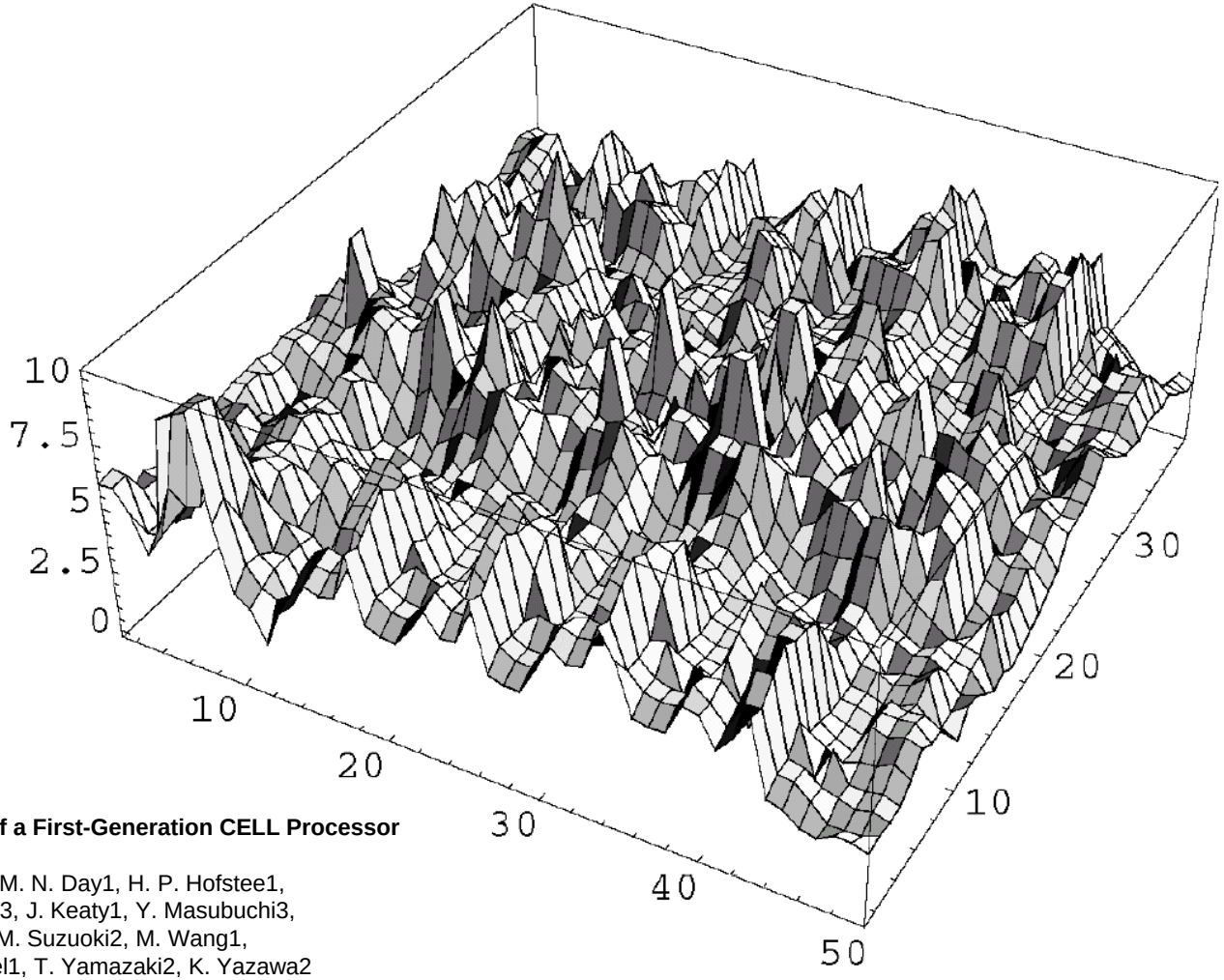


Figure 28.5.5: Resonant clock jitter with and without added supply noise.

Digest of Papers ISSCC 2005
28.5 1.1 to 1.6GHz Distributed Differential Oscillator Global Clock Network
Steven C. Chan1, Kenneth L. Shepard1, Phillip J. Restle2
1Columbia University, New York, NY
2IBM, Yorktown Heights, NY

ISSCC 2005: Clock Skew across CELL Processor
Global Clock Distribution



The Design and Implementation of a First-Generation CELL Processor

D. Pham1, S. Asano3, M. Bolliger1, M. N. Day1, H. P. Hofstee1,
C. Johns1, J. Kahle1, A. Kameyama3, J. Keaty1, Y. Masubuchi3,
M. Riley1, D. Shippy1, D. Stasiak1, M. Suzuoki2, M. Wang1,
J. Warnock1, S. Weitzel1, D. Wendel1, T. Yamazaki2, K. Yazawa2
1IBM, Austin, TX
2Sony, Tokyo, Japan
3Toshiba, Austin, TX

Figure 10.2.2: Clock-skew map.

ISSCC 2005: Optical Clocking

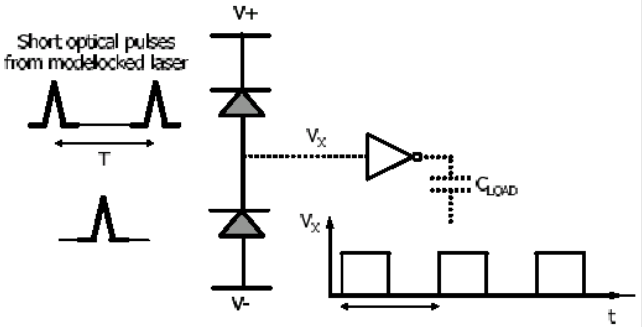


Figure 4.6.3: Generation of electrical clock using reverse biased photodiodes and short optical pulses.

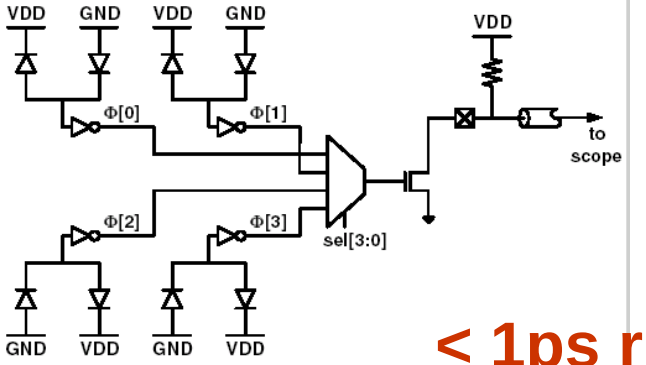


Figure 4.6.4: Optically Injected Clock MUX. The pairs of reverse-biased photodiodes shown are hit by alternating short optical pulses to generate clock signals.

< 1ps rms jitter

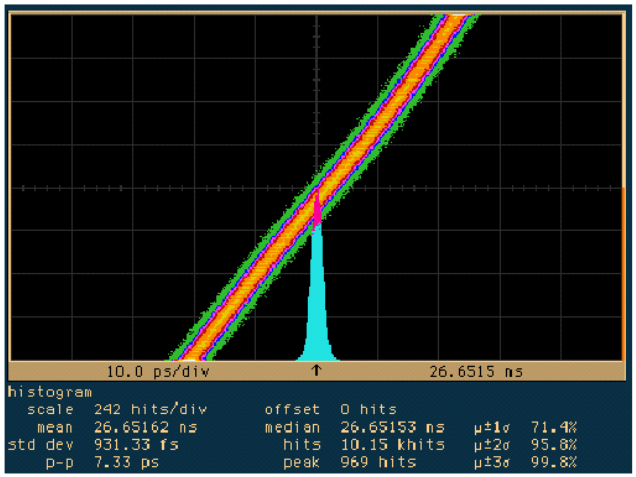


Figure 4.6.5: Jitter histogram for optically-triggered electrical clock output - GaAs PIN detectors driven with 850nm light.

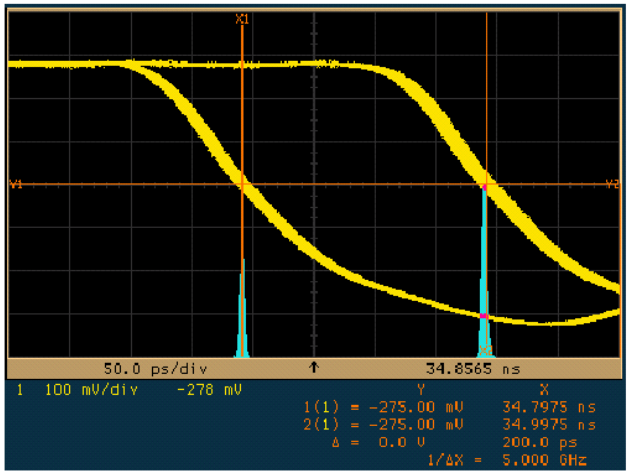


Figure 4.6.6: Phase spacing for optically-triggered electrical clock output.

Diodes are off-chip, receiving laser pulse and driving into mux selctor on-chip … integrated in the future …

Opportunities for Optics in Integrated Circuits Applications
By D.A.B. Miller, A. Bhatnagar, S. Palermo, A. Emami-Neyestanak, M.A. Horowitz
Digest of Technical Papers ISSCC 2005

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Key Learning's

- Choose your skew battles wisely
  - Look at the overall skew and fix it globally if possible.
  - It is okay to be loose in one area if you can gain back in effort, productivity and better design.
  - Getting the design out a quarter earlier at a slightly lower speed wins. There is a 1% "effective" performance loss for every week the schedule slips.
- Minimize if not eliminate interconnect matching requirements
  - Fewer paths to match means fewer things can go wrong
- Make clock distribution more tolerant to design mismatch
  - Don't need to tune each path correct to the last pico-second
- Unit and block clock loading data changes till the last minute
- Final clock loadings can be up to 2.5x the original expectations
- Most practical solutions involve combination of techniques (i.e. global H-tree, local grid …)

Summary

- A successful clock distribution network should:
  - Maintain low skew
  - Be tolerant to design mismatches and deviations from ideality
  - Reduce and or eliminate very careful matching of layouts
  - Reduce or eliminate final tuning effort right before tapeout
  - Reduce / minimize design effort
  - Include ability to be flexible: plan for things to go wrong, and put in place backup solutions.

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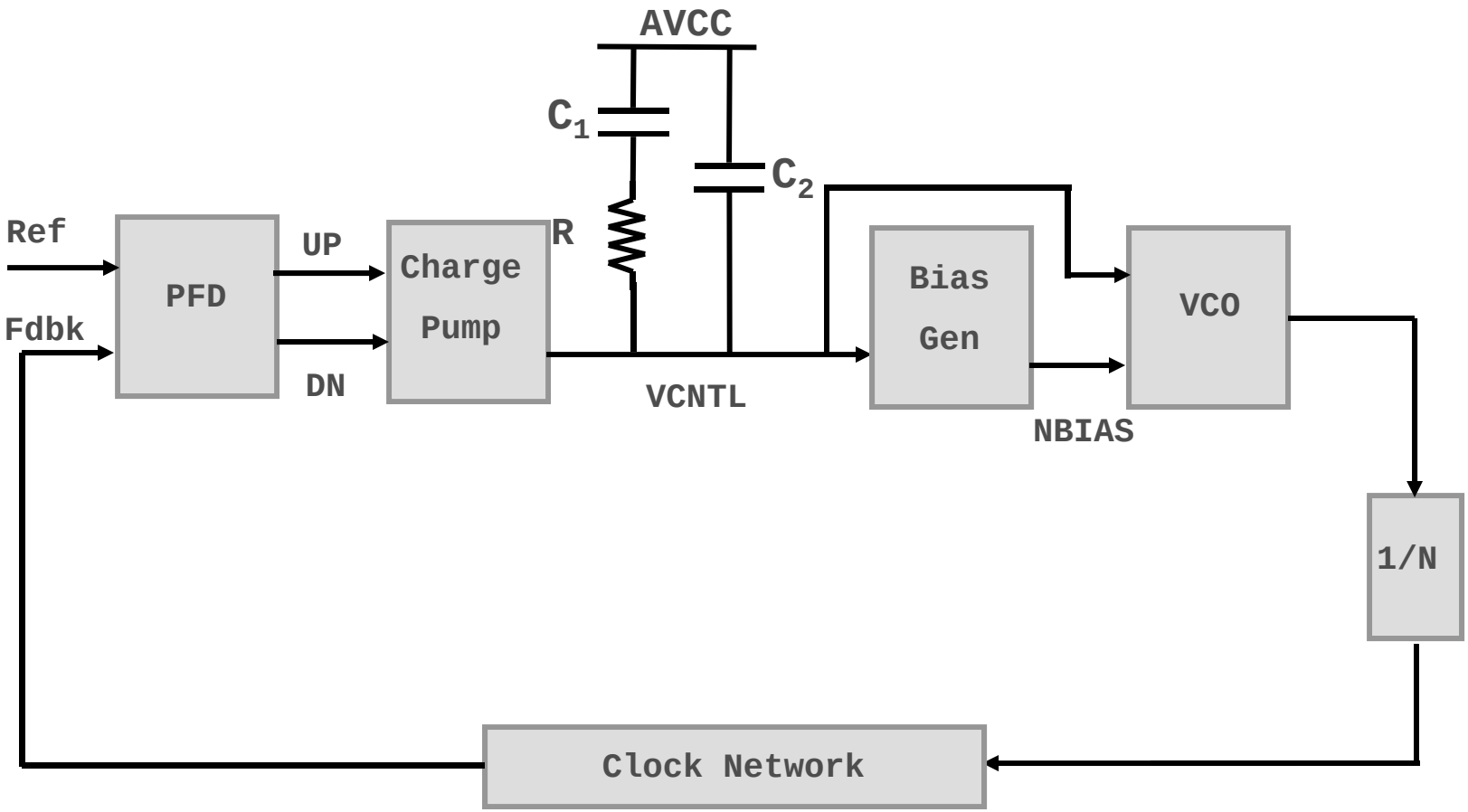
Backup

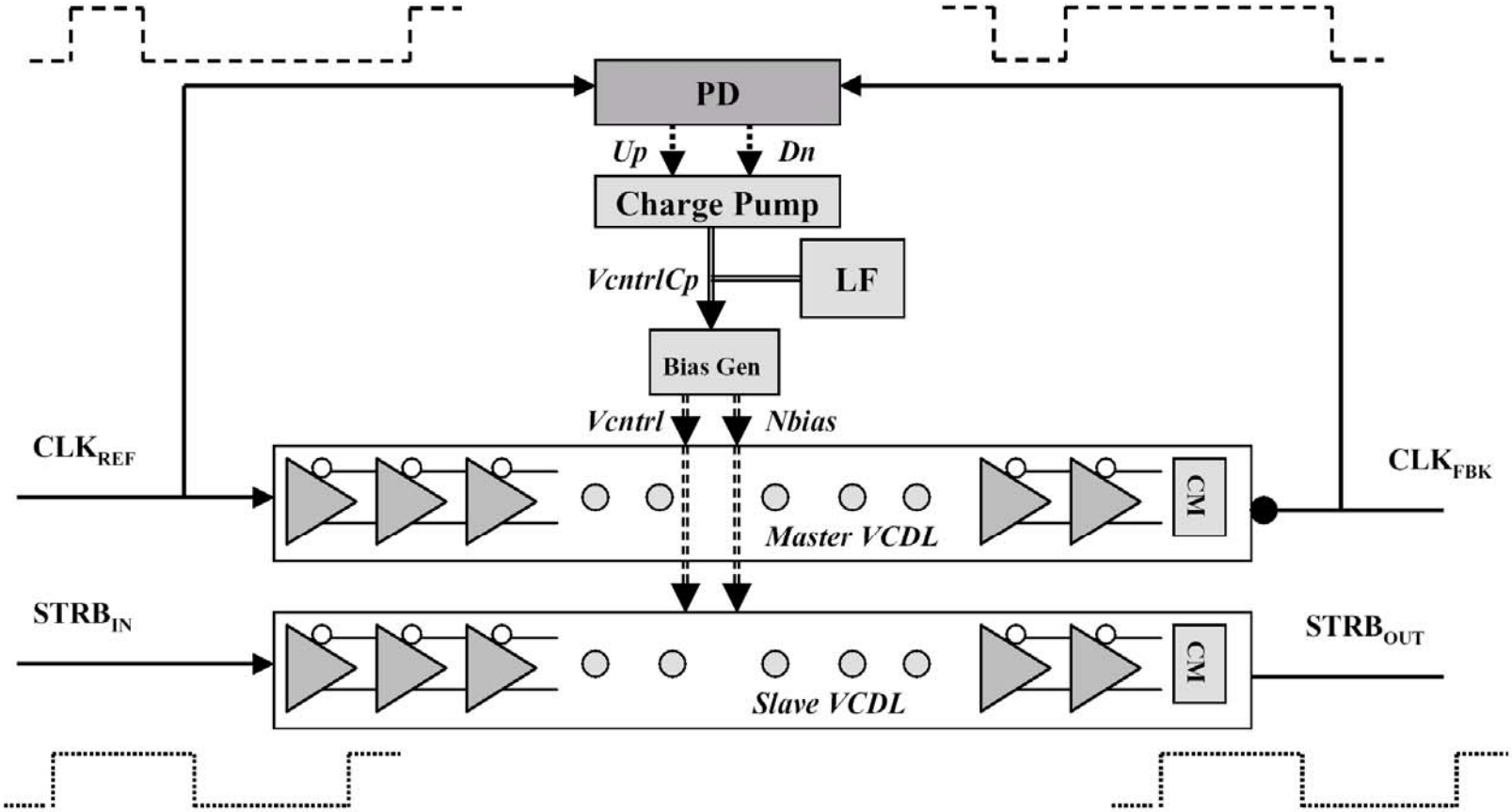
Acronyms

- PLL – Phase Locked Loop
- DLL – Delay Locked Loop
- PD – Phase Detector
- VCO – Voltage Controlled Oscillator
- GCDN – Global Clock Distribution Network
- LCB – Local Clock Buffer
- GCB – Global Clock Buffer
- MIM – Metal-Insulator-Metal
- PD SOI – Partially Depleted SOI
- BT transistor – Body-Tied transistor

Typical 2nd order PLL Block Diagram



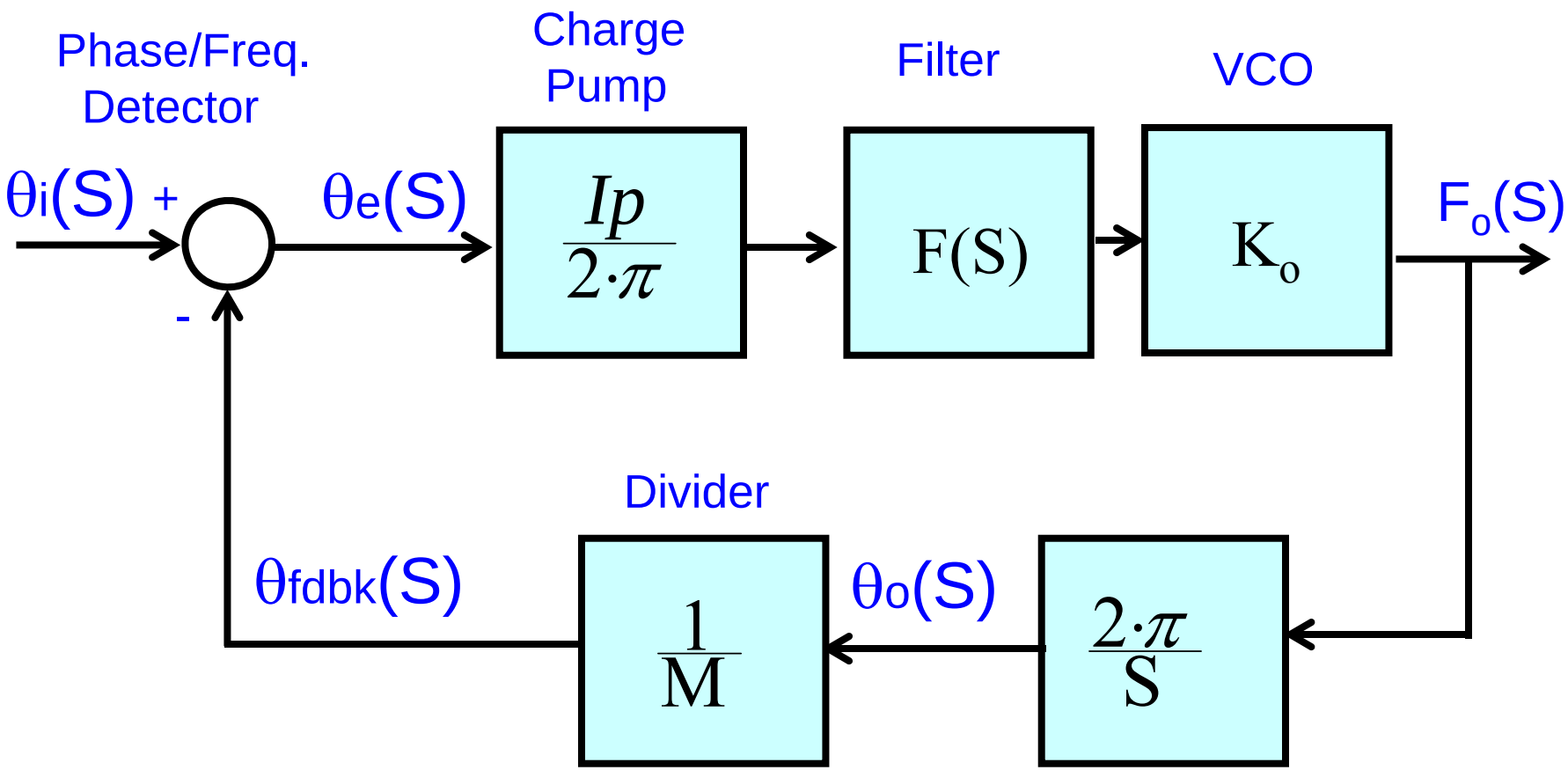
DLL – Delay Locked Loop



PLL Loop Bandwidth vs. Jitter Trade-off

- A low loop bandwidth is desirable to suppress reference clock jitter
- A high loop bandwidth is desirable to track power supply noise
- In general, PLL output jitter is mainly due to power supply noise rather than reference clock jitter (crystal oscillator based)
- Minimize peaking in closed-loop response
- Can use filtering to help reduce jitter due to external power supply noise
  - Dedicated power supply rail
  - LC Filter
  - On-die supply regulation

PLL Analysis: Locked State



PLL Loop Equations

Analyzing the Transfer Function: θo(S) / θi(S)

Loop Natural Frequency (Bandwidth):

$$F_n = \left(\frac{1}{2 \cdot \pi}\right) \cdot \sqrt{\frac{K_o \cdot I_p}{M \cdot C_1}}$$

Loop Damping (First Order Filter):

$$\varsigma = \pi \cdot R \cdot C_1 \cdot F_n$$

PLL Loop Analysis

- Higher VCO Gain (Ko) → More Difficult to Stabilize Loop.
- Loop Bandwidth is chosen based on application and stability limitations.
- Desirable to minimize peaking effect in closed-loop frequency response.
- Under-damping → more frequency overshoot, faster loop response.
- Over-damping →less frequency overshoot, better stability, slower loop response.

PLL Parameters

- PLL Lock Time
  - This is the time it takes for the PLL to achieve steady-state lock condition from power-up.
  - Function of Loop Parameters → VCO gain and loop bandwidth.
  - It is determined by a one-shot measurement of the PLL output clock when the PLL is powered-up.
  - This time is important if the reference clock is dynamically changed during operation, e.g., changing to slow speed clock to reduce power.
- PLL Tracking Range
  - Determines the Min & Max VCO frequency of operation for stable PLL loop.
  - Function of VCO gain characteristics.
  - Determined by sweeping the PLL input frequency and measuring the PLL output frequency.

PLL Parameters

- PLL Frequency Overshoot
  - It is a measure of PLL stability.
  - It is determined by the Filter and the VCO Gain Parameters
  - It is a one-shot measurement of the PLL output clock when the PLL is powered-up.
    - Need to limit the overshoot to prevent erroneous circuit operation.
- PLL Output Jitter
  - Jitter performance is a strong function of PLL loop parameters along with many other sources of noise.
  - Reference clock jitter and power supply noise along with the loop bandwidth also impact PLL output jitter
  - Must consider both high and low frequency content of jitter:
    - Low frequency jitter →jitter is measured over many clock cycles.
    - High frequency jitter → edge-to-edge variations

VCO - Voltage Controlled Oscillator

- There are a number of requirements placed on voltage controlled oscillators used in clock generation circuits:
  - Phase stability
  - Broad tuning (tracking) range
  - Linearity of frequency vs. control voltage
  - Large gain factor K_O

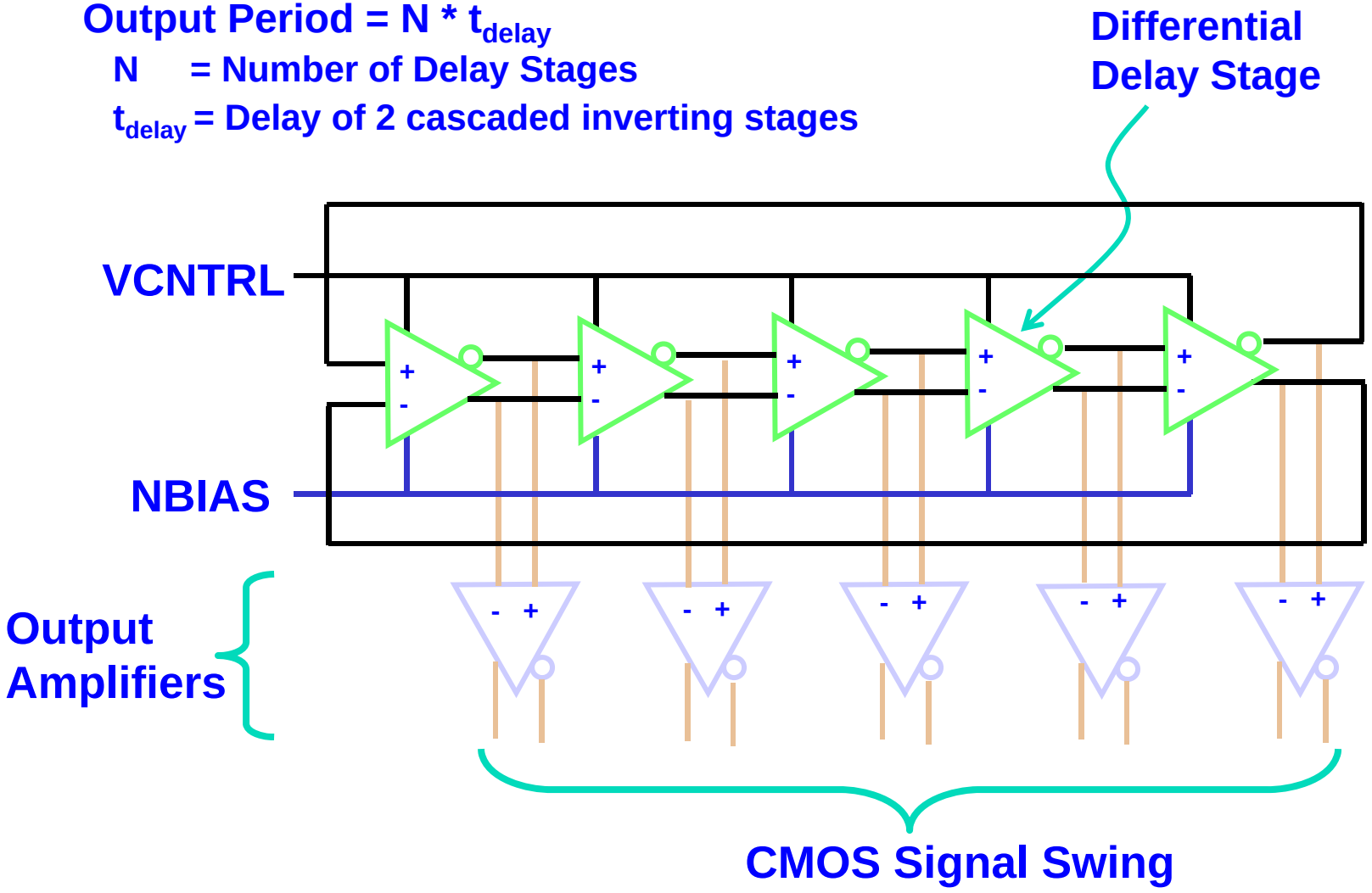
- These requirements are usually in direct conflict with each other.
  - To obtain good wideband features phase stability will be reduced.

Differential VCO

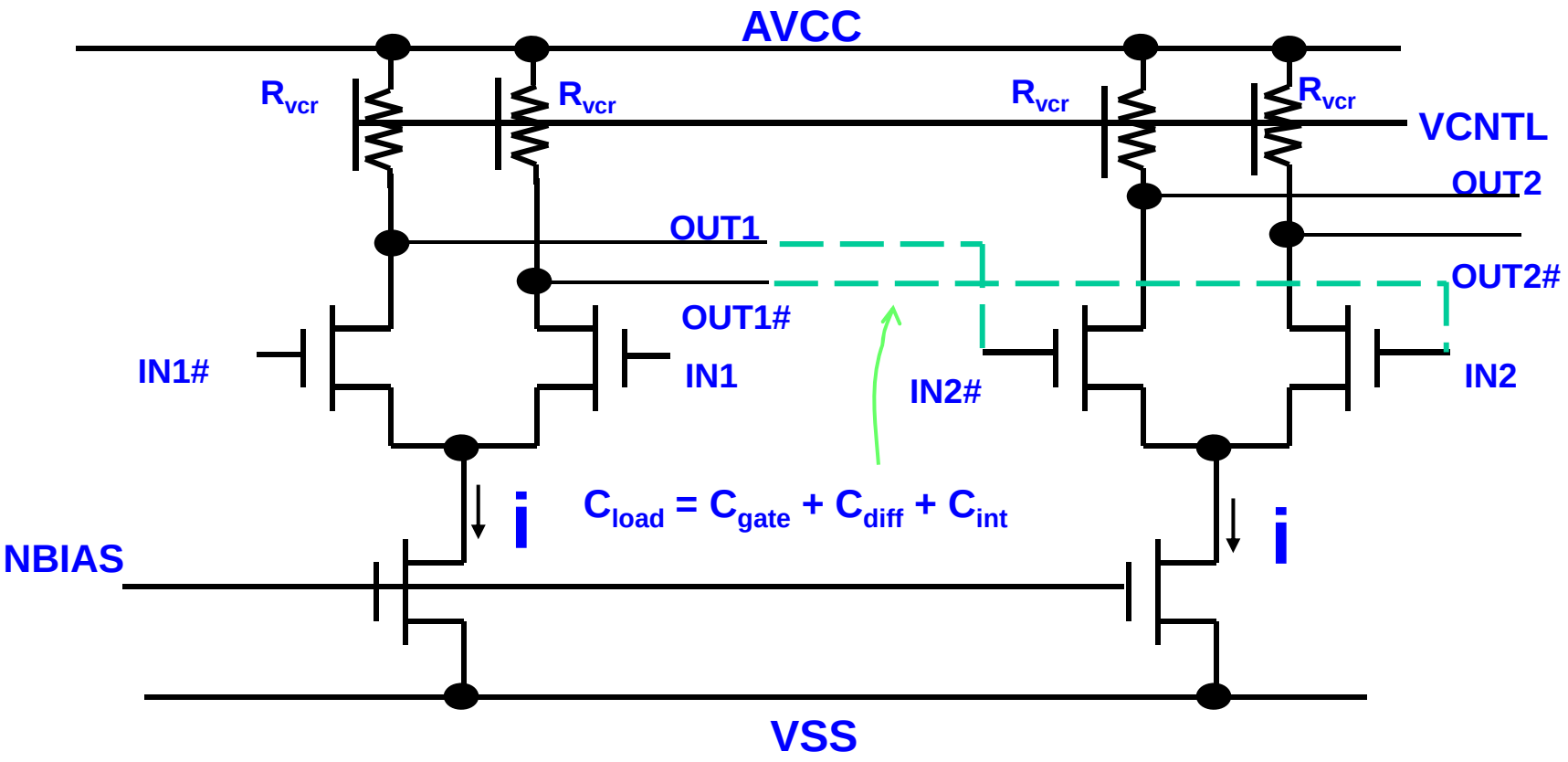
Output Period = N * t_{delay}

N = Number of Delay Stages

t_{delay} = Delay of 2 cascaded inverting stages



Differential Delay Stage



Advantages:

- Differential signals more immune to noise
- Insensitive to switching trip-point inaccuracy

VCO Frequency of Oscillation

$$i = C \cdot \frac{\Delta V}{\Delta T}$$

$$t_{delay} = C \cdot \frac{\Delta V}{i}$$

$$Frequency = \frac{i}{C \cdot \Delta V \cdot N}$$

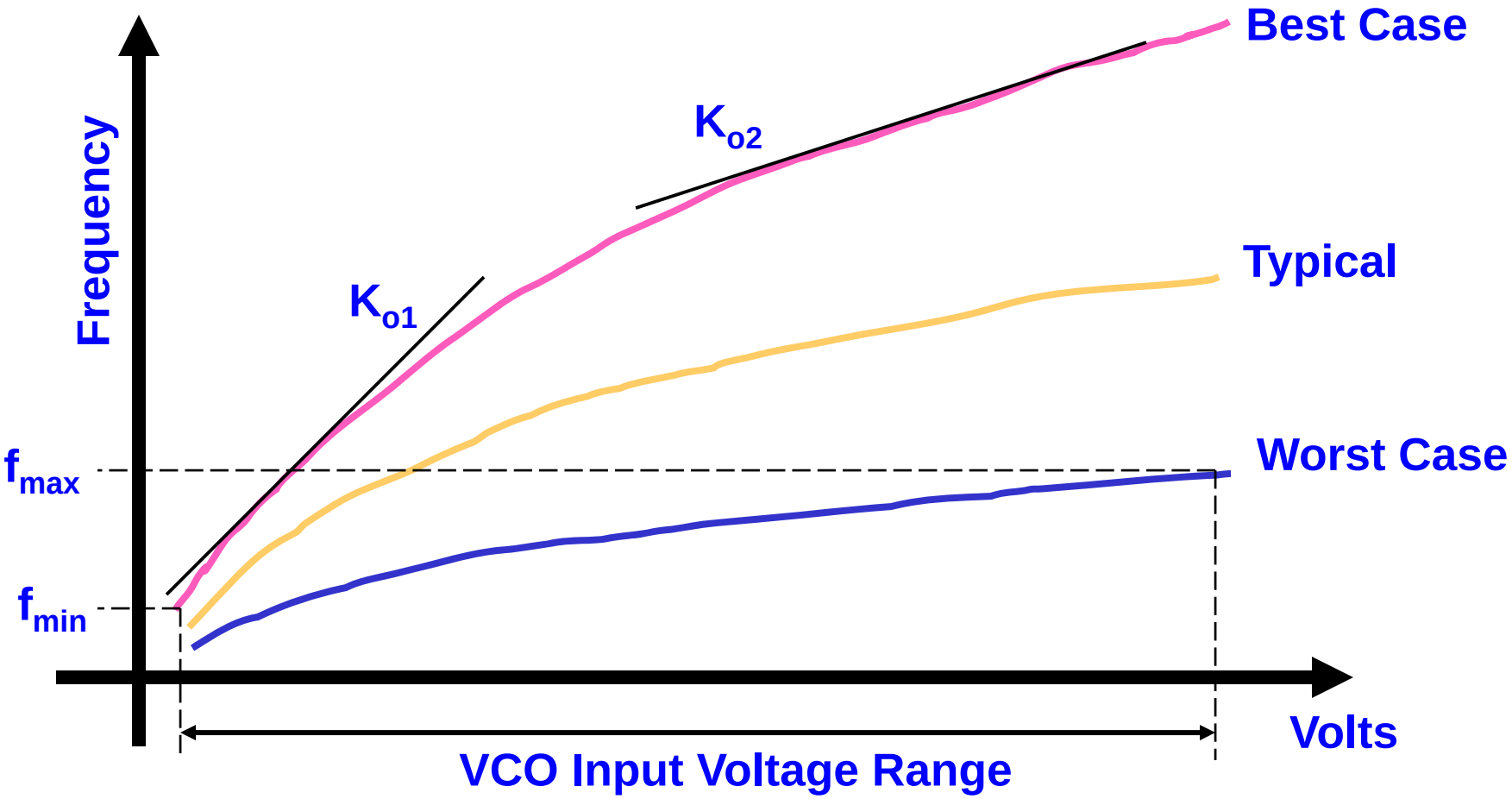
where **N = number of delay stages**

ΔV = Peak-Peak Voltage Swing (AVCC-Vcntrl)

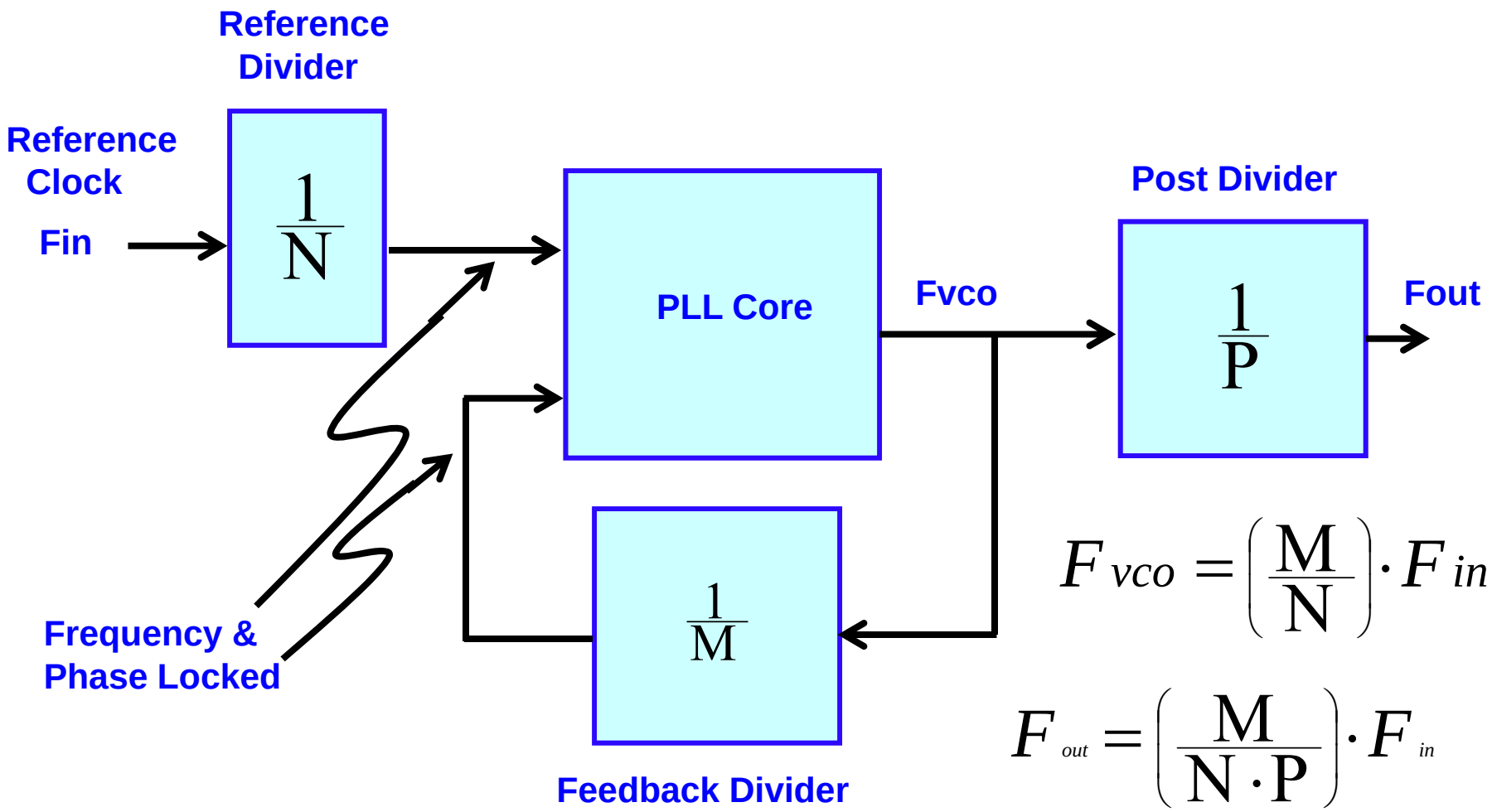
C = total capacitance on output node

i = input current to Ring Osc. (Tail Current)

VCO Transfer Function



PLL Block Diagram



$$F_{vco} = \left(\frac{M}{N}\right) \cdot F_{in}$$

$$F_{out} = \left(\frac{M}{N \cdot P}\right) \cdot F_{in}$$

PLL Reading List

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