Training exercises for VHDL modelling

Course homepage: http://apachepersonal.miun.se/~bentho/vhdwebb/index.htm
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1 Basic elements of VHDL

1.1 Write VHDL code, entity and architecture according to the following description

Entity name: C2_1
Architecture name: A2_1
Input signals: x (integer)
Output signals: z (integer)
Function: The output signal *z* must be assigned *x+10* every time the input *x* changes its value.

1.2 Write VHDL code, entity and architecture according to the following description

Entity name: C2_2
Architecture name: A2_2
Input signals: x, y (std_logic)
Output signals: z (std_logic)
Function: The value corresponding to *x AND y* must be assigned to the output signal *z* every time inputs *x* or *y* change their values.

1.3 Write VHDL code, entity and architecture according to the following description

Entity name: C2_3
Architecture name: A2_3
Input signals: x0, x1 (std_logic)
Output signals: z (std_logic)
Function: The output signal z must be assigned values according to the following truth table. All unspecified states of input signals must result in output signal *z* being assigned to zero.

x0	**x1**	**z**
0	0	1
0	1	0
1	0	1
1	1	1

1.4 Write VHDL code, entity and architecture according to the following description

Entity name: C2_4
Architecture name: A2_4
Input signals: x0, x1, x2 (std_logic)
Output signals: z (std_logic)
Function: The output signal *z* must be assigned the value of a 3-inputs XOR gate.

1.5 Explain the abbreviation VHDL?

1.6 Explain the abbreviation RTL and what is the meaning of RTL?

2 Parallel and sequential data processing

2.1 What is wrong with the VHDL-code below? Suggest how to correct the error.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity exc_F2_2 is
    port (
    a, b, c : in  std_logic;
    x,z: out std_logic);
end  exc_F2_2;

architecture rtl of exc_F2_2 is
begin  -- rtl
  z <= b or c;
  x <= a and b and z;
end rtl;
```

2.2 What will be the value of the output signal z when the inputs (x2,x1,x0) change from (0,1,1) to (1,1,1)?

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity exc_F2_3 is
  port (
    x2, x1, x0: in  std_logic;
    z: out std_logic);
end  exc_F2_3;

architecture rtl of exc_F2_3 is

signal a,b : std_logic;
begin  -- rtl
  z <= x1 and b;
  a <= x0 and x1 and x2;
  b <= a xor x0;
end rtl;
```

2.3 Schedule the driving of the signal for the following process. Assume that a='1', b='0' and x='1' at simulation time 0 ns. At 3 ns, b='1' and at 6 ns a='0' and b='0'

```
process(a,b)
begin
  z <= a or b after 1 ns;
end process;
```

Time	a,b,x	Driving	Comments

2.4 Develop the logical expression for output signal e without minimization.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity exc_F2_4 is
  port (
    a, b, c, d: in  std_logic;
    e: out std_logic);
end  exc_F2_4;

architecture rtl of exc_F2_4 is

signal s0, s1, s2, s3 : std_logic;
begin  -- rtl
  U0 : and2 port map (i0 => a, i1 => b, z  => s0);
  U1 : or2 port map (i0 => a, i1 => b, z  => s1);
  U2 : or2 port map (i0 => s2, i1 => s3, z  => e);
  U4 : cl port map (i0 => a, i1 => s0, i2 => d, z => s2);
  U5 : cl port map (i0 => a, i1 => s1, i2 => d, z => s3);
end rtl;
```

Component name	Logical expression
and2	z = i0 · i1
or2	z = i0 + i1
cl	z = (i0 xor i1) · i2

3 Design of combinatorial networks

4 Design of sequential networks

This document will later be updated!