

# BUILDING DIVIDERS WITH FLIP-FLOPS

## *Basic Designs*

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## SUBTRACT

In this essay, we will introduce two method of building a divider with flip-flops. One is called D flip-flop loop, another is achieved by J-K flip-flops. For a divider, we will discuss the input circuit and output circuit independently. The input circuit may decide the function of the divide (or say the frequency of output signal) and the output circuit may decide the duty cycle of the output signal.

## PREFACE BY THE AUTHOR

Divider is an easy-designed machine, for us, the beginner of digital circuits; we probably need to design some machine that already exists in order to obtain some basic experience. I have just done this work independently and enjoy the happiness of researching for the first time. Thus, I write the easy, in order to remember this milestone story for me and share my achievement with everybody.

## ANNOUNCEMENT

The figures in my essay contain some figures in my professor's lecture slides; please obey the local laws when you copy the figures in my essay for other uses. The basic description of J-K flip-flop dividers and the idea of code system of D flip-flop dividers are my original thought thus there's no reference at the last. All my rights of the essay have been reserved.

## WHAT IS A DIVIDER?

When we study the sequential digital circuit, we must have learnt flip-flops and their functions. A very famous application is that a counter. Probably every professor has shown the example on the left to their students:

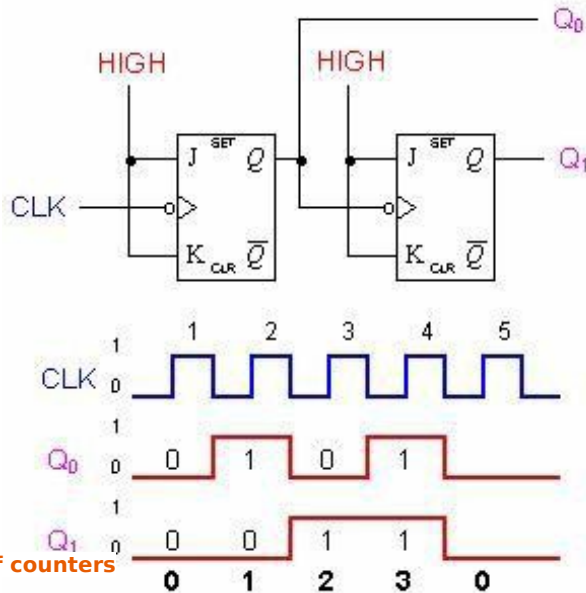


Figure 1 Example of counters

Needless to say, in the circuit, there are just two J-K flip-flops. And if we take account of both outputs of the flip-flops, we can see that the circuit is doing a counting work just like a child to learn how to count: 0,1,2,3 and 0,1,2,3 and 0,1,2,3 ...

Now let's go little further about the example. The only input of the circuit is a square wave with a fixed frequency  $f$ . When we look at the output waves of each output terminal independently, we can easily find that the output  $Q_0$ , and  $Q_1$ , are both a square wave with a fixed frequency  $0.5f$ ,  $0.25f$  respectively.

Then, we can see for output  $Q_0$ , this circuit can be called as half-frequency divider and for output  $Q_1$ , it is called quarter-frequency divider. Thus, we can obtain that the counter and divider is almost the same machine with only difference of output terminals.

## HOW TO DESIGN A DIVIDER?

There are plenty of ways to design a divider with basically elements such as flip-flops and gates. But we should find the element thoughts of a divider. When we are going to design a divider, probably we should find a basic thought. Of course, a divider must be a sequential circuit design (furthermore it is a synchronization circuit), then we should follow the steps of designing a sequential machine.

First, we should think about how many states are there. We can see that the amount of states depends on which frequency of signal you want to obtain (compared with basic frequency  $f$ ).  $0.25f$ ,  $1/3f$ , or even  $1/7f$  (Yeah, we can do that!) for  $0.25f$ , we need 4 states and for  $1/3f$  we need 3 states, then, needless to say  $1/7f$  need 7 states indeed.

Then we can make out a transition table make sure that what will the next-state be in each case and their outputs. The outputs are designed by yourself; however, you can't make them to be all 0 or all 1. Otherwise, you will see that the output signal is not a periodic signal at all the then saying some words such as

In the following parts of the essay, if we don't make an announcement, the letter  $f$  will always mean the basic frequency of the original input signal.

frequency would be meaningless. Still, you can design in which case the output would be 1 and in which case it would be 0. How long does the output being 1 in one cycle would be mentioned as the term 'duty cycle' which means that the ratio of time being 1 in each cycle and the time of one cycle. And we will discuss about duty cycle in detail afterwards.

The following is fairly similar to what we learn from the class. With the help of Karnaugh maps and transition equations, we can derive out the expression of each input and then, we can draw a circuit diagram.

In the following parts of the essay, we will just go little further about it with some classical designs.

## BUILD $1/2^N$ -FREQUENCY DIVIDERS WITH J-K FLIP-FLOP

I strongly recommend you to look back at Figure 1. This is the easiest way to design a divider. We need  $N$  J-K flip-flops to build  $1/2^N$  -frequency dividers. All of them should be cascaded. And the output terminal should be the Q terminal of the last J-K flip-flop.

## BUILD DIVIDERS WITH D FLIP-FLOP LOOPS

### D flip-flop loops

One classical way to build a divider with D flip-flop is known as D flip-flop loop. When designing this kind of dividers, we should follow these steps.

These kinds of circuits, unlike most sequential circuit, contain two parts only: input circuits and output circuits. Thus, the locations of input circuits are different than those in usual sequential circuit. In usual case, there would be input circuits at each input terminal of flip-flops (or say D terminal). But here, no matter how many flip-flops are there, we only need to consider about the input terminal of the first flip-flop. For other input terminals of following flip-flops, we just connect them directly with the output terminal of the previous flip-flops. The output circuits have the same function as in usual case.

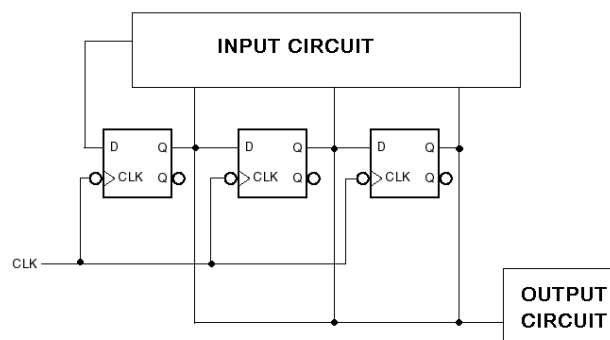


Figure 2 D flip-flop loop

### Procedure of design

First, we should find out a sequence of code that can assigned to each case you've decided to use. For instance, if you decide to build a  $1/5$ -frequency divider,

you ought to design 5 states in your machine. Then, you should assigned one code in your code system to each state. Moreover, all the codes in your code system should be used and each code may be used for only once. However, designing a code system is not that easy as when we design a sequential machine. The code systems we used here are fairly special and shared the same specificity: *a previous code in the system can be obtained by left shift the next code with a supplement bit either '1' or '0'. And for the last one, it should be obtained by left shift the first code.* This condition is really strict and you would be annoyed a lot by this condition when you design your own divider. Such complex code system would ensure that the state of your machine would run in a cycle.

In most cases, we can assign an initial value to each D flip-flop which means that the initial values of the terminal Qs can be assigned to any one state you've assigned with its code. Then, what we should do is just design parts of combinational circuits which make sure that the input of most left D flip-flop can make up the code of next state after one clock cycle.

Last, we should build the output circuit. In some cases, we can use the Q terminal of one D flip-flop as the output terminal. Also, we can build more complex output circuit in order to change the duty cycle.

### Example I: 1/3-frequency divider

First, we should build our own code system. Fairly easy, we can obtain the following one: '00' → '10' → '01' → '00'. Then, we can receive the transition table:

Current State ( $Q_A Q_B$ )		Next State ( $D_B D_A$ )	
0	0	0	1
0	1	1	0
1	0	0	0
1	1	X	X

If you have assigned the code to each case correctly, you may find the  $B=A^*$  (or  $C=B^*$ ,  $D=C^*$ , etc.) and that would be true in all other flip-flops except the first one. Thus, listing the transition table would become meaningless. As we mentioned above, we only focus on the input terminal of first D flip-flop. Probably, we can use a truth table to find next A (or  $D_A$  for avoiding misunderstanding) as the following instead:

Current State ( $Q_A Q_B$ )		Next $D_A$
0	0	1
0	1	0
1	0	0
1	1	X

Then we can draw a Karnaugh map and obtain the input equation:

$$D_A = (Q_A + Q_B)' = Q_A' \times Q_B'$$

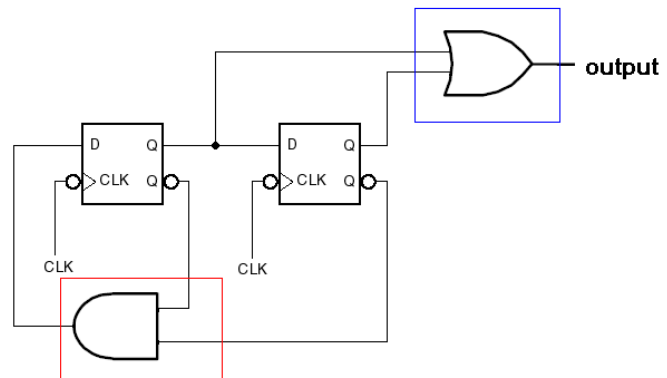
Then, we should decide the output, which decides the duty cycle. Take duty cycle is 66.7% or 2:3, we can obtain a truth table (by this table, we can see that this divider is a Moore Machine):

Current State ( $Q_A Q_B$ )		Output
0	0	0
0	1	1
1	0	1

We suppose  $\text{Output} = Q_A + Q_B$ , thus we have finished all the design step and obtain the whole circuit:

In the red frame, it is input circuit, in the blue frame, it is output circuit.

The CLK signal is the basis signal you want to tackle.<sup>2</sup>



What should we do if **Figure 3 1/3-frequency divider (D Flip-flop, Duty cycle: 66.7%)** we want to change the duty cycle, of course just re-design the output circuit. One of the easiest and the general way is use a multiplexer<sup>3</sup>. Obviously, the current state take the role of selector and the input can be simply got from the output table. The following output table is a divider whose duty cycle is 50%. (From this table, we know that this machine is no longer a Moore Machine but a Mealy Machine instead)

Current State ( $Q_A Q_B$ )		Output
0	0	0
0	1	CLK
1	0	1

If we don't have a multiplexer, then we can do it in a traditional way: use the Karnaugh map to design a combinational circuit with basic elements.

Figure 4 has shown a divider whose duty cycle is 50% that made up by multiplexer. And another method to do so is shown by Figure 5. Figure 5 is just an output circuit which may replace the circuit in blue frame in Figure 4.

<sup>2</sup>If we don't mention in the following parts of essay, CLK signal will always be the basis signal.

<sup>3</sup>The idea of using the multiplexer to do so is fairly familiar; readers can build a divider according to this example. Thus, in the following parts of essay, we won't mention this method again, however, that doesn't mean this method won't work.

A. Code System  
'000' → '100' → '110' → '011' → '001' → '000'

B. Truth Table of both Inputs and Outputs

C. Input equation:  $D_A = Q_B' \times Q_C' = (Q_B + Q_C)'$

Current State (Q <sub>A</sub> Q <sub>B</sub> Q <sub>C</sub> )			Next D <sub>A</sub>	Output (Duty Cycle: 40%)	Output (Duty Cycle: 50%) ~CLK
0	0	0	1	0	0
1	0	0	1	0	0
1	1	0	0	0	0
0	1	1	0	1	1
0	0	1	0	1	1

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## E. Circuit Diagram:

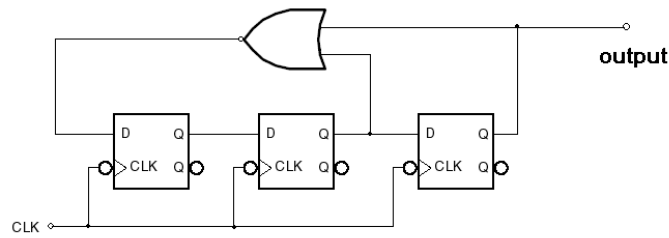


Figure 6 1/5-frequency divider (D flip-flop, Duty cycle: 40%)

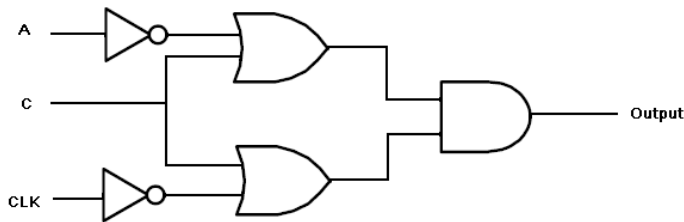


Figure 7 Output circuit for 1/5-frequency divider (D flip-flop, Duty cycle: 50%)

## Example III: Input circuits for 1/7-frequency and 1/13-frequency divider

## A. Code System

For 1/7-frequency divider:

'000' → '100' → '010' → '101' → '110' → '011' → '001' → '000'

For 1/13-frequency divider:

'0000' → '1000' → '0100' → '1010' → '0101' → '0010' → '1001' → '1100' → '1110' → '1111' → '0111' → '0011' → '0001' → '0000'

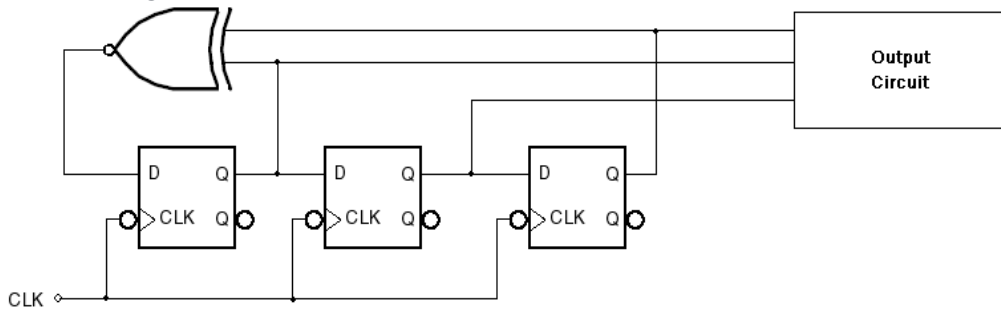
B. Truth table for Next D<sub>A</sub>

Current State (Q <sub>A</sub> Q <sub>B</sub> Q <sub>C</sub> )				Next D <sub>A</sub>
0	0	0	0	1
1	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	0	0	0
0	1	1	0	0
0	0	1	1	0
0	0	0	1	0

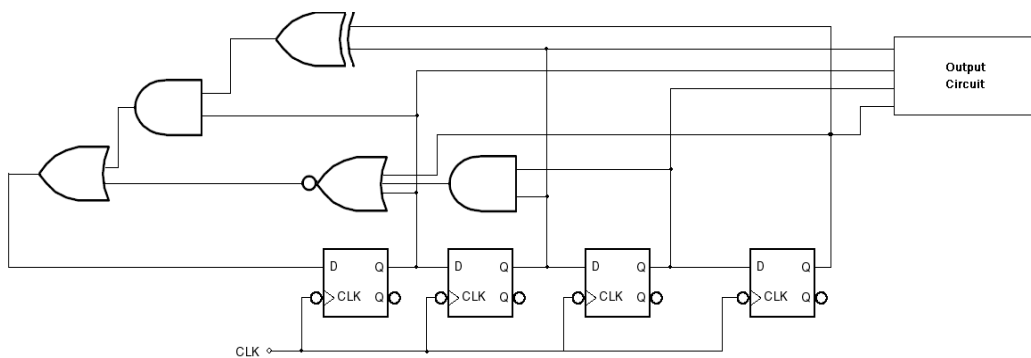
Current State (Q <sub>A</sub> Q <sub>B</sub> Q <sub>C</sub> Q <sub>D</sub> )				Next D <sub>A</sub>
0	0	0	0	1
1	0	0	0	0
0	1	0	0	1
1	0	0	1	0
0	1	0	0	0
0	0	1	0	1
1	0	0	1	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	0
0	1	1	1	0
0	0	1	1	0
0	0	0	1	0
0	0	0	0	1



- C. Next  $D_A = Q_A \text{ XNOR } Q_C$  (for 1/7-frequency divider)  
 Next  $D_A = (Q_A + Q_D + Q_B \times Q_C)' + Q_A \times (Q_B \text{ Xor } Q_D)$   
 D. Circuit Diagram:



**Figure 8 1/7-frequency divider (D flip-flop)**



**Figure 9 1/13-frequency divider (D flip-flop)**

## BUILD DIVIDERS WITH J-K FLIP-FLOPS

### Basic thought

In Figure 1, we have shown a counter (divider) made up with J-K flip-flop. In fact not only do  $1/2^N$ -frequency dividers can be seemed as a counter, but also all dividers made up with J-K flip-flop. For a 1/3-frequency divider, we need to count three number each time, or '00'  $\rightarrow$  '01'  $\rightarrow$  '10'  $\rightarrow$  '00'. As the D flip-flop loops, we should design an output circuit in order to decide the duty cycle of the output signal. However, in J-K flip-flop divider, the input circuit could be very complicated. Since we should not only decide the input of the first flip-flop but also the inputs for other flip-flops. The input of each flip-flop may be decided by you as well but should have the same function which ensures the combinational output of each flip-flop keeping on counting a cycle.

### Procedure of design

First, we should decide how we count. Unlike the case of D flip-flop loop, the order of counting has no limitation. You can follow your favor.

Then you can obtain a transition table, and see what would  $J_n$   $K_n$  be at state  $n-1$ . Then, just as when we design a sequential circuit, we should use Karnaugh map to get the input equation of each J-K flip-flop.

You may think that the analysis would be too complex since you may use  $n$ -variable Karnaugh map for  $2n$  times. However, the struggle for making out a code

system would be vanished. Sometimes, in order to make the designing more easily, we connect J terminal and K terminal of a flip-flop together and then the designing would be little easier. When the output of the flip-flop remains to the previous state, the input ought to be one, otherwise it would be zero. Then we need only to use Karnaugh Map for n times. Sometimes if the output of the flip-flop doesn't contain the unit 'X→0→0→X', then you can connect the J terminal with the HIGH signal directly. Similarly, the K terminal can be connected with the HIGH signal directly if the output of the flip-flop doesn't contain the unit 'X→1→1→X'.

### Example IV: 1/3-frequency divider

We need 2 flip-flops to obtain the final results, and suppose our count order is '00→01→10', then we can obtain the following transition table:

Current state (Q <sub>A</sub> Q <sub>B</sub> )	Next J <sub>A</sub>	Next K <sub>A</sub>	Next Q <sub>A</sub>	Next J <sub>B</sub>	Next K <sub>B</sub>	Next Q <sub>B</sub>
0 0	0	1	0	1	1	1
0 1	1	1	1	0	1	0
1 0	1	1	0	0	1	0

Although you can fill in the column Next J<sub>A</sub>, K<sub>A</sub>, J<sub>B</sub>, K<sub>B</sub> now by the truth table of J-K flip-flop, that would make the problem become little complicated. By observing the cycle of Q<sub>A</sub> and Q<sub>B</sub>, we see that the cycle of Q<sub>A</sub> is '0→1→0→0→1→0', we can see that the cycle contains the unit 'X→0→0→X', thus, K<sub>A</sub> terminal can be connected with the HIGH signal directly. For the same reason, the cycle of Q<sub>B</sub> doesn't contain 'X→1→1→X', that is to say, the K<sub>B</sub> terminal may be connected with signal HIGH directly. Then, according to the truth table of J-K flip-flop, we can decide the value of J<sub>A</sub> and J<sub>B</sub>.

In this example, the value of K<sub>A</sub> and K<sub>B</sub> has been fixed. Then we may consider the input equation of J<sub>A</sub> and J<sub>B</sub>. By Karnaugh map, we can get

$$J_A = Q_A + Q_B$$

$$J_B = (Q_A + Q_B)' \text{ or } J_B = J_A'$$

Thus, the circuit diagram can be drawn as:

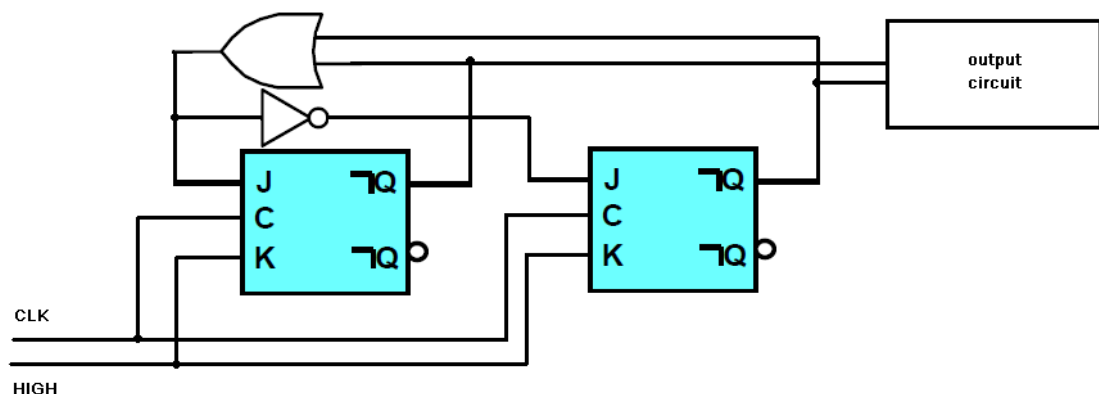


Figure 10 1/3-frequency divider (J-K flip-flop)

### Example V: 1/5-frequency divider

Current state ( $Q_A Q_B Q_C$ )			Next $Q_A$	Next $Q_B$	Next $Q_C$	
0	0	0	0	0	1	
0	0	1	0	1	0	
0	1	0	0	1	1	
0	1	1	1	0	0	
1	0	0	0	0	0	

Current state ( $Q_A Q_B Q_C$ )			Next $J_A$	Next $K_A$	Next $J_B$	Next $K_B$	Next $J_C$	Next $K_C$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	0	0	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	0	1

The transition table and the input table have been already shown above. There is only one thing to say, when decide the value of  $J_B$  and  $K_B$ , we can see that the units, both ' $X \rightarrow 0 \rightarrow 0 \rightarrow X$ ' and ' $X \rightarrow 1 \rightarrow 1 \rightarrow X$ ' can be found. Then, we can connect the  $J_B$  and  $K_B$  together, once the output changes, the input should become both '1', otherwise, they remain both '0'.

Then, we can derive out the input equations:

$$J_A = Q_B \times Q_C \text{ and } K_A = \text{HIGH}$$

$$J_B = K_B = Q_B \text{ XNOR } Q_C$$

$$J_C = Q_A' \text{ and } K_C = \text{HIGH}$$

Then, the circuit diagram is:

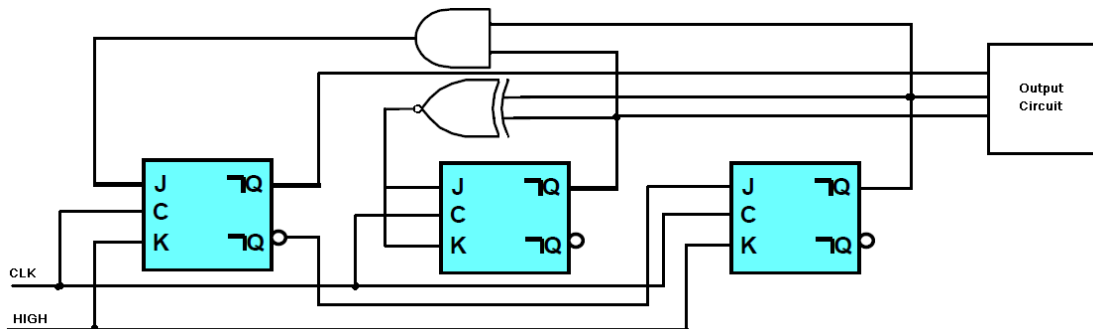
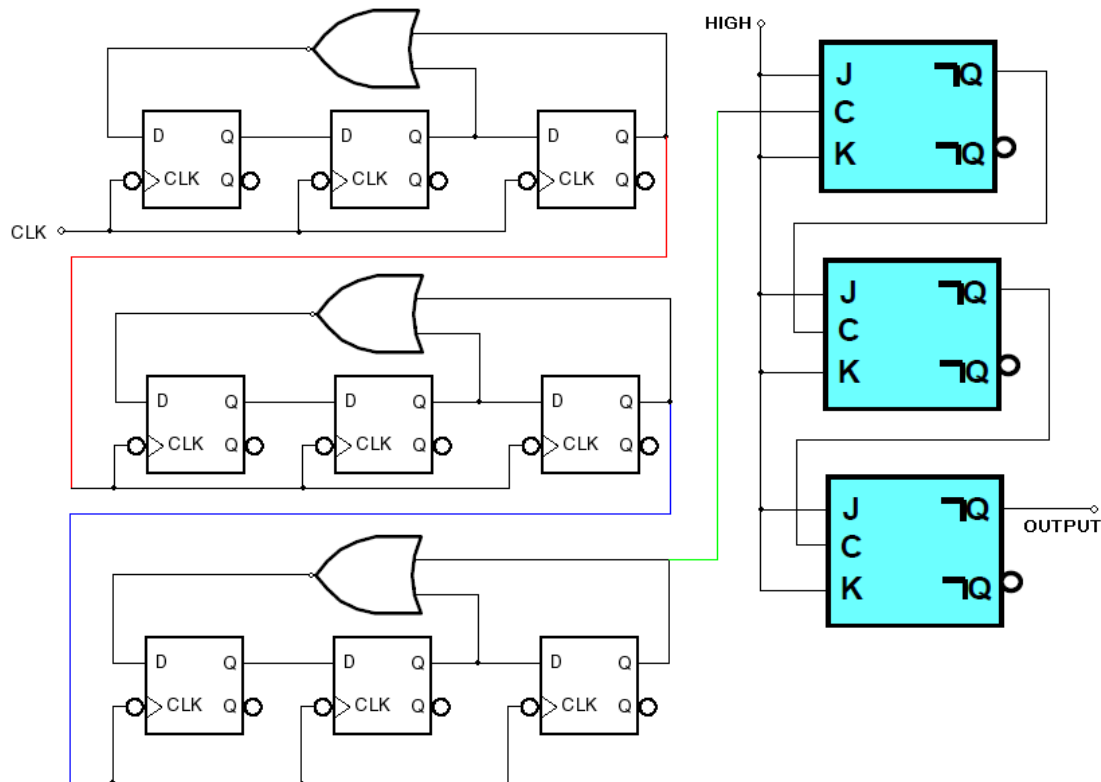


Figure 11 1/5-frequency divider (J-K flip-flop)

### CASCADE

Just like the cascaded transistor circuit,  $A_v = A_{v1} * A_{v2} * \dots * A_{vn}$ , the function of the dividers may be integrated as a bigger one. A half-frequency divider cascade with a 1/3-frequency divider can be used as a 1/6-frequency divider. Thus, if we want to change a 1 KHz square frequency to 1 Hz square frequency, since  $1000 = 5 * 5 * 5 * 2 * 2 * 2$ , we can just cascade 3 half-frequency divider and 3 1/5-frequency divider. The output of the previous level divider should be connected with the terminal CLK in all the circuit diagrams above.

## Example VI: 1/1000-frequency divider



**Figure 12 1/1000-frequency divider (duty cycle: 50%)**

As we mentioned above, in figure 12, on left there are three 1/5-frequency dividers cascaded here, and on the right, there is one 1/8-frequency divider. The red, blue and green lines are connections between each level. However, the output of each level has a limitation: *there can only be one '1' and one '0' in each cycle of the output signal*. The duty cycle of the output signal namely the signal we obtained at last is depend on the output circuit of the last divider only.

## LAST PART

On account of the limitation of my knowledge of digital circuit and English, this essay probably may contain huge amount of mistakes. I hope readers may point them out and tell me with my E-mail account: [shengchenli@hotmail.com](mailto:shengchenli@hotmail.com). And thanks for my father and Mr. Zhu Xiaoming provide me some basic idea of divider. And thanks for my professor Paula, all the figures contain the pictures on her lecture slides, which save a lot of my time. If my essay can give some help to ones who are studying the digital circuit, I would be very pleased. I am still a student and I am going to continue my study in my University and some further module on digital designing is waiting for me. And I hope I can have time to supplement this essay later after my studying has finished.

## REFERENCE

1. Figure 1 are copied from the slides of my teacher's, Paula's, lecture slide. And all the pictures of gates and flip-flops are part of the content of the lecture slides as well.
2. The basic idea of D flip-flop is introduced by Mr. Zhu.