ESY-Lab WS15/16
Project

Group 6
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CONTENT

1. General Description

Topic: *"Musical Note Generator"*

Development board: Xilinx Virtex5 LX50T FPGA
Platform: Linux OS

System requirements

★ *Functional*

+ Be able to display tone's name on LCD
+ Change the key number using JOYSTICK (Up/ Down buttons)
+ Generate piano notes (range 40 - 55)
    - Playing sound when pressing the button
    - Muting sound when releasing

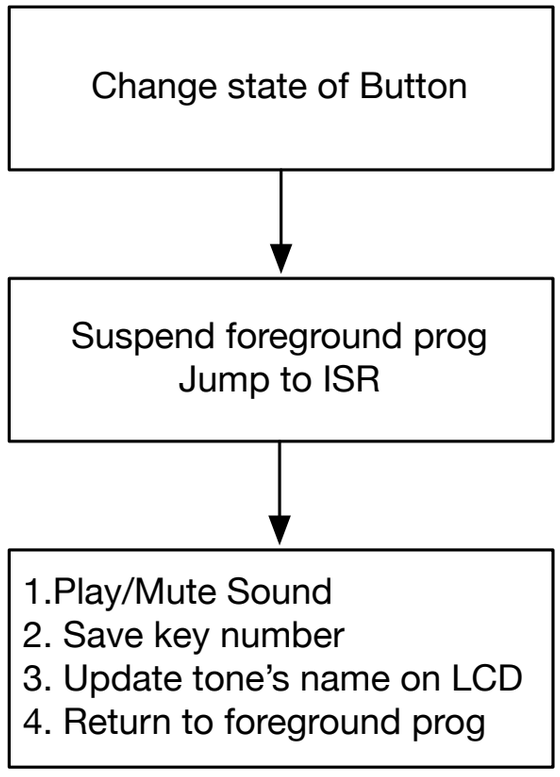
★ *Non-functional*

- Using square wave form to generate sound
- Storing sample numbers of corresponding notes on ROM

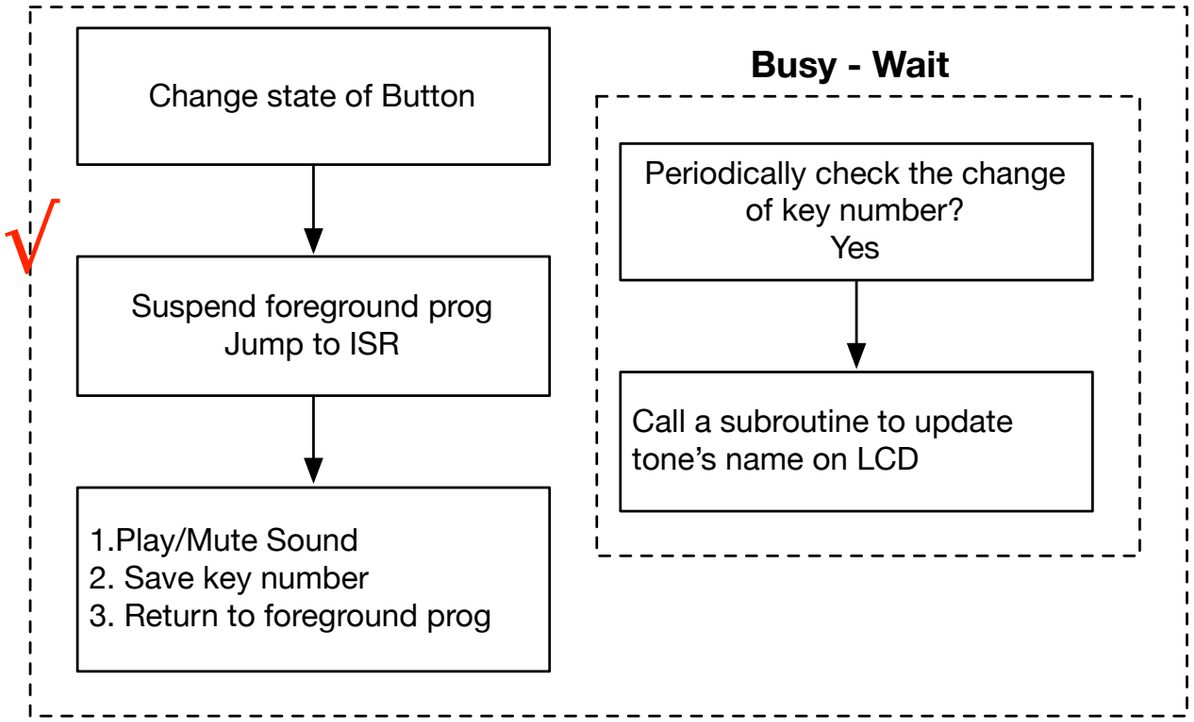
1. General Description

Topic: *"Musical Note Generator"*

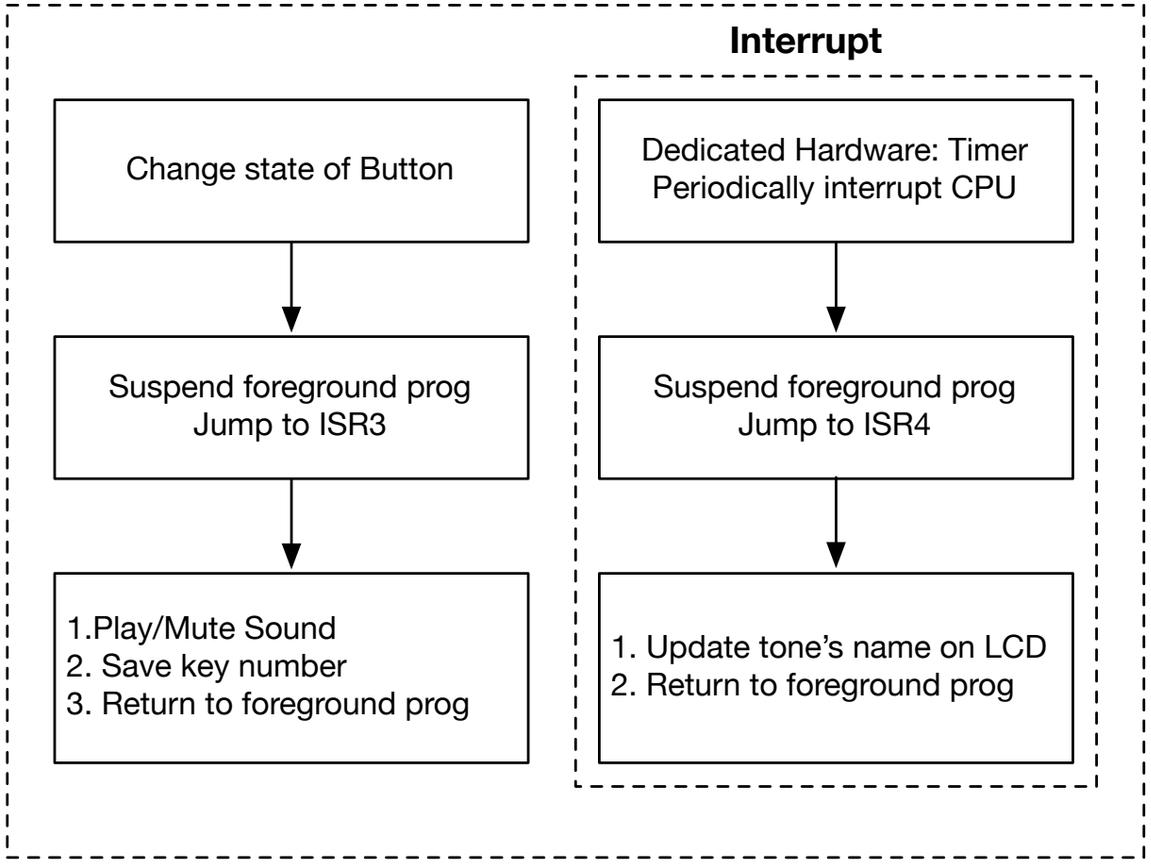
How does it work?



1st Option √

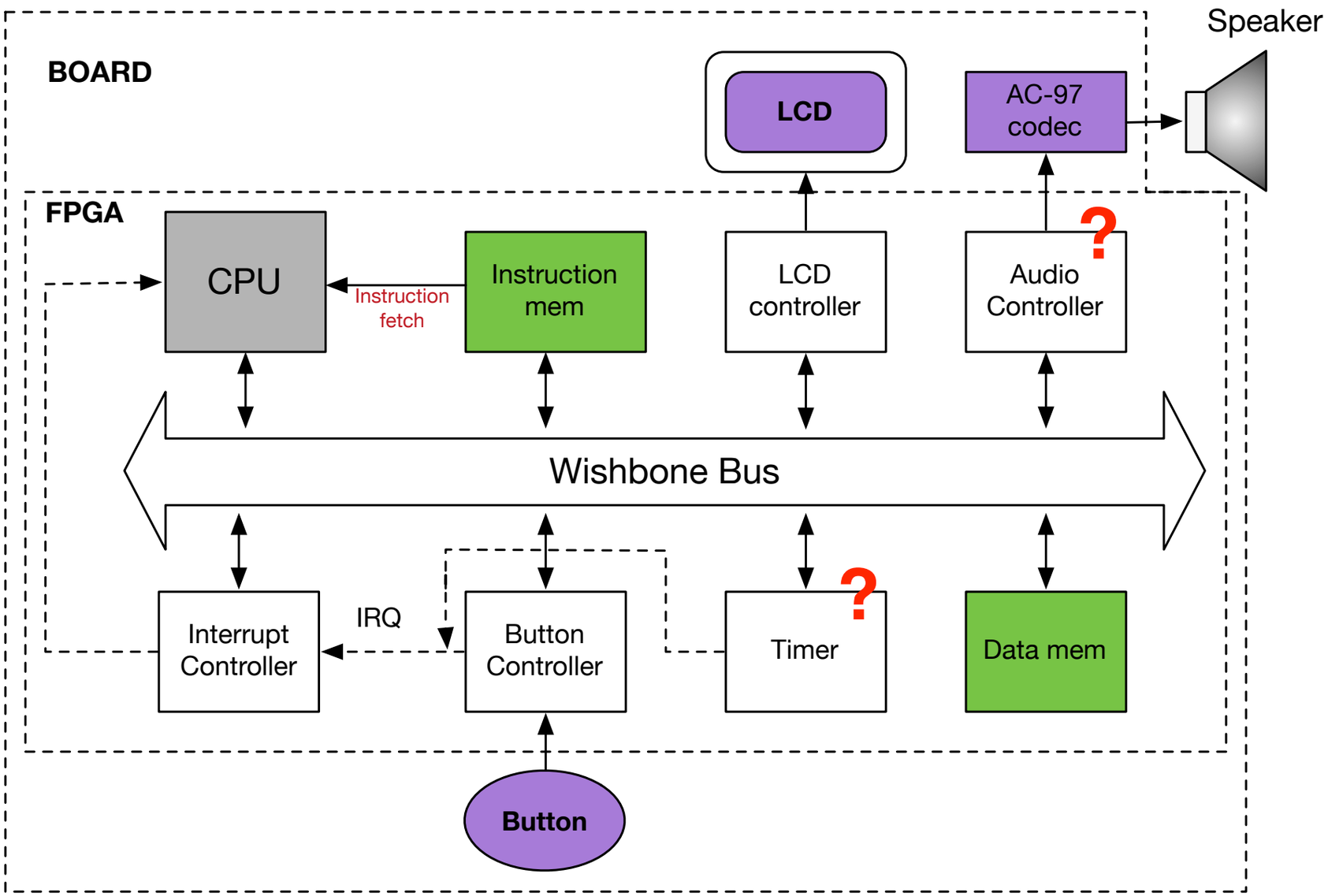


2nd Option



2. Architecture

Harvard Architecture



2.1. Hardware Implementation
2.1.1. Audio Controller

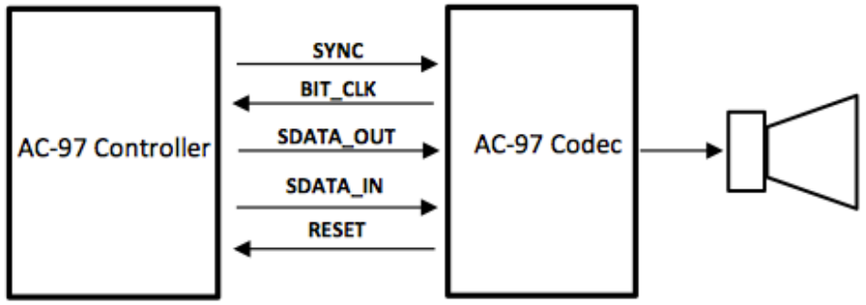
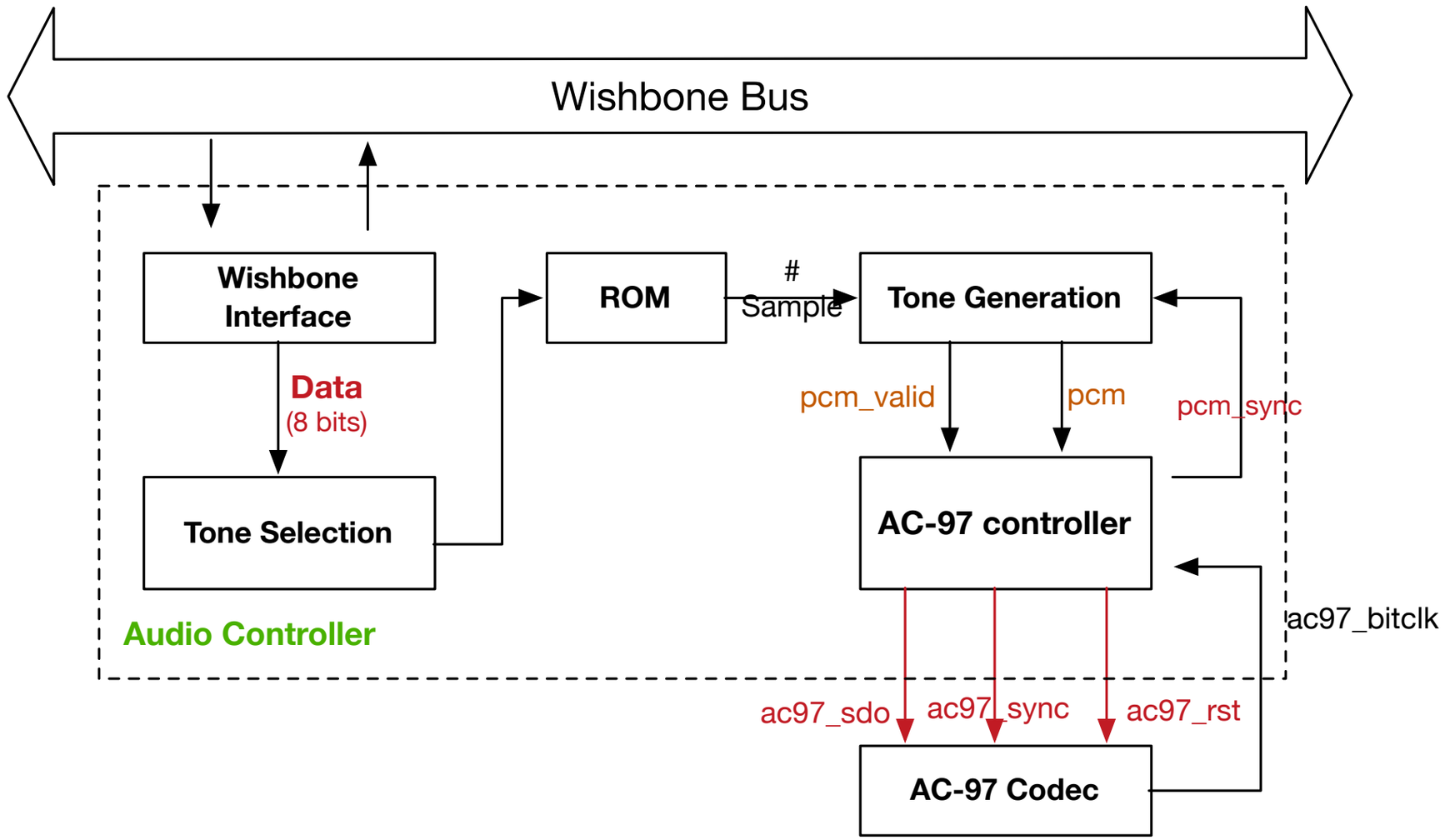
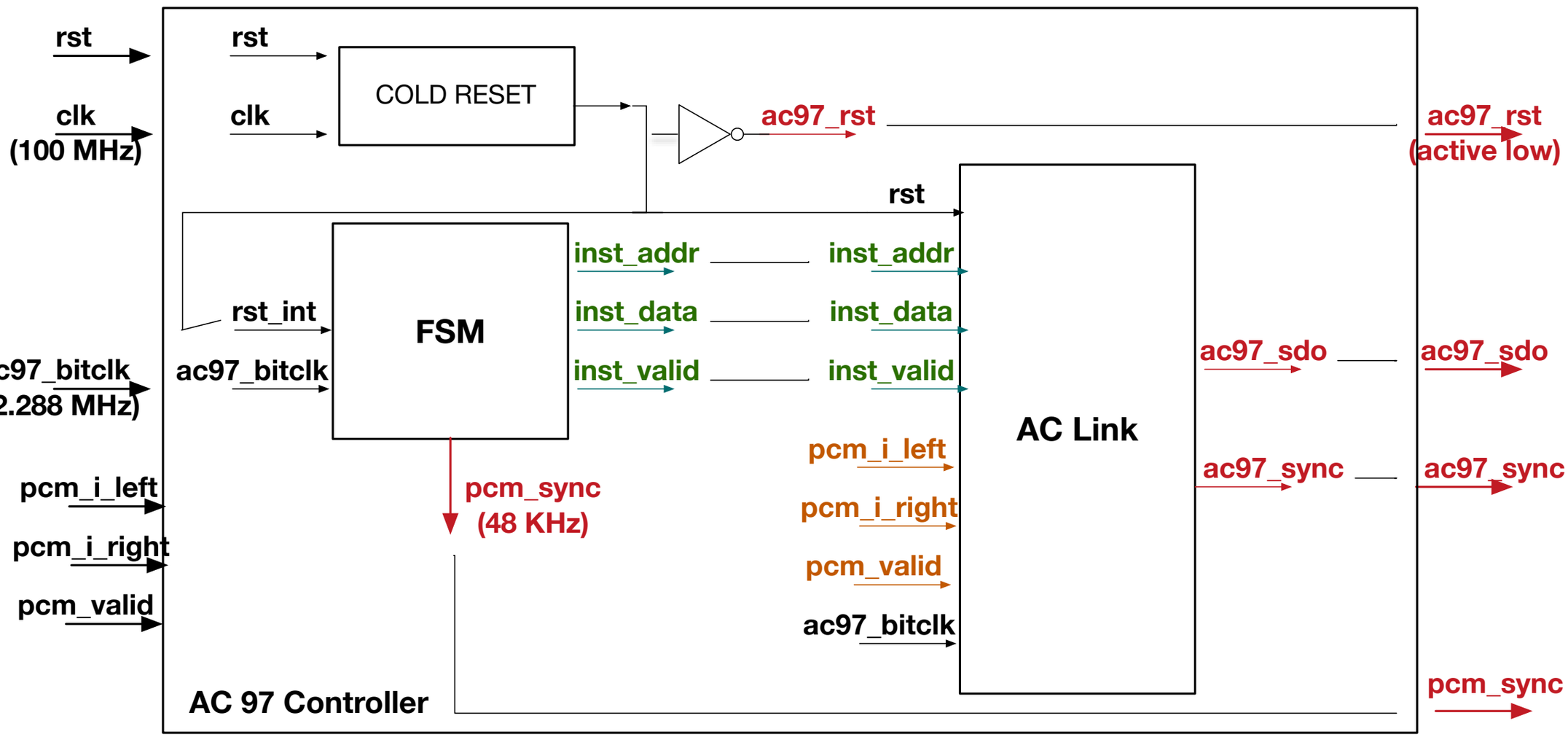


Fig. 1. AC-97



2.1. Hardware Implementation
2.1.1. Audio Controller

AC 97 Controller



2.2. Software Implementation

Two approaches under consideration

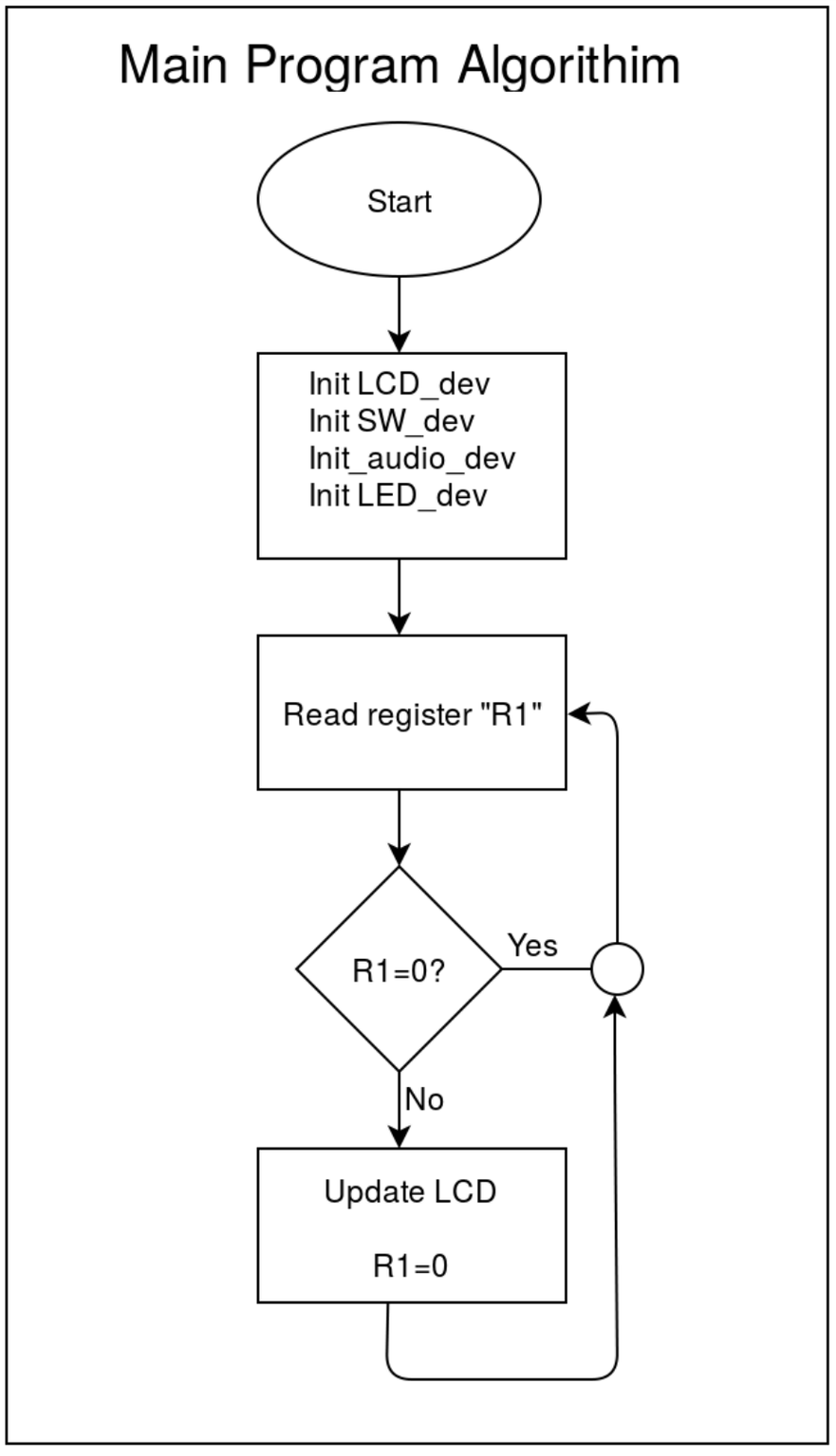
No change in LCD H/W

Tight demands on assembly code due to limited PC relative addressing

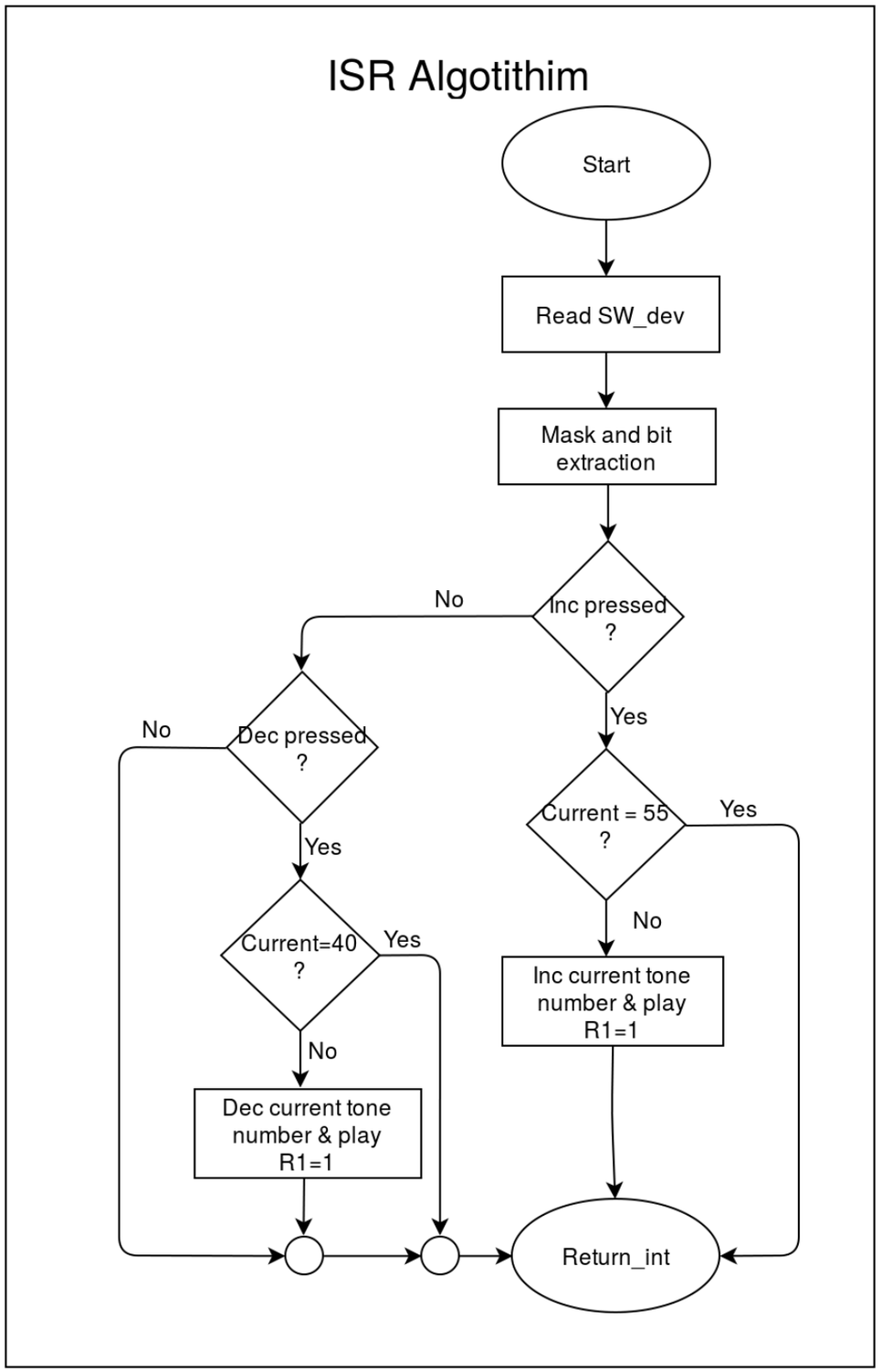
Change LCD H/W

Flexibility in assembly code making LCD H/W vulnerable to errors

2.2. Software Implementation



2.2. Software Implementation



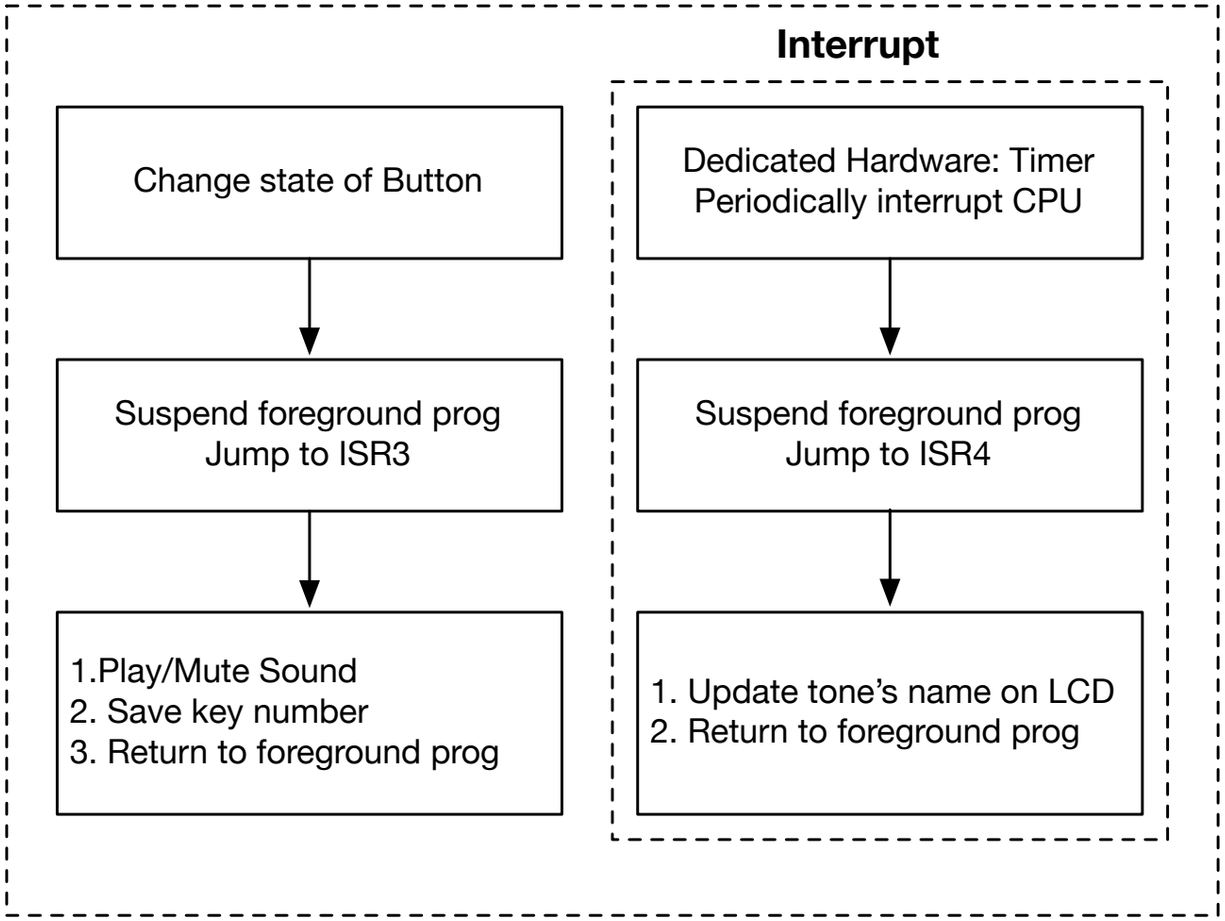
Future Extension

Currently Busy-wait is used in main program

Busy-wait is inefficient in terms of power and processor utilization

To make system energy efficient => We can use a dedicated HW - "**Timer**"

Timer will periodically interrupt the CPU to update current tone on LCD



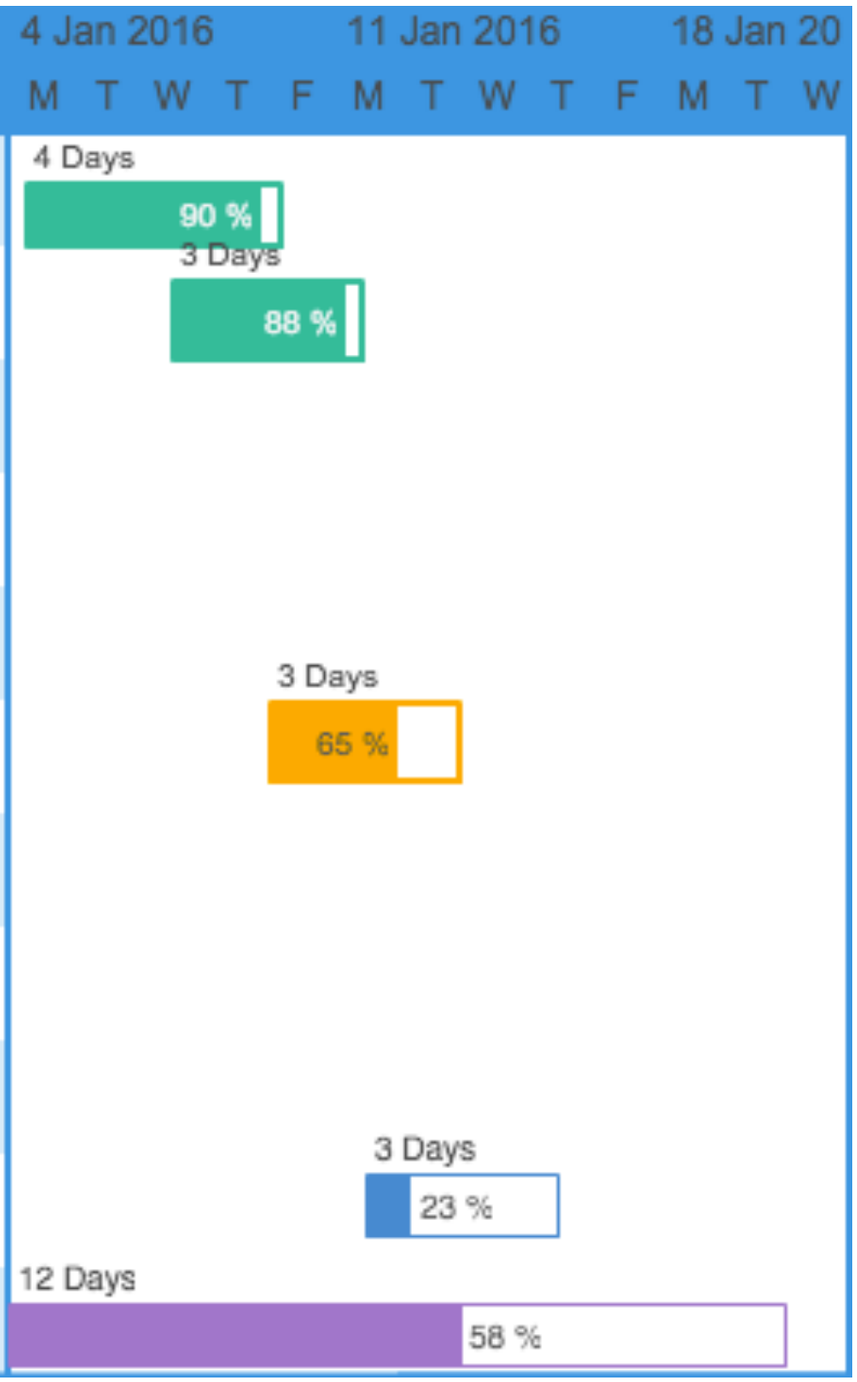
3. Verification Plan

Two stages of verification:

- Module level: Create each module and simulate its functionality independently using ISIM
  - AC-Link block
  - AC-97 Controller
  - Audio Controller
- System level: Integrate modules with the system and check the functionality

4. Time Schedule

ID	Task Name	Duration
1	Preliminary Study	4 days
2	Hardware implementation	4 days
2.1	AC-Link module and AC-97 Controller	
2.2	Audio Controller	
2.3	Testing	
3	Software implementation	3 days
3.1	LCD interface	
3.2	Button and audio interface	
3.3	Testing	
4	Testing the system	3 days
5	Miscl.	3 days



5. Work Distribution

Waseem Hassan	Trung C. Nguyen
Software Implementation (Timer Implementation)	Hardware Implementation
Testing	

Question ?