

"CompRunner" ISS/RTL Runtime Verification Environment

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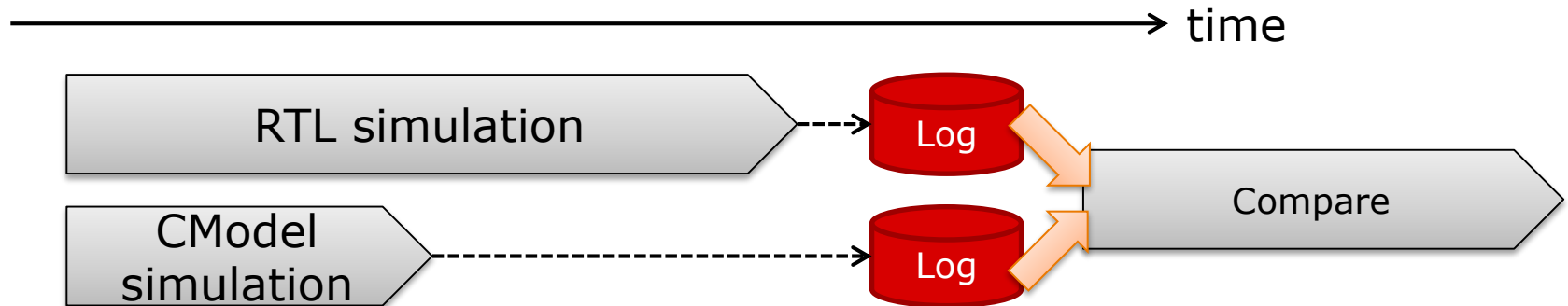
Rev. 0.00

Introduction

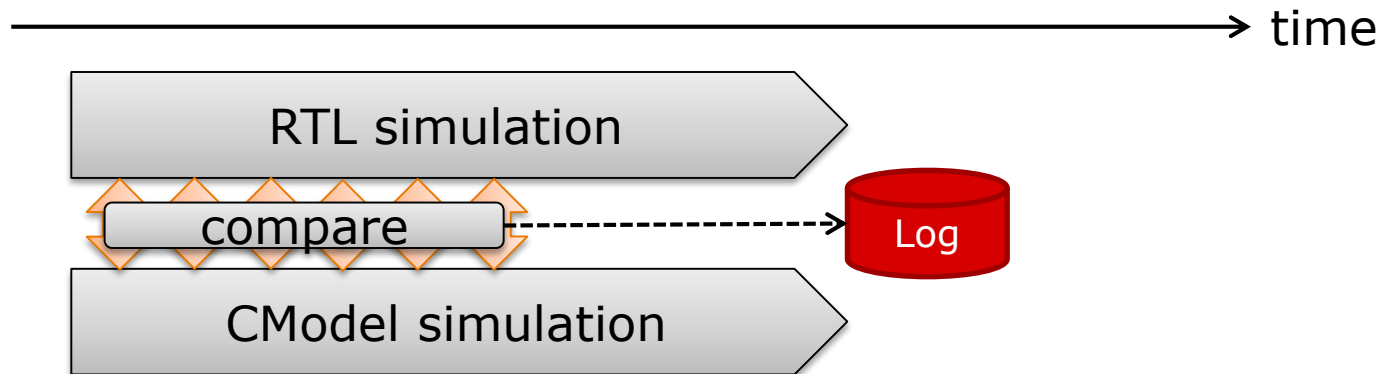
- Two methods of G4H verification using instruction set simulator(ISS)
 - Post simulated verification (CompTrace)
 - Runtime Verification (CompRunner)
- This materials explains overview of CompRunner, runtime verification environment and how to connect RTL to ISS.

CompTrace v.s. CompRunner

■ **CompTrace** (Post verification)



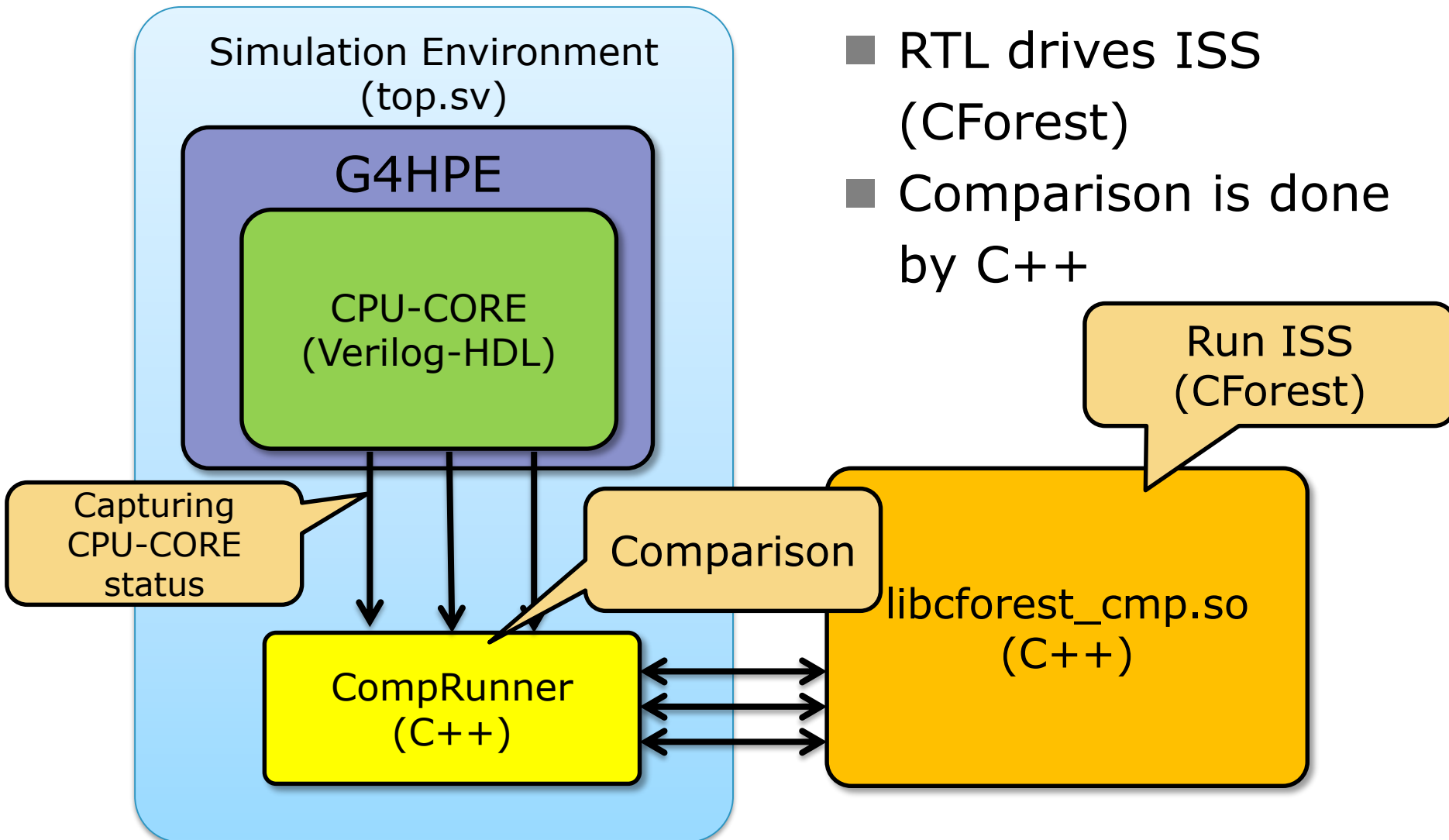
■ **CompRunner** (Run-time verification)



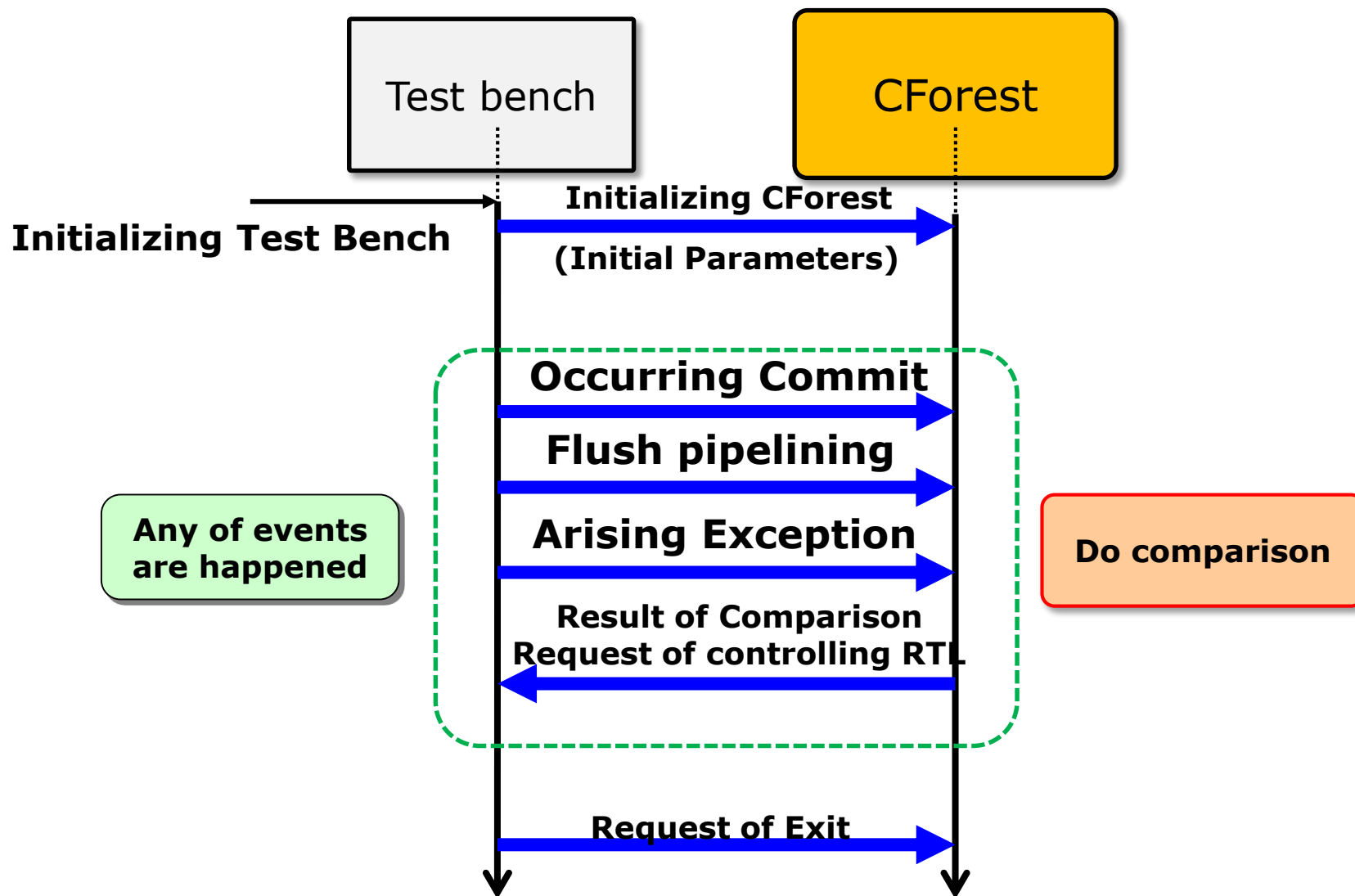
- CompRunner needs not explicit "Comparison" time.
- Comparison is could be done during simulation

Actual Implementation

- RTL drives ISS (CForest)
- Comparison is done by C++



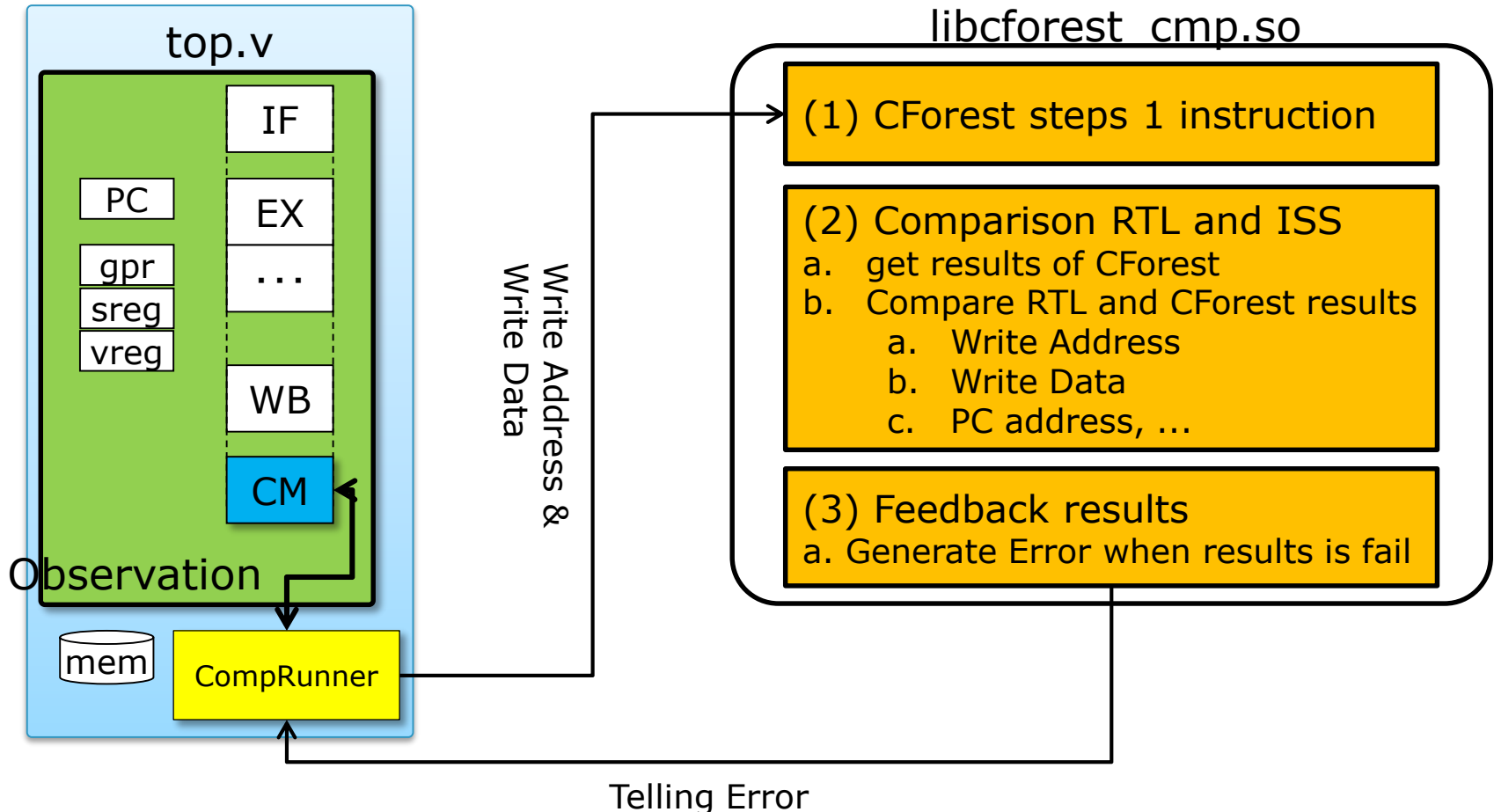
Test flow for ISS-RTL



Comparison flow

■ Driven by Register write

- RTL tells CForest when Commit is occurred
- CForest steps 1 instructions → Compare results



Sample of CompRunner log

```
...
[0000024e] 0000001f ; movw 1193267, r1      GR[01] <=00123533
[00000250] 35330621 ; movw 4900, r2          GR[01] <=00123533
[00000256] 13240622 ; movw 4916, r3            GR[02] <=00001324
[0000025c] 13340623 ; movhi -20971520, r0, r1  GR[03] <=00001334
[00000262] fec00e40 ; divu r1, r2, r4          GR[01] <=fec00000
X[00000266] 22c217e1 ; add r1, r3
                VALUE MISMATCH RTL:GR[03]<=00001234, ISS:GR[03]<=00001233
[00000266] 22c217e1 ; st. h r3, 8[r1]
[0000026a] 000019c1 ; ld. h 8[r1], r3          GR[03] <=fec01334
[0000026c] 00081f61 ; st. b r3, 16[r1]
[00000270] 00081f21 ; ld. b 16[r1], r3          GR[03] <=00001334
[00000274] 00101f41 ; mul r1, r2, r4          GR[04] <=00001324
[00000278] 00101f01 ; div r1, r2, r4          GR[03] <=00000034
[0000027c] 222017e1 ; ld. w 16[r1], r3          GR[02] <=00000000
[0000027c] 222017e1 ; movr r5, r4          GR[04] <=00000000
...
```

Case of
comparison
is failed

Advantage of Runtime Verification

	ポストシミュレート検証	ランタイム検証
速度	ISS/RTL実行&ログ取得 → ログ突合せ 低速	ISS/RTL実行 → 1命令毎に結果突合せ 高速
ディスク使用量	ISS/RTL双方でログを 格納する領域が必要 使用量大	ログが存在しなくても突合せ可能 → ディスク使用量節約 使用量小

Variations in SystemVerilog Environments

	DPI	VPI
Speed of Simulations	Faster	Slower
Calling strategies	Call to SV task/functions	Only called from SV
Google tells	43,100 pages	29,100 pages
Support	Synopsys VCS Cadence IUS Verilator	Synopsys VCS Cadence IUS Veritak



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