Yield Learning and the Sources of Profitability in Semiconductor Manufacturing and Process Development

Charles Weber

***Abstract*—A numerical model that identifies the high-leverage variables associated with profitability in semiconductor manufacturing is presented. Varying the parameters of the model demonstrates that a rapid yield-learning rate determines profitability more than any other factor does. Factors such as ramping-up early, adding fab capacity, depressing the terminal fault density, and shrinking die size all yield diminishing returns. The model also suggests that developing a rapid problem-solving capability in the early stages of process development enables successful yield learning.**

***Index Terms*—Profitability, semiconductor manufacturing, yield learning.**

I. Introduction

THE RELENTLESS drive to increase feature density has made the semiconductor industry extremely capital intensive [1]. Price tags in excess of $1 billion for wafer fabrication facilities (fabs) are no longer considered extraordinary, and they are likely to rise with the arrival of 300-mm wafers. Amortizing fixed costs must thus be considered a key objective of semiconductor manufacturers and their suppliers. In this context, yields near 100% are viewed as highly desirable, and yields significantly below 100% are considered a problem that warrants immediate attention.

In order to achieve yields near 100%, a semiconductor manufacturer needs to master a procedure called yield learning, which essentially consists of eliminating one source of faults after another until an overwhelming portion of manufactured units function according to specification. The engineers, technicians, and managers who are involved in the yield-learning process would like to proceed with fault reduction in a manner that maximizes revenues and minimizes costs. However, in practice, they frequently experience difficulties in implementing the optimal practices for achieving high yields, at least in part because, to date, the relationship between yield and profitability is not completely understood.

In this paper, I define the key stylized facts that characterize the semiconductor industry, and based on those facts construct a model that shows the inner mechanism that drives profitability. The heart of the model is the crucial yield-learning process, whose management is vital to a semiconductor manufacturer's survival. In Section II, I describe the empirical background of this model. In Section III, I develop a production model for a complementary metal–oxide–semiconductor (CMOS) process of the 130-nm generation, the state of the art in the semiconductor industry 2003. The physical assumptions of the production model are derived from the 2001 edition of the Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) [2]. In Section IV, I develop a financial model that describes the expected scenario for financing integrated circuit (IC) ventures in 130-nm technology. In Section V, I vary individual parameters of this model, *ceteris paribus* (all other things remaining equal), to illustrate the mechanisms that drive profitability in the semiconductor industry. In Section VI, I draw a series of conclusions for the semiconductor industry, which, I hope, will help semiconductor-manufacturing firms manage future IC ventures more effectively. I also propose a set of best practices in the semiconductor industry that are suggested by the model, which many semiconductor firms are already implementing to maximize profitability.

II. Empirical Background

The model presented in this paper is grounded in empirical evidence, which has been derived using the method of extended case study research [3], [4]. The inner mechanisms of learning in semiconductor manufacturing and process development are documented in 69 cases of solved yield, process and equipment problems from all functional areas of integrated circuit fabrication, which have been provided by 37 industry experts in one-on-one interviews. The respondents in these interviews have observed semiconductor processes at all levels of maturity in 35 distinct manufacturing and process development environments. The cases span the last quarter of the 20th century, and they involve at least 35 semiconductor manufacturing firms and 23 supplier firms.

The 69 case interviews in this study are supplemented by an additional series of interviews that solicit the expertise of 65 specialists in a variety of disciplines that pertain to semiconductor manufacturing. Experts have been recruited by recommendations from within their respective peer groups. Data have transcribed, coded, analyzed, and converted into a numerical model of the semiconductor lifecycle from which general conclusions about learning in semiconductor manufacturing and process development can hopefully be drawn. The model's output has been tested for consistency with broadly based cross-sectional studies

Manuscript received November 3, 2002; revised February 23, 2004.

The author is with the Department of Engineering and Technology Management, Portland State University, Portland, OR 97207-0751 USA (e-mail: charles.weber@etm.pdx.edu).

Digital Object Identifier 10.1109/TSM.2004.835724

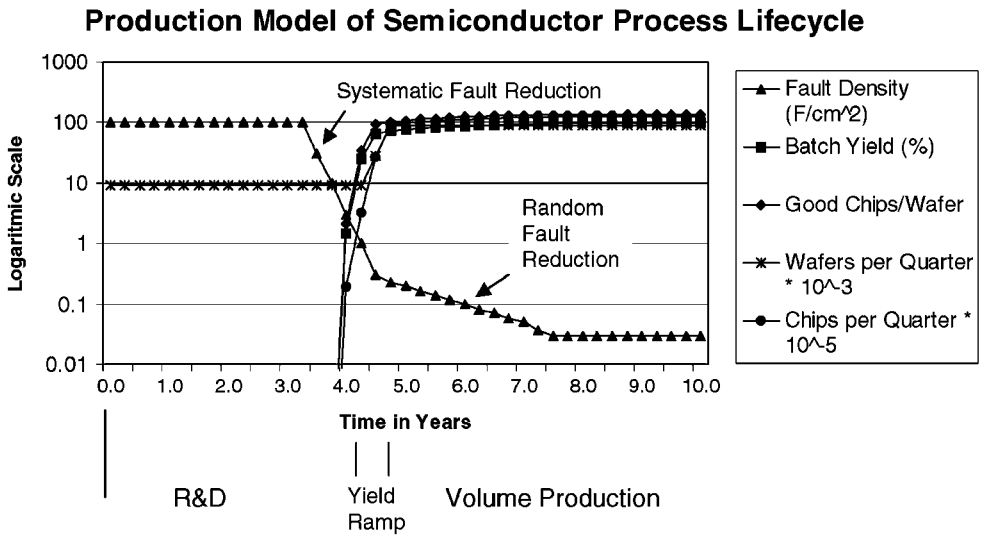

Fig. 1. Fault density, yield, and output as a function of the time since the inception of a semiconductor technology node.

on competitiveness in semiconductor manufacturing [5]–[7] and 25 years of longitudinal historical performance data of individual companies (e.g., [8] and [9]).

III. Production Model

Fig. 1 illustrates the physical assumptions of the production model. Data are displayed on a quarterly basis. The horizontal axis represents the time since the inception of a semiconductor technology node, a proxy for the investment in learning that is consistent with activities in which solving problems of a complex nature is required [10], [11]. The production model uses the Poisson yield model,[1] in which the die-sort yield $(\mathrm{Y_P})$ of a wafer is an inverse exponential function of the product of the density of electrical faults (F) on that wafer and the critical area (A) of an integrated circuit that is susceptible to these faults

$$\mathrm{Y_P} = \mathrm{e}^{-\mathrm{AF}}. \tag{1}$$

The production model also assumes that the process is run on wafers with a diameter of 200 mm, and critical areas of integrated circuits that are realized by this process equals 1.4 cm^2. Approximately 140 such integrated circuits will fit onto a 200-mm wafer.

Early research activities, such as modeling and device performance testing, dominate the first three years of the process life cycle [12]. During this time period electrical fault density on a silicon wafer exceeds 100 faults/cm^2 or is not even measured. Consequently, yields and output are negligible. Up to 3000 wafers exit the R&D facility every month. A very large-scale integrated (VLSI) circuit is introduced into process development late in the third year. Engineers begin to solve systematic process problems, which cause the fault density to drop by an order of magnitude every six months. Due to the exponential relationship between die-sort-yield and fault density [8], the die-sort-yield skyrockets once the fault density drops below 0.3 faults/cm^2. The fab ramps up to 30 000 wafers per month within six months of the yield rise, an aggressive assumption, which according to interviews with industry experts is consistent with the performance of the "best-of-breed" semiconductor manufacturers. Fab output as measured by total number of chips produced per quarter jumps accordingly. The learning rate flattens off in the fifth year as random faults begin to dominate. Ultimately, the fault density settles at its terminal value of 0.03 faults/cm^2.

[1]The Poisson yield model assumes a random distribution of electrical faults with negligible clustering. Introducing yield models that take clustering into account (e.g., [13] and [14]) does not affect the production model or the financial models in any significant way.

IV. Financial Model

The financial assumptions of the model are relatively straightforward. The semiconductor manufacturer incurs operating costs of $50 million per three-month period during the early research and process R&D stages of the life cycle. These costs come from sustaining a design team, an R&D team, and the capital investment in plant equipment during the R&D effort. All equipment depreciates over five years. As the manufacturer ramps up to volume production in the fourth year, the operating costs rise to $150 million per three-month period, primarily due to the amortization of plant equipment at the level required for volume production. Once the equipment has depreciated, operating costs drop back to $50 million per three-month period.

A study of semiconductor economics [15] has shown that the demand for semiconductors creates a "bullwhip effect" [16]–[19] in the semiconductor industry in which the suppliers of technology are exposed to a more volatile economic environment than the users of technology are. Similarly, the demand for microprocessors is relatively independent of cyclical factors when compared to the demand for DRAMs and semiconductor process equipment. The demand function for the semiconductor profitability model, which is depicted in Fig. 3, has been customized for microprocessors for this reason. The chip price is modeled as an exponentially decaying function, which starts out above $10 000 per chip in the first year, when essentially none of the chips are available, and decays by an order of

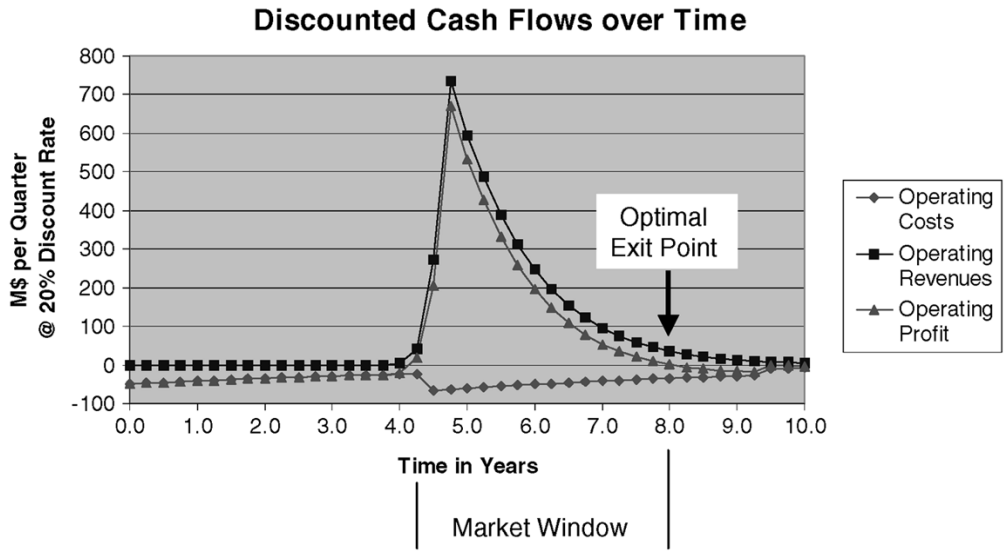

Fig. 2. Discounted cash flows of a semiconductor venture.

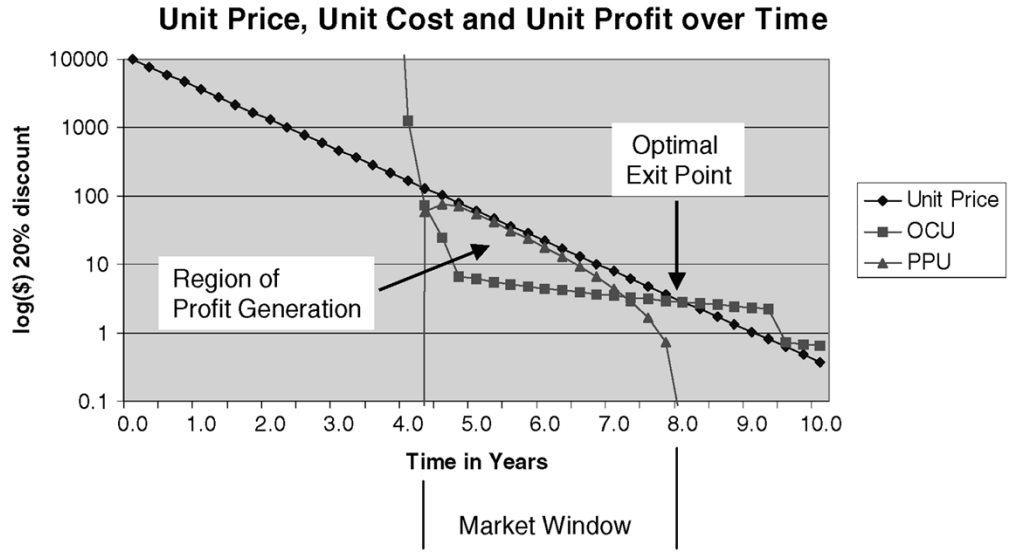

Fig. 3. Unit price and unit cost and unit profit of microprocessors as a function of time.

magnitude every 2.25 years.[2] At the end of the ten-year period covered by the model, the market price of a chip is below $1. These pricing assumptions are consistent with the demand function for microprocessor development for the last three technology nodes. However, noise induced by events such as unexpected changes in the demand for microprocessors and the effect of competitors entering the market have been excluded from the model. The model assumes a 20% discount rate, which is consistent with the opportunity cost of capital for a manufacturer of microprocessors that is not the market leader.

Fig. 2 shows the discounted cash flows that result when the model is run with the hitherto mentioned assumptions from the production model and the financial model as inputs. The semiconductor manufacturer that operates under these conditions essentially invests for about four years without any revenue because yields are negligible. The profit picture goes even more negative during the ramp to volume production but after the ramp profitability surges due to a yield-driven revenue infusion. More than 70% of pretax profits are made within one year of the ramp to volume production, causing many semiconductor manufacturers to choose accelerated depreciation schedules to distribute profits more evenly over time. However, the model shows that this practice has little effect on the total profit gained from a semiconductor venture. Revenues decay exponentially until net cash flows go negative in the eighth year. Therefore, producing microprocessors makes no economic sense beyond the eighth year even though yields are high and plant equipment is amortized [21], [22].

Fig. 3 implies that the exponential relationship between yield and fault density places the semiconductor industry under a regime of radical experience curves [23], [24]. Comparing the operating cost per unit (OCU) to the unit price of a micropro-

[2]The respondents, on average, expected a deterioration rate of an order of magnitude every three years, which has been commensurate with Moore's Law [20]. The value 2.25 years per order of magnitude approximately represents this estimate discounted at 20% per annum.

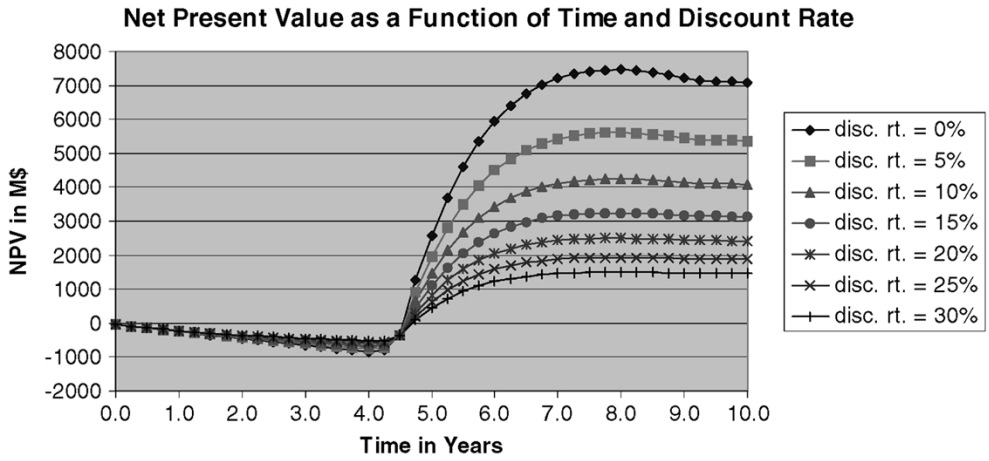

Fig. 4. Effect of the discount rate on profitability. Discount rate ranges from 0% to 30%.

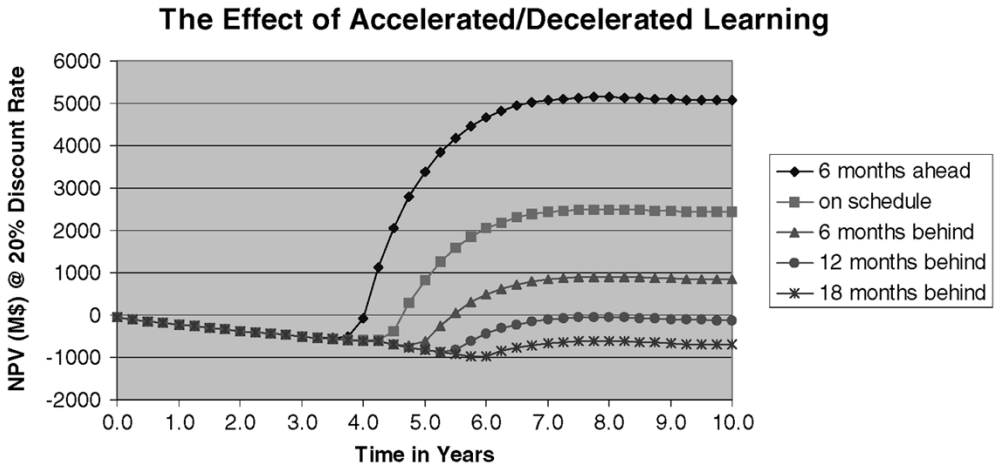

Fig. 5. Effect of accelerated or decelerated yield learning.

cessor confirms the relatively short period of time in which semiconductor ventures can remain profitable. The operating cost per unit is defined as the ratio of operating costs incurred in one particular quarter to the number of products produced that quarter. The profit per unit (PPU) is the difference between the unit price and the operating cost per unit. Fig. 3 shows that the OCU remains at very high values until die-sort-yield becomes significant. By the time of the ramp-to-volume production the OCU drops below the unit price of the chip, and the venture becomes profitable. The OCU remains below the unit price for a bit longer than three years, after which the semiconductor venture ceases to be profitable and should be shut down.

V. Varying Parameters

Having established a model that describes the experience curves of the semiconductor process life cycle, I can now proceed with identifying the high-leverage variables that govern profitability in the semiconductor industry. I do so by varying the individual parameters of the model, *ceteris paribus*, and graphically displaying the effect on profitability. I use net present value (NPV), which can be interpreted as the expected discounted cumulative profit of a venture, as a metric for profitability.

Fig. 4 shows how the profits of a semiconductor venture accumulate over the life cycle of a technology generation. For the first four years of generations life cycle the semiconductor manufacturer invests in research, process development, and product design, as well as making a concerted effort at integrating technologies developed by outsiders [7]. If all these endeavors are successful, then fault density drops, and yield surges in a manner detailed in Fig. 4. The semiconductor manufacturer ramps to maximum capacity, while yield is improving dramatically, a phenomenon that is termed the "yield ramp." The semiconductor venture becomes highly profitable during the yield ramp, because the manufacturer is still operating in an environment of capacity constraint that allows him/her to charge a premium price for the manufactured goods. However, the price drops as the capacity constraint eases, and profitability deteriorates. The manufacturer should exit the venture at the point of highest level of cumulative profit, which is represented by the highest point of an NPV trajectory in Fig. 4. However, the amortization of capital equipment, which tends to continue beyond the optimal exit point, may deceive the semiconductor manufacturer into persisting with the production of microprocessors at loss rates that may be too small to be noticed.

TABLE I
FACTORS THAT EXHIBIT DIMINISHING RETURNS

The effect of varying ***terminal fault densities***.					
FDt in (f/cm^2)	1	0.3	0.1	0.03	0.01
Net Profit (M$)	-1400	1800	2400	2500	2500
The effect of adding 30000 wafer outs per month of ***fab capacity*** every six months.					
# of Fabs	1	2	3	4	5
Net Profit (M$)	2400	4300	5300	5700	5900
The effect of ***shrinking*** die area and feature sizes by 15% every year.					
Critical Area (cm^2)	1.41	1.18	1	0.84	0.71
# of Dice per Wafer	142	169	200	238	282
Net Profit (M$)	2400	2900	3100	3200	3200

A. Discount Rate

One of the most obvious factors that affect profitability is the discount rate of the venture, which is determined by general economic factors such as inflation, interest rates, the risk of the venture, and alternate opportunities for spending capital. Fig. 4 illustrates that the discount rate for semiconductor ventures has an adverse effect on their profitability but that it does not decide whether or not a semiconductor venture will be profitable. If one assumes the conditions described in Sections III and IV, then semiconductor ventures are profitable at some level, regardless of the discount rate.

B. Yield-Learning Rate

The yield-learning rate tends to be the most significant contributor to profitability in semiconductor manufacturing. Fig. 5 shows that moving the yield ramp up by six months more than doubles the cumulative net profit of the semiconductor venture, whereas delaying it by six months eliminates two thirds of the profit. Semiconductor ventures that are a year late tend to lose money. These figures translate into a cost of about $5000 for every minute of process development time. Thus, a problem that is on the critical path of process development can induce a loss rate of $5000/min or more. A slower rate of fault reduction or yield improvement also erodes profitability, only at a slower rate, as does a slower ramp to production. By contrast, an earlier (later) deterioration of the price of microprocessors has the opposite effect of and earlier (later) yield ramp. If the price deteriorates six months ahead of (behind) schedule, then the profitability drops (rises) by the same amount that a delay (acceleration) of the ramp would cause.

The schedule in Fig. 5 is determined by the substitutability of the product and the time of entry of the competitors. "On time" from the point of the view of this model means producing at high volumes on the date when Moore's Law [20] predicts high volumes of the product should be available. The model only covers the range from beating Moore's law by six months to lagging it by 18 months. Beating the schedule by more than six months is considered extremely difficult because the suppliers of process technology are in all likelihood not going to be able to deliver their technology at that time. Conversely, a manufacturer that enters the market more than 18 months behind the date suggested by Moore's Law is not likely to make a profit.

C. Factors That Exhibit Diminishing Returns

Since the level of profitability of a semiconductor venture primarily depends upon when the ramp to volume production occurs, it would be tempting for a manager of a process development effort to simply ramp up before the yield surges. However, the model shows that ramping up at higher fault density reaps no additional benefits, because the majority of the output goes to waste. According to [25] the model is even optimistic in regards to this conclusion because it does not take into account the fact that learning at high yields is faster than learning at low yields.

Table I shows the effect of varying three additional parameters in the model *ceteris paribus*, all of which yield diminishing returns. Varying the terminal fault density of a semiconductor process indicates that achieving profitability is difficult at fault densities above 0.7 faults/cm^2, even for microprocessors, which have a relatively high value. Profitability increases dramatically between 0.5 and 0.2 faults/cm^2 but reaches diminishing returns below 0.1 faults/cm^2. Adding 30 000 wafers per month of fab capacity also reaches diminishing returns after the third iteration. Simultaneous technology transfer from one fab to many fabs right after ramping up in the first fab would be a much more profitable approach because the chipmaker operates in an environment of capacity constraint in which he/she can command much higher prices for chips.

Shrinking designs and feature sizes also reach diminishing returns. The model assumes that the initial design, which exhibits a critical area of 1.41 cm^2, is released at $t = 4.0$, just before the yield ramp. Additional design revisions are released in annual intervals thereafter. The critical area of the design shrinks by 15% from revision to revision and the number of printed dice per wafer increases accordingly. The first shrink, which occurs at $t = 5.0$ years when unit price is very high, adds about $0.5 billion to the bottom line. However, the third and the fourth shrink, which respectively occur at $t = 7.0$ and $t = 8.0$ years when the unit price is an order of magnitude lower, barely impact profitability. It is assumed that these later design shrinks can be realized without purchasing a new generation of lithography tools. If this assumption is false, then the shrinks at $t = 7.0$ and

$t = 8.0$ years may actually decrease net present value of the venture, suggesting that shrinking designs by more than 30% of their original size may actually impact profitability in a negative way.

The reasons for diminishing returns depicted in Table I are essentially the same in all cases. It takes calendar time to advance quality, add factory capacity, or generate new design revisions. In an environment in which unit price decays exponentially over time, the benefits of producing more sellable chips per unit time will ultimately be neutralized by the smaller amount of profit that each chip generates.

VI. Conclusion

Yield learning can be defined as a process for developing goods with low unit cost under four conditions: 1) long development times; 2) high fixed costs associated with development and production; 3) an exponentially decaying failure rate of the goods to be sold; and 4) a deteriorating unit price. The stylized model of yield, profitability, and cost that is described in this paper illustrates that the yield-learning phenomenon is directly related to profitability in the semiconductor industry. The model generates the following conclusions, which are consistent with findings from the engineering and management literature, and it suggests a series of practices, most of which are generally known and believed by senior managers and engineers in the industry.

1) The exponential relationship between yield and fault density imposes a capacity constraint on the supply of chips until fault density drops to a level of 0.3 faults per square centimeter.
2) Assuming the demand for the chips to be produced is high, the semiconductor venture becomes profitable as soon as yield surges. At that point in time it is in the manufacturer's interest to produce as many units as possible. The manufacturer can only do this if the product, the process, and the factory are ready for a ramp at that point in time. Achieving this feat requires extensive coordination between product development, process development, and technology supply chain development efforts, which has also been observed outside the semiconductor industry [26], [27].
3) Due to deteriorating chip prices, profitability depends upon short development times and the time to reach full capacity utilization [22]. The sooner the yield ramp occurs and the steeper it is, the more profitable the venture is. Most of the semiconductor venture's profit is made in a brief period right after the yield ramp [21].
4) Profitability for the initial product in a technology node essentially disappears within less than four years of the yield ramp, after capacity constraint eases. Therefore, making cheap chips using depreciated equipment makes no real money. The useful lifetime of a fabrication facility can, however, be extended by introducing newer more lucrative designs that run on the same process.
5) The cost of learning appears enormous before the yield ramp—it requires huge investments of time and money (equipment, etc.) but seems trivial thereafter. Yet, in practice, semiconductor manufacturing organizations learn on a continuous basis. A large portion of this learning occurs before the release of any product, a phenomenon that is not unique to the semiconductor industry [26], [28].

Qualitative information, which has been revealed in the interviews with managers, engineers, and technicians involved in semiconductor manufacturing or its technology and material supply chain provides insight into the mechanisms by which these manufacturers achieve profitability through learning. Many of these insights are consistent with problem-solving practices that have been documented in the management and engineering literature.

1) Competitive advantage is derived from identifying the problems whose resolution will have the most impact [29] and from solving these problems as rapidly as possible. Rapid diagnosis of the problems is critical [30], [31].
2) Rapid diagnosis requires years of coordinated and integrated preparation. At all stages of process development, semiconductor manufacturers design for diagnosability (DfD), in order to accelerate the learning rate. DfD practices include designing microelectronic test structures into products and inspection/diagnostic steps into the process. Using knowledge that has been accumulated from their previous experience bases, problem solvers in the semiconductor solution space partition the space of a problem—the area where the solution of a problem must lie—by running a manufacturing baseline in parallel with a process R&D effort. The president of a company that supplies diagnostic technology to semiconductor manufacturers has used the following metaphor to explain this line of reasoning.

"Essentially what we are doing is setting up mousetraps. We set them up where we think the mice are most likely to be. . . . A mouse may be caught by a combination of traps."

3) Design for diagnosability in the semiconductor industry tends to involve a total systems approach [9], [32]. The amount of information extracted is traded off with the time it required for information extracted, which is driven by the length of the experimentation cycle. Experimentation cycles of different practices vary from real time in the case of *in situ* sensors to months in the case of reliability physics. The amount of information extracted per experimentation cycle and per unit time can serve as a metric for learning rate [33].
4) Within the problem solving process, rapid localization of a problem to a particular technology provides the most leverage [30], [31]. A manager who is an expert in ion implantation cites an example.

"I can recall an instance where the [die-sort] yield crashed to near-zero levels in four production lines. . . . The loss rates were enormous. Our vice president later told us this problem cost us about $64 million. . . . Once we had localized the problem to a particular ion implanter that was feeding these four lines, we were able to shut down the implanter and search for the cause of the problem within the implanter. . . . We lost production capacity because the implanter had been taken offline, but the yield came back because the problem had been isolated. . . . Running on fewer implanters and achieving high [die-sort] yields

was much better than achieving low yields at production capacity."

5) Learning modes shift dramatically during the life cycle of a semiconductor process technology node. Simulation of circuitry and VLSI process cross sections dominates the early stages of process development, when it is believed to remove more errors per effort than any other approach. This practice is replaced by physical experimentation once the perceived performance of simulation saturates [34]. Once fault density drops to levels where it can be measured with statistical significance, more faults can be reduced per unit time by realizing dummy VLSI circuits (see for example [35]) with candidate processes, a mode of experimentation that is particularly useful for the elimination of complex systematic faults. The actual products are generally introduced shortly before the yield ramp and tend to serve as vehicles for reducing random faults.

The model in this paper can be summarized in a single sentence: In order to produce profitable products in the semiconductor industry, you must produce the right product using the right process in the right fabrication plant at the right time. This is a complex coordination problem requiring a high level of management skills in human resources, technology, and finance. The requisite management skills in this high-wire feat are sufficiently rare to comprise a significant barrier to entry. The key to success appears to be predicting from existing knowledge problems that are likely to occur and designing mechanisms for their rapid solution before they occur.

ACKNOWLEDGMENT

The author would like to thank Prof. S. Maital (Technion University), Prof. R. Bohn (University of California, San Diego), Prof. N. Repenning, Prof. E. B. Roberts, and Prof. M. Cusumano (all three of MIT's Sloan School of Management) for sharing their expertise on experience curves.

REFERENCES

[1] P. Silverman, "Capital productivity: Major challenge for the semiconductor industry," *Solid State Technol.*, vol. 37, no. 3, p. 104, Mar. 1994.
[2] "The National Technology Roadmap for Semiconductors," : Semiconductor Industry Association, 1997, pp. 99–113.
[3] R. K. Yin, "The case study crisis: Some answers," *Administrative Sci. Quarterly*, vol. 26, pp. 58–65, Mar. 1981.
[4] K. M. Eisenhardt, "Building theories from case study research," *Acad. Manage. Rev.*, vol. 16, pp. 620–627, 1989.
[5] R. C. Leachman, "Competitive manufacturing survey: Third report on the results of the main phase," Univ. California, Berkeley, Rep. CSM-31, 1996.
[6] R. C. Leachman and D. Hodges, "Benchmarking semiconductor manufacturing," *IEEE Trans. Semiconduct. Manufact.*, vol. 9, pp. 158–169, May 1996.
[7] M. Iansiti and J. West, "Technology integration," *Harvard Bus. Rev.*, pp. 69–79, May–June 1997.
[8] C. Stapper and R. Rosner, "Integrated circuit yield management and yield analysis: Development and implementation," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 95–101, May 1995.
[9] C. Weber, B. Moslehi, and M. Dutta, "An integrated framework for yield management and defect/fault reduction," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 110–120, May 1995.
[10] W. Fellner, "Specific interpretations of leaning by doing," *J. Econom. Theory*, no. 1, pp. 119–140, Aug. 1969.
[11] L. Dudley, "Learning and productivity change in metal products," *Amer. Econom. Rev.*, vol. 62, pp. 662–669, Sept. 1972.
[12] Y. Nishi, "VLSI research and development in the U.S. and Japan," in *Proc. Mater. Res. Symp.*, 1990, pp. 3–11. VLSI V.
[13] S. Cunningham, "The use and evaluation of yield models in integrated circuit manufacturing," *IEEE Trans. Semiconduct. Manufact.*, vol. 3, pp. 60–71, May 1990.
[14] C. Stapper, "Modeling of integrated circuit defect sensitivities," *IBM J. Res. Develop.*, vol. 27, pp. 549–557, Nov. 1983.
[15] K. VanBree, "Silicon cycles," M.S. thesis, MIT, Cambridge, MA, 1995.
[16] J. W. Forrester, *Industrial Dynamics*. Cambridge, MA: Productivity Press, 1961.
[17] J. Sterman, "Modeling managerial behavior: Misperceptions of feedback in a dynamic decision making environment," *Manage. Sci. 35*, no. e, pp. 321–339, 1989.
[18] P. Senge, *The Fifth Discipline*. New York: Doubleday, 1990, ch. 3.
[19] H. Lee, V. Padmanabhan, and S. Whang, "Information distortion in a supply chain: The bullwhip effect," *Manage. Sci.*, vol. 43, no. 4, pp. 546–558, Apr. 1997.
[20] G. Moore, "Progress in digital integrated circuits," *IEDM Tech. Dig.*, p. 11, 1975.
[21] R. E. Bohn and C. Terwiesch, "The economics of yield-driven processes," *J. Operations Manage.*, vol. 18, no. 1, pp. 41–59, 1999.
[22] C. Terwiesch and R. E. Bohn, "Learning and process improvement during production ramp-up," *Int. J. Production Econom.*, vol. 70, no. 1, pp. 1–19, 2001.
[23] *Executive Economics*, pp. 139–168, 1994.
[24] C. Weber, "Accelerating three dimensional experience curves in integrated circuit process development," M.S. thesis, May 1996. MIT.
[25] C. Fine, "Quality improvement and learning in productive systems," *Manage. Sci.*, vol. 32, no. 10, pp. 1301–1315, 1986.
[26] G. P. Pisano, "Learning before doing in the development of new process technology," *Res. Policy*, vol. 25, pp. 1097–1119, 1996.
[27] C. H. Fine, *Clock Speed: Winning Industry Control in the Age of Temporary Advantage*. Reading, MA: Perseus, 1998.
[28] S. H. Thomke and T. Fujimoto, "The effect of front-loading problem solving on product development performance," *J. Product Innovation Manage.*, vol. 17, no. 2, pp. 128–142, Mar. 2000.
[29] *Quality Control Handbook*, 3rd ed., J. M. Juran, Ed., McGraw-Hill, New York, 1974, pp. 2-16–2-19.
[30] C. Weber and E. von Hippel, "Maximizing profitability through easy information transfer," in *Proc. IEEE/SEMI/ASMC*, Boston, MA, Sept. 13, 2000, pp. 250–255.
[31] ——, "Knowledge transfer and the limits to profitability: An empirical study of problem-solving practices in the semiconductor industry," in *Proc. PICMET-2001*, Portland, OR, July 30, 2001, pp. 349–354.
[32] C. Weber, D. Jensen, and E. D. Hirleman, "What drives defect detection technology?," *Micro*, pp. 51–72, June 1998.
[33] C. Weber, V. Sankaran, G. Scher, and K. Tobin, "Quantifying the value of ownership of yield analysis technologies," in *Proc. IEEE/SEMI/ASMC*, Boston, MA, Sept. 8, 1999, pp. 64–70.
[34] S. H. Thomke, "Managing experimentation in the design of new products," *Manage. Sci.*, vol. 44, no. 6, pp. 743–762, June 1998.
[35] E. J. Sprogis and R. E. Newhart, "Defect diagnostic matrix—A defect-learning vehicle for submicron technologies," in *Proc. IEEE/ICMTS*, 1988, pp. 103–106.

Charles Weber received the A.A. degree in physical science from the American College of Switzerland, the B.S. degree in engineering physics from the University of Colorado, Boulder, the M.S. degree in electrical engineering from the University of California, Davis, the S.M. degree in management of technology from the Massachusetts Institute of Technology (MIT), Cambridge, and the Ph.D. degree in management from the Sloan School of Management, MIT.

He joined Hewlett-Packard (HP) Company as a Process Engineer in an IC manufacturing facility. He subsequently transferred to the IC process development center, working in electron beam lithography, parametric testing, microelectronic test structures, clean room layout, and yield management. From 1996 to 1998, he managed the defect detection project at SEMATECH, as an HP assignee. In December 2002, he joined the faculty of Portland State University, Portland, OR, as an Assistant Professor of engineering and technology management.