Organizational Learning and Capital Productivity in Semiconductor Manufacturing

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***Abstract*—This paper presents an empirical study, which leads to a theoretical framework that links organizational learning and capital productivity. The approach described in this paper helps fab managers make fundamental strategic decisions concerning capital investment and point of entry by engaging in scenario planning. Three strategic options for semiconductor manufacturing are analyzed in detail—leading-edge manufacturer, fast follower, and slow follower. The study concludes that profitability and capital productivity can be in conflict with each other. Leading-edge manufacturers can make large profits, if they ramp up to volume production in a timely manner, but their return on investment and thus their capital productivity are relatively low. Generally, manufacturers that do not run state-of-the-art processes are less profitable than those that do, but their return on investment and thus their capital productivity is comparatively high. Fast followers, which import part of their manufacturing process and ramp to volume production rapidly but with a delay, neither break even nor recover their investment.**

***Index Terms*—Organizational learning, capital productivity.**

I. Introduction

THE relentless escalation of the cost of human, physical and financial capital, which has characterized the semiconductor industry for over two decades [1], is forcing semiconductor manufacturers to ask themselves a few fundamental questions. What are the circumstances under which we remain profitable and recover our investment if we 1) continue on the Moore's Law trajectory; 2) upgrade to the next wafer size; 3) do both; or 4) do neither? What is the optimal point of entry for our next technology node? Should we be a technology leader, a fast follower or a slow follower? When and under which circumstances should we invest in a new wafer fabrication facility (fab)? The stakes associated with these questions are in the billions of U.S.$, and answering these questions incorrectly could put a semiconductor manufacturer out of business. The phenomena that underlie the issues that these questions raise are therefore considered worthy subjects for academic study (see, for example, [2]).

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Semiconductor manufacturers and SEMATECH have generated models that have attempted to address the fundamental strategic issues that semiconductor manufacturers face (see, for example, [2]). These models have successfully characterized the general economic environment in which semiconductor manufacturers find themselves. However, they do not explore the relationship between the two most important drivers of profitability in semiconductor manufacturing — organizational learning (see, for example, [3]–[6]) and capital productivity [1]. Factors related to organizational learning and capital productivity can vary greatly from manufacturer to manufacturer. Prior economic models have therefore not been particularly useful to semiconductor manufacturers when they make resource allocation decisions that pertain to their specific situations.

This paper addresses the abovementioned questions and issues in a manner that contributes directly to the bottom line of semiconductor manufacturers. It describes an empirical study that assesses the economic value of various organizational learning practices that are common in semiconductor manufacturing and links them to capital productivity. In particular, the study explores how deliberate organizational learning activities impact the profitability and return on investment of semiconductor manufacturing ventures for the three fundamental strategic options that semiconductor manufacturers can pursue — leading-edge manufacturer (LEM), fast follower (FF) and slow follower (SF). Preliminary results of the study described in this paper have been presented in [7]–[10].

This paper's primary contribution is an empirically grounded theoretical framework of the cost and value of organizational learning (CoVaL), which can be applied to semiconductor manufacturing. The framework helps practicing managers make fundamental strategic decisions through scenario planning. It integrates well-known, subsystem-level organizational learning metrics (number of dice per wafer, fault density, line yield, fab throughput), environmental economic variables (average sales prices of the goods to be sold, quantity demanded) and internal metrics that estimate the cost of learning. These inputs can be customized to reflect the specific conditions of a particular semiconductor venture. The framework can also be used to estimate profit and capital productivity of the venture over its expected lifetime.

The remainder of this paper is organized as follows. Section II details the research methods that have been deployed in the study described in this paper. Section III presents the theoretical framework for organizational learning and capital productivity that has emerged from the empirical findings of

the study. In Section IV, the framework from Section III is customized to generate six scenarios that are of particular interest to modern semiconductor manufacturers. Section V estimates profitability and capital productivity for each scenario. Section VI summarizes the contributions of this paper and draws conclusions. It also points out the limitations of the model that is described in this paper and suggests opportunities for further research.

II. Research Methods

Data for this study have been obtained by deploying the case study research method [11], [12], an inductive, qualitative approach from the social sciences that has been implemented successfully in previous studies of the semiconductor industry (see, for example, [7]–[10], [13]–[20]). This method was chosen in part because semiconductor manufacturers are highly reluctant to make quantitative technical data and financial data available to outsiders. Case study research also permits inferences from multiple sources [12], *e.g.*, interviews, surveys and participant observation, as well as previously published quantitative economic and technical data.

The case study research method is particularly useful for generating analytical models of complex economic and social processes for which extant theory is inadequate [12]. However, models generated from case study research are derived from data samples that are purposely biased to reveal the mechanisms that govern the processes under study. Consequently, conclusions derived from these models do not carry statistical significance [11], [12].

Primary data for this study were collected in personal, one-on-one interviews with 123 managers, engineers and technicians employed by 29 chipmakers and supplier firms, which were conducted between 1996 and 2013.

> *"In these interviews, the respondents recounted instances of learning and problem solving in which they were personally involved. They answered specific questions concerning technical and financial variables, and they were asked to explain how the numerical values of these variables evolved over time. In addition, the respondents were asked open-ended questions, the answers to which provided a more detailed explanation of why the variables in each case varied over time as they did."* [9, pp. 43-44]

As recommended in [11] and [12], data from case interviews have been compared to data from secondary sources. These include normalized data on the average sales prices of integrated circuits [2], [21] and projections of technical trends that have been published in various editions of the Semiconductor Industry Association's *International Technology Roadmap for Semiconductor*s [22]. Primary source data was also supplemented by observing the behavior of the employees of a semiconductor production facility over a prolonged period of time [17], [18].

A semiconductor manufacturing venture that represents a particular strategic option constitutes a case. Consistent with [11, pp. 46-63], three cases were constructed from the data, one for each aforementioned strategic option—LEM, FF and SF. Each case contains multiple units of analysis. Each unit of analysis consists of a "story" about one specific technology development project in which deliberate, subsystem-level (departmental) learning efforts have had a measurable impact on fab performance. Every story is told by one respondent.

Analysis of data from within the individual cases has revealed consistent patterns that illustrate how technical and financial variables have evolved over time within each venture (see, for example, [7]–[10], [14]–[20]). Comparing cases (cross-case analysis [23]) provides insight into how the external economic environment of each venture affected the venture's profitability and return on investment. A literature search is conducted in parallel with the analysis of the empirical data so that findings that contradict extant theory can be identified [24]. Novel theory is built in part from resolving the contradictions [20], [23].

Analytical CoVaL models of the lifecycles of six stylized semiconductor ventures have been derived from within-case analysis, cross-case analysis, and analysis of the data from secondary sources. They track key technical and financial variables throughout the lifecycle of a semiconductor manufacturing venture from inception of the venture through mature volume production. The models are expressed in terms of visual formalisms such as Figs. 1–7, as well as in the associated narrative presented in Sections III–V. Empirical evidence is primarily used to validate that the CoVaL models reflect semiconductor manufacturing reality and to determine the numerical value of critical parameters.

> *"Key aspects of the models of the semiconductor manufacturing lifecycles have been validated in interviews with 40 experts in thin films, photolithography, photomask manufacturing, plasma etching, ion implantation, semiconductor operations, integrated circuit process development, tool development, materials development and related technical fields. These experts were recruited by recommendations from within their respective peer groups. In addition, some of the respondents that recited a case have acted as validation experts for cases other than their own. The technical complexity of semiconductor manufacturing has warranted such a large number of expert interviews. For example, an expert in materials engineering would not necessarily be able to validate the relevance of a case that revolved around optics and polymer chemistry. Similarly, aspects of a case in which production management skills were germane to performance improvement required validation by experts in operations management, logistics, or supply chain management, rather than validation by technical experts."* [9, p. 44]

The prolonged duration of the study (>17 years) has given the authors a sense of how semiconductor manufacturing has evolved over time. "In particular, the authors have been able to assess which practices have changed over time and which have not. The authors are also able to identify findings that were valid in the past but no longer are." [20, p. 466]

III. Empirically Grounded Theoretical Framework

Empirical evidence from this study suggests that many aspects of organizational learning (see, for example, [3]–[6]), which have been observed in a multitude of high technology industries, apply to semiconductor manufacturing. For example, "many high tech industries are characterized by shrinking product lifecycles, [as well as] increasingly expensive production equipment and up-front cost. ... These forces pressure organizations to cut not only their development times (time-to-market), but also the time it takes to reach full production volume (time-to-volume), in order to meet their financial goals for the product (time-to-payback)" [25, p. 1]. "Learning in high technology industries is thus characterized by a sense of urgency [26]: it is in the interest of high technology firms to begin the learning process as early as possible and to ramp to production volume as rapidly as possible" [15, p. 1220]. "Process development occurs somewhat in parallel with product development" [27, p. 90], and organizational learning, to a large degree, transpires in parallel at the subsystem level (*e.g.*, within production and process engineering departments [7]–[10], [14], [15], [28]).

A. Production Volume Learning

Empirical evidence gathered for this study suggests that a fab learns from novel experiences as it increases its production volume [4]. The fab encounters new problems as it produces wafers at a greater rate, and it has to develop new approaches to solve them. In the words of an expert in semiconductor diagnostics:

> *"You cannot just crank up a wafer fab like the volume knob on your stereo. It requires some learning. You will add more equipment. You may have to add and manage additional shifts in maintenance and production. Equipment problems that do not occur when you run at low volume are likely to appear. For example, robotic loading equipment is more likely to fail if you run it perpetually without maintenance. ... You may also have to remove a few unnecessary [diagnostic] steps from the process to minimize your WIP [work-in-progress] inventory. You will have to learn how to run the fab without the information that these [diagnostic] steps reveal. ... All of this [learning] takes time."* [15, p. 1228]

In this study, the rate of Production Volume Learning (PnVL) for a particular semiconductor venture 'j' is measured by $W_j(t)$, the rate of 'wafer starts'. $W_j(t)$ is defined as the number of wafers associated with venture 'j' that enter the production line between time t and time $t + \Delta t$, where Δt represents a measurable increment of time. The point in time at which a leading-edge manufacturer commences with process development on the technology node under consideration is defined as $t = 0$.

B. Semiconductor Process Lifecycle

The lifecycles of the semiconductor processes observed in this study bear significant resemblance to those observed in other high tech manufacturing industries that are associated with an urgent environment (see, for example, [27], [29]). "Processes go through three development phases – Process Research (PR), Pilot Development (PD) and Commercial Start-up (CS)" [27, p. 90], prior to commencing with volume production (VP). *Process Research* "involves defining the basic structure of the process. ... The goal of process research is to define the basic process architecture rather than the details" [27, p. 90]. This goal is generally achieved by running a set of small-scale experiments in a laboratory setting to select reaction sequence from a set of theoretically feasible alternatives. "*Pilot Development* involves scaling up the process to some intermediate scale [though modest production volume learning] and selecting reaction parameters (such as timing, temperature, pressure), which optimize the efficiency of the process" [27, p. 90]. Pilot Development is much more empirical in nature than Process Research because it relies on the analysis of the output of pilot production runs, which are subjected to conditions that reflect actual production environment more accurately. *Commercial Startup*, the last phase of VLSI circuit research and development, involves ramping production volume up to commercial scale while continuing to make changes to the semiconductor process. CS generally also tends to include transferring the process from a development organization to a production organization (see, for example, [25], [30]–[32]). "How smoothly this phase goes, depends upon how well problem solving during Process Research and Pilot Development have integrated knowledge about the factory environment" [27, p. 91]. CS is characterized by capacity constraint, implying that all products that a particular semiconductor process realizes will be sold. Ramping up continues until capacity constraint eases. During *volume production*, market forces determine the quantity of VLSI circuits produced per unit time ([8], [19], [20], [29]).

C. Quality Learning

Prior studies of the semiconductor industry [7]–[10] have observed three forms of organizational learning that occur at the subsystem level and pertain to quality. Production Quality Learning (PnQL) improves the quality of production by increasing the survival yield, $S_j(t)$. Process Quality Learning (PcQL) reduces fault density, $F_j(t)$. Design Learning (DL) consists of shrinking the size of integrated circuit parts from design revision to design revision. DL reduces the odds that a particular part contains a fault. It also increases $N_j(t)$, the number of potentially functional parts per wafer. $S_j(t)$, $F_j(t)$ and $N_j(t)$ pertain specifically to wafers associated with venture j, which entered the production line between t and $t + \Delta t$. All measurements are made when these wafers exit (or fail to exit) the production line.

Our study shows that all three quality learning efforts behave in a manner that is consistent with Lotka-Volterra models (see, for example, [3]), in which engineers and managers are treated as predators that prey on all "errors, wastes and other inefficiencies that impair the operations of the [production] process" [3, p. 911]. Under these circumstances, the performance metric M(q) of a continuous improvement effort

can be expressed in terms of the differential equation

$$dM(q)/dq = -c\left(M(q) - M^*\right)^{\varphi+1}, \quad (1)$$

where 'q' denotes an experience variable; M* designates the metric's optimal value; c is a coefficient; and 'φ' represents a parameter that reflects the effectiveness of management. The quantity '|M(q) – M*|' represents the magnitude of the non-value-added (NVA) or 'wasted' component of M(q), a performance gap that closes with increasing production experience [3], [15].

The empirical component of our study suggests that semiconductor manufacturers consistently engage in deliberate, continuous, persistent and sustained quality learning efforts of a constant magnitude. Time t can therefore be substituted for the generic experience variable q. For every venture j, each quality learning effort begins at t_{ij} and ends at t_j^*, the point in time at which the quality metric should achieve its optimal level. Under these circumstances, (1) generates finite forms ($\varphi > 0$) [3, p. 917-918], and the performance metrics for the previously described quality learning efforts can be expressed in terms of (2), (3) and (4).

For $t < t_{ij}$,

$$S_j(t) = S_j\left(t_{ij}\right) \quad (2a)$$

$$F_j(t) = F_j\left(t_{ij}\right) \quad (3a)$$

$$N_j(t) = N_j\left(t_{ij}\right) \quad (4a)$$

For $t_{ij} = t = t_j^*$,

$$S_j(t) = \left[S_j\left(t_{ij}\right) - S_j\left(t_j^*\right)\right]\left[1 - \left(t - t_{ij}\right)/t_j^*\right]^{dS} + S_j\left(t_j^*\right) \quad (2b)$$

$$F_j(t) = \left[F_j\left(t_{ij}\right) - F_j\left(t_j^*\right)\right]\left[1 - \left(t - t_{ij}\right)/t_j^*\right]^{dF} + F\left(t_j^*\right) \quad (3b)$$

$$N_j(t) = \left[N_j\left(t_{ij}\right) - N_j\left(t_j^*\right)\right]\left[1 - \left(t - t_{ij}\right)/t_j^*\right]^{dN} + N\left(t_j^*\right) \quad (4b)$$

In (2b), (3b) and (4b), the constants d_S, d_F and d_N determine the learning rates of the respective quality learning efforts.

It is assumed that capacity constraint eases at $t = t_j^*$, and that the quantity demanded remains constant thereafter. Then the following holds for $t_j^* < t$.

$$S(t) = S(t^*) \quad (2c)$$

$$F(t) = F(t^*) \quad (3c)$$

$$N(t) = N(t^*) \quad (4c)$$

D. Learning Leverage

Prior studies have shown that the four previously discussed, deliberate, subsystem-level learning efforts all contribute to the product output rate, $Q_j(t)$, which is defined as the total quantity of functional chips that a fab can supply from wafers that entered the production line between t and $t + \Delta t$ [14], [15], [18], [33]. An estimate of the product output rate for a particular semiconductor venture j can be given as

$$Q_j(t) = W_j(t)S_j(t)Y_j(t)N_j(t), \quad (5a)$$

where $Y_j(t)$ denotes the die-sort yield for wafers of type j that entered the production line between t and $t + \Delta t$. $Y_j(t)$ is defined as the fraction of dice that are fully functional when the wafer that contains them exits the production line. If we assume faults are randomly distributed, we may substitute a Poisson model for $Y_j(t)$. Then,

$$Q_j(t) = W_j(t)S_j(t)e^{-Fj(t)/Nj(t)}N_j(t), \quad (5b)$$

which is a highly sensitive function of t [10]. Depending on a venture's position in the lifecycle, we substitute (2a), (2b) or (2c) for $S_j(t)$; (3a), (3b) or (3c) for $F_j(t)$; and (4a), (4b) or (4c) for $N_j(t)$.

The fab has an incentive to increase $Q_j(t)$, as long as the revenue generated by producing one more chip (marginal revenue) exceeds the cost of producing that chip (marginal cost). The marginal revenue equals the marginal cost at $t = t_j^*$. Therefore,

$$Q_j\left(t_j^*\right) = W_j\left(t_j^*\right) S_j\left(t_j^*\right) e^{-Fj(tj^*)/Nj(tj^*)} N_j\left(t_j^*\right). \quad (5c)$$

We assume that capacity constraint eases at $t = t_j^*$, and that quantity demanded remains constant for all $t > t_j^*$. Then $Q_j(t) = Q_j(t_j^*)$ for all $t > t_j^*$.

The abovementioned learning efforts are subjected to varying degrees of leverage [10]. Production Quality Learning is not leveraged for the domain $t_{ij} \le t \le t_j^*$, because, according to (5b), $S_j(t)$ contributes directly to $Q_j(t)$. $S_j(t)$ is a concave, monotonic, continuous function, whose performance gap decreases over time and ideally disappears at $t = t_j^*$ [10], [14]. Production Volume Learning also has no leverage from the point of view of the product output rate because, all other factors being constant, $Q_j(t)$ is directly proportional to $W_j(t)$. By contrast, Process Quality Learning and Design Learning are highly leveraged, because the die-sort yield $Y_j(t)$ is a highly nonlinear function of die size and fault density [34]. When $F_j(t) > 2$ faults per part (fpp), then $Y_j(t)$ is very low. $Y_j(t)$ rises dramatically when 2 fpp $> F_j(t) > 0.5$ fpp. Once $F_j(t) < 0.5$ fpp, $Y_j(t)$ begins to saturate at high values [10]. $N_j(t)$ increases in discrete increments every time circuit designers shrink die size. This typically occurs once per year, suggesting that Design Learning has particularly long learning cycles [10].

Learning leverage is greatest when a fab links Production Volume Learning to quality learning. During CS, ramping to volume production concurrently with fault reduction and die shrinkage becomes affordable once die-sort yield rises rapidly, and a revolution in organizational performance takes place [15], [25], [35]. The financial success of a semiconductor venture to a large degree depends upon whether this revolution occurs on time [7]–[10], [14].

E. Financial Metrics

When wafers exit the production line, the average unit sales price of an integrated circuit that is realized by venture j can be given as

$$P_j\left(t + CT_j(t)\right) = \left[P_j(0) - P_{j-min}\right] 10^{-kPj[t+CTj(t)]} + P_{j-min}, \quad (6)$$

where $P_j(0)$, $P_j(t)$ and P_{j-min} respectively denote the average unit sales price at t = 0, the average unit sales price at the time wafers entered the production line and the asymptotic lower limit of the average unit sales price [10], [17], [18], [25]. The decay constant of the average sales price is given by k_{Pj}. $CT_j(t)$ represents fab cycle time, which is defined as the average amount of time that wafers associated with venture j, which were started between t and t + Δt, spend in the production line. $CT_j(t)$ is a highly nonlinear function of wafer starts; it increases geometrically as the fab's load (wafers of all types) approaches fab capacity [7]–[10], [17]. If k_{Pj} is high, then $P_j(t + CT_j(t))$ very sensitive to $CT_j(t)$. Under these circumstances, the average unit sales price can be significantly higher when wafers enter the production line than when they exit. Increasing the rate of Production Volume Learning may increase $CT_j(t)$, thereby adversely affecting the unit price of goods sold [17], [21].

For wafers of type j, which enter the production line between t and t + Δt, the revenue generation rate, $R_j(t)$, is given by multiplying the average unit sales price with the product output rate.

$$R_j(t) = P_j\left(t + CT_j(t)\right) Q_j(t), \tag{7}$$

where $P_j(t + CT_j(t))$ is given by (6) and $Q_j(t)$ is given by (5b). The total cash outlay rate, $C_j(t)$, for producing these wafers is given as the sum of the individual cash outlay rates of the venture's abovementioned, constituent, deliberate learning efforts: PnVL, PnQL, PcQL and DL.

$$C_j(t) = c_{PnVLj}(t) + c_{PnQLj}(t) + c_{PcQLj}(t) + c_{DLj}(t) \tag{8}$$

The costs of a particular semiconductor manufacturing venture j are incurred over a prolonged investment horizon that is given by the quantity $t\text{-}t_{ij}$. Assuming continuous cash flows, the discounted cumulative cash outlay of a venture j up to a particular point in time t is given by

$$CCO_j(t) = \int_{tij}^{t} C_j(t)e^{-\rho t}dt, \tag{9}$$

where ρ denotes the continuously compounded discount rate; $\rho = \ln(1 + \kappa)$, where κ represents the semiconductor manufacturer's effective annual cost-of-capital rate [36]. $C_j(t)$ denotes a stream of cash outlays that is given by (8).

The revenue of a particular semiconductor manufacturing venture j is accrued over a prolonged period of time that is given by the quantity $t\text{-}t_{Rj}$, where t_{Rj} denotes the point in time at which venture j releases its first product into production. By definition, $t_{ij} < t_{Rj}$. If $t_{ij} < t < t_{Rj}$, then $R_j(t) = 0$, even if $Q_j(t) > 0$, and $P_j(t + CT_j(t))$ is very high. Assuming continuous cash flows, the discounted cumulative revenue generated by venture j up to a particular point in time t is then given by

$$CRG_j(t) = \int_{t_{R_j}}^{t} R_j(t)e^{-\rho t}dt, \tag{10}$$

where $R_j(t)$ represents a revenue stream that is given by (7).

The profitability of a particular venture j at time t is generally measured by its net present value [36], $NPV_j(t)$. This criterion reflects the difference between the expected discounted cumulative revenue to be accrued by the venture over its investment horizon and the discounted cumulative cash outlays that are expected to occur over the investment horizon. Thus net present value can be expressed as

$$NPV_j(t) = CRG_j(t) - CCO_j(t), \tag{11}$$

where $CCO_j(t)$ and $CRG_j(t)$ are respectively given by (9) and (10).

Capital productivity is generally viewed as a return on invested capital, which can be human, physical or financial. In semiconductor manufacturing virtually all capital is spent on enabling learning [10]. Thus $CCO_j(t)$ serves as an excellent proxy measure for all capital that has been invested in venture j up to time t. $CRG_j(t)$ measures the return generated by all capital investments in venture j up to time t. The capital productivity of a venture j up to time t can thus be expressed in terms of a cumulative return on a cumulative investment, $CRoCI_j(t)$, where $CCO_j(t)$ and $CRG_j(t)$ are respectively given by (9) and (10).

$$CRoCI_j(t) = CRG_j(t)/CCO_j(t). \tag{12}$$

It is frequently assumed that a highly profitable venture generates a high return on investment. However, in conjunction, (11) and (12) suggest that this is not necessarily the case. A venture that is very profitable but costly may generate a relatively low return on investment, whereas a venture that is not very profitable but inexpensive may generate a relatively high return on investment. A semiconductor manufacturer may thus want to estimate $NPV_j(t)$ and $CRoCI_j(t)$ over the complete investment horizon of j, before deciding whether to pursue the leading edge or become a follower.

IV. Developing Scenarios

The CoVaL model that has emerged from the data of this study approximates the conditions under which semiconductor manufacturers engage in process development, make capitalization decisions and operate their fabs. The model has been exercised to develop six scenarios that are of particular interest to modern semiconductor manufacturers and their technology suppliers. Each scenario simulates a stylized fab under a particular set of physical and financial assumptions that are consistent with actual operating conditions in real fabs.

A. Physical Assumptions

The physical assumptions pertain to timing and wafer size, as well as to subsystem-level learning variables like die size, fault density, survival yield and wafer start rate. They are summarized in Tables I and II, as well as in Figs. 1–3. Table I displays assumptions pertaining to timing and wafer size. Table II displays the basic assumptions that pertain to quality learning. Figs. 1–3 respectively depict how the wafer start rate $W_j(t)$, fault density $F_j(t)$ and die size $N_j(t)$ evolve of over the lifecyles of the various scenarios under consideration. For all scenarios, the basic time increment, Δt, is set to three months.

Leading-edge manufacturers go through the complete process lifecycle that was described in Section III-B. They

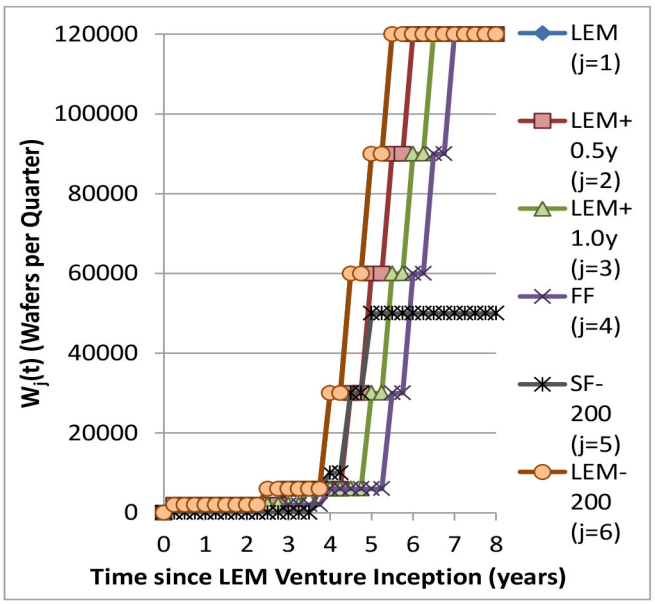

Fig. 1. Wafer start rate, $W_j(t)$, over time.

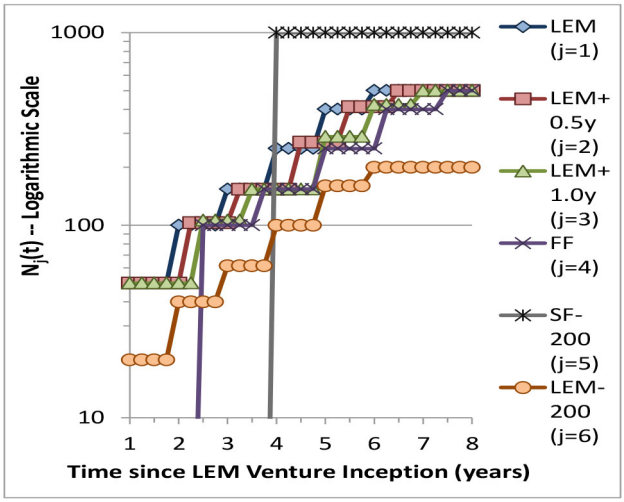

Fig. 2. Number of dice per wafer ($N_j(t)$) for various scenarios.

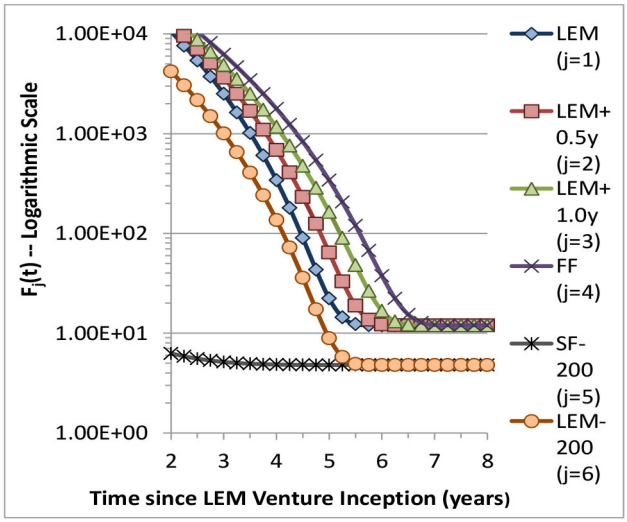

Fig. 3. Number of faults per wafer ($F_j(t)$) for various scenarios at particular points in time.

TABLE I
PHYSICAL ASSUMPTIONS FOR SCENARIOS UNDER CONSIDERATION

Scenario	*j=*	t_{ij}	t_{Rj}	t_j*	Wf. Dia.	CT_j
LEM	*1*	0.0 years	4.0 years	5.5 years	300 mm	50 days
LEM+0.5y	*2*	0.0 years	4.5 years	6.0 years	300 mm	50 days
LEM+1.0y	*3*	0.0 years	5.0 years	6.5 years	300 mm	50 days
FF	*4*	2.5 years	5.5 years	7.0 years	300 mm	50 days
SF-200	*5*	4.0 years	4.0 years	5.5 years	200 mm	33 days
LEM-200	*6*	0.0 years	4.0 years	5.5 years	200 mm	50 days

TABLE II
KEY ASSUMPTIONS ABOUT QUALITY LEARNING

Scenario	*j=*	$S(t_{ij})$	$S(t_j^*)$	d_S	$F(t_{ij})$	$F(t_{Rj})$	$F(t_j^*)$	d_F	$N(t_{ij})$	$N(t_j^*)$	d_N
LEM	*1*	0.50	0.95	3	80k fpw	341 fpw	12 fpw	5	50 dpw	500 dpw	2
LEM+0.5y	*2*	0.50	0.95	3	80k fpw	233 fpw	12 fpw	5	50 dpw	500 dpw	2
LEM+1.0y	*3*	0.50	0.95	3	80k fpw	164 fpw	12 fpw	5	50 dpw	500 dpw	2
FF	*4*	0.50	0.95	3	80k fpw	120 fpw	12 fpw	5	154 dpw	500 dpw	2
SF-200	*5*	0.95	0.95	0	5 fpw	5 fpw	5 fpw	0	1k dpw	1k dpw	0
LEM-200	*6*	0.50	0.95	3	32k fpw	136 fpw	5 fpw	5	20 dpw	200 dpw	2

pursue Production Volume Learning during joint development projects with suppliers that create leading-edge technology [19], [20]. They engage in a Process Research effort for about 2.5 years, during which they utilize a minimal equipment set. They expand their equipment set at the beginning of Pilot Development, which they pursue for about 1.5 years. During this stage, the LEM runs leading-edge product prototypes. Commercial Startup begins once leading-edge prototypes are released into production. The production line is subsequently ramped up to Volume Production in a stair-step pattern [21].

Three of the scenarios under consideration cover leading-edge manufacturers that run on wafers with a diameter of 300 mm. In the *LEM (j = 1)* scenario, the manufacturer operates in Process Research mode from $t = t_{i1} = 0$ to $t = 2.5$ years with a wafer start rate of 2000 wafers per quarter. From $t = 2.5$ years to $t = 4.0$ years, the LEM runs a pilot line at 6000 wafers per quarter. The LEM releases its product line into production at $t = t_{R1} = 4.0$ years, and ramps to Volume Production in the stair-step pattern that is observed in many fabs (see, for example, [21]). This Commercial Startup is complete at $t = t_1^* = 5.5$ years, after which the fab in *LEM (j = 1)* starts 120,000 wafers per quarter.

The *LEM + 0.5y (j = 2)* and *LEM + 1.0y (j = 3)* scenarios are based on the same assumptions except that they respectively reflect a delay in development of 0.5 years and 1.0 years. In another scenario, titled *LEM-200 (j = 6)*, a leading-edge manufacturer operates in a fab that runs wafers with diameters of 200 mm. This scenario is otherwise identical to *LEM (j = 1)*. Thus scenarios *LEM (j = 1)* and *LEM-200 (j = 6)* are indistinguishable in Fig. 1.

Fast followers do not engage in Process Research, and they limit Pilot Development by importing many of their process technologies once these are available from external sources. Instead, FFs integrate process technologies [37] and ramp up to Volume Production as rapidly as possible [19], [20]. Slow followers import process technology that is a few generations

behind the leading edge and run it on mature equipment that has mostly been amortized.

A scenario for fast followers, titled *FF (j = 4),* simulates a stylized 300-mm fab that starts 6000 wafers per quarter between t = t_{i4} = 4.0 and t = 6.0 years. Commercial Scale-up begins at t = t_{R4} = 6.0 years and lasts for 18 months (t_4* = 7.5 years). The wafer start rate during Volume Production is 120,000 wafers per month. By contrast, a scenario for slow followers, *SF-200 (j = 5)* launches a 10-year-old process (∼four technology nodes behind the leading edge) at t = t_{i5} = t_{R5} = 4 years in a fab that runs wafers with a diameter of 200 mm and ramps up to its Volume Production rate of 50,000 wafers per quarter by t = 5 years.

The assumptions for fab cycle time for all six scenarios are consistent with those of prior studies [7]–[10], [17], [18]. During Volume Production, all of the stylized fabs are loaded to 80% of capacity and run at 2.5 times intrinsic cycle time. This corresponds to an actual cycle time (CT) of 50 days for leading edge manufacturers and fast followers. The fabs of leading edge manufacturers and fast followers are loaded significantly below capacity during the ramp to volume production, but their manufacturing processes are less mature at that time. Thus, according to the input of most respondents, a cycle time of 50 days is still realistic. The fabs of slow followers are assumed to be loaded at 80% throughout their lifecycle. When they ramp up a mature manufacturing process, they replace another process that is obsolete. Fab cycle time equals 37 days for slow followers because their mature semiconductor processes contain fewer steps than those of the semiconductor processes of the leading-edge manufacturers and fast followers. In all scenarios, cycle time is constant while these fabs are generating revenue. We can thus make the simplifying assumption that, for all practical purposes pertaining to revenue generation, $CT_j(t) = CT_j$.

The assumptions regarding survival yield, dice per wafer and fault density are consistent with the practices that manufacturers in the aforementioned scenarios would deploy. $S_j(t)$, $F_j(t)$ and $N_j(t)$ follow (2), (3) and (4), respectively. The numerical values of key parameters that are associated with these variables are given in Table II.

Leading-edge manufacturers typically generate new design revisions for their products on an annual basis. Die size decays exponentially from design revision to design revision, in order to increase the number of dice that can be produced on each wafer. The impact of shrinking die size on the number of dice per wafer (dpw) is shown in Fig. 2.

Fast followers do not have to generate early design shrinks because they do not engage in early Process Research. Slow followers do not need to generate design revisions at all; they run very mature designs that are much smaller than state-of-the art designs. The *SF-200* scenario assumes that designs have already been shrunk to the point of diminishing returns (0.16 square centimeters) by product release. Wafers for *SF-200* contain 1000 of these dice.

Fig. 3 shows that fault reduction efforts also proceed at rates that are consistent with the practices of manufacturers that operate under the scenarios from above. The number of faults per wafer (fpw) decreases exponentially over time.

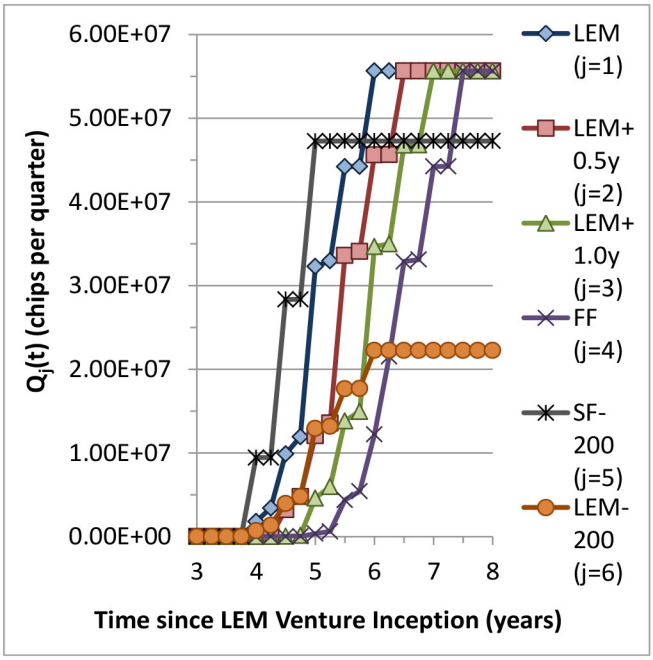

Fig. 4. Quantity of functional chips produced ($Q_j(t)$) for all six scenarios under consideration.

LEMs pursue fault reduction on an accelerated schedule; FFs follow the LEMs' schedule with a delay of one year. SFs reduce faults quite rapidly when they introduce their mature technology. They also tend to achieve a lower value for the ultimate number of faults per wafer because they fabricate smaller wafers.

B. Financial Assumptions

Financial assumptions are primarily related to the quantity of chips that are sold and their average unit sales price, which determine the revenue of semiconductor ventures, as well as to the costs of deliberate learning efforts, which act as endogenous constraints on the venture. Financial assumptions are summarized in Figs. 4 and 5 and the narrative that explains these diagrams.

Fig. 4 displays the number of functional chips produced, $Q_j(t)$, for all six scenarios under consideration. Since we are assuming capacity constraint during PR, PD and CS, as well as a stable and predictable market demand during VP, the quantity of functional chips produced equals the quantity of chips sold. By definition this number equals zero prior to product release. It surges during CS and saturates during VP. Thus the fabs in all scenarios undergo a revolution in organizational performance during CS.

Assumptions pertaining to the average unit price of the good to be sold are consistent with the historical pricing data for leading-edge semiconductor manufacturing (see, for example, [2], [21]) and the views of the respondents in this study. Except for *SF-200 (j = 5)*, all scenarios under study assume that P(t = 4 years) = U.S.$ 1000; P_{j-min} = U.S.$ 2; and k_P = 1.0. This implies leading-edge manufacturers and fast followers encounter an average unit sales price for high end chips, which equals U.S.$ 1000 when it is released into production by a leading-edge manufacturer. The

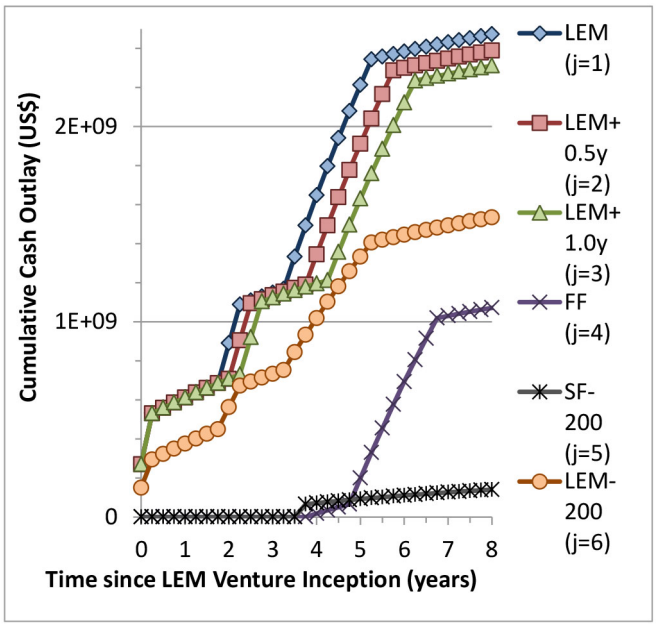

Fig. 5. Real cumulative cash outlay (CCO(t)).

price subsequently erodes to not much more than U.S.$ 2 over a period of 2.5 years. Scenario *SF-200 (j = 5)* assumes that the price of the good to be sold is constant; $P(0) = P_{j-min}$ = U.S.$ 2; $k_P = 0$.

Empirical evidence from this study, and from many that have preceded it (see, for example, [7]–[10], [15], [16], [18]), suggests that the cost of learning how to increase production volume dwarfs that of all other deliberate learning efforts. The cost of learning is consequently proportional to the intensity of Production Volume Learning. As Fig. 5 illustrates, the cumulative cash outlay (CCO(t)) grows rapidly whenever capital equipment has to be purchased, and personnel have to be hired and trained.

Fig. 5 also shows that the cost of process development and production varies from scenario to scenario. Leading-edge manufacturers, who go through the complete learning cycle, incur a cost surge at the beginning of Process Research (t∼0 years), before a pilot line is started (t∼2 years) and during the ramp to Volume Production. A fast follower does not have to invest in organizational learning at these early stages; his/her learning costs primarily accrue during the ramp to Volume Production. A slow follower has a relatively small cost-of-learning problem. He/she must invest in a very limited amount of new equipment shortly prior to product release at $t = t_{R5}$ and train very few new workers [9], [20]. After product release, a slow follower primarily incurs learning costs related to sustaining and monitoring, which is true for all scenarios during VP. Not surprisingly, Fig. 5 also indicates that fabs, which run on 200-mm wafers, incur lower development and production costs than fabs that run on 300-mm wafers.

Finally, it should be noted that both cumulative cash outlays and cumulative revenue generation are discounted at an annual rate of 15%. This rate is commensurate with the opportunity cost of capital for semiconductor ventures and consistent with the assumption of prior studies (see, for example, [7]–[10], [14]–[16], [17]).

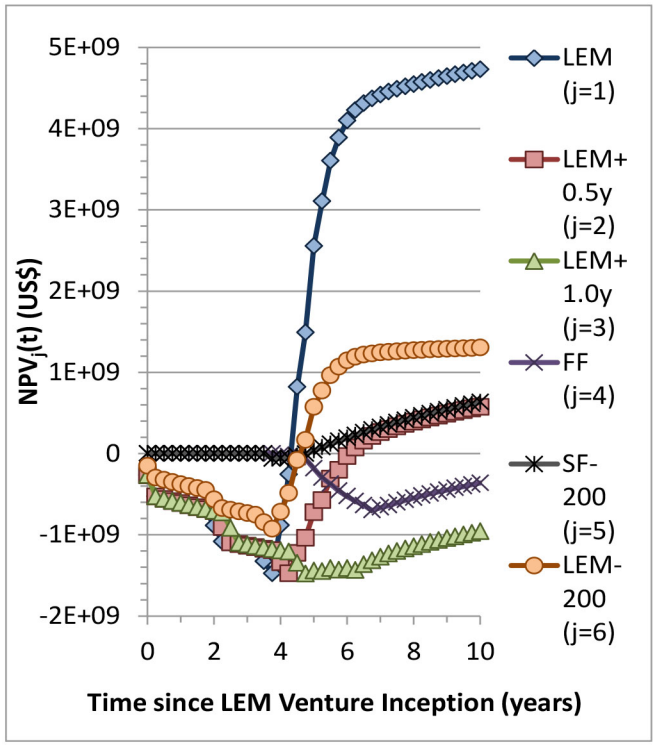

Fig. 6. Net present value ($NPV_j(t)$) for the six scenarios under consideration.

V. Results: Profitability Versus Capital Productivity

Fig. 6 illustrates that the net present value of the five scenarios that have been described in Section IV varies enormously. $NPV(t_1^*)$ for *LEM (j = 1)* is very high — the expected discounted cumulative profit, $NPV_1(t = 10$ years) approaches U.S.$ 5 billion. However, over 90% of this profit was generated between t = 4 years and t = 7 years. A six-month delay causes more than 80% of this profit to evaporate, and a one-year delay induces a loss of about U.S.$ 1 billion. A leading-edge manufacturer that produces in a 200-mm fab, ultimately generates less that 30% of the profit generated by one that produces in a 300-mm fab.

Fast followers do not break even. Evidently, saving U.S.$ 2 billion in development costs does not make up for the loss of revenue that they incur from consciously delaying the ramp to volume production. Slow followers make a profit of about U.S.$ 600 million by t = 10 years, which amounts to less than 15% of the profit of a successful LEM.

Fig. 7 displays $CRoCI_j(t)$ for the six scenarios that have been described in Section IV from venture inception for the leading-edge manufacturer (t = 0) to maturity (t = 10 years). In the *LEM (j = 1)* scenario, $CRoCI_1(t)$ surges between t = 4 and t = 7 years, but saturates thereafter slightly below 3. In the *LEM-200 (j = 6)* scenario, $CRoCI_6(t)$ surges between t = 4 and t = 6 years, but saturates thereafter slightly below 2. In *LEM + 0.5y (j = 2)*, $CRoCI_2(t)$ reaches its breakeven value of 1.00 by t = 6 years, but does not reach 1.5 by t = 10 years. The *LEM + 1.0y (j = 3)* scenario and the *FF (j = 4)* scenario do not break even by t = 10 years. By contrast, in

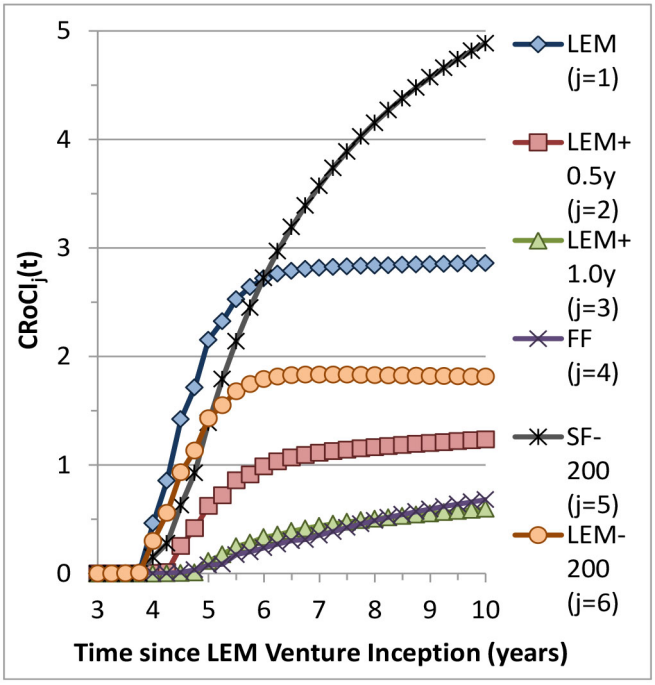

Fig. 7. Cumulative return on cumulative investment (CRoCI(t)).

the *SF-200 (j = 5)* scenario, $CRoCI_5(t)$ rises sharply immediately after its 10-year-old product line goes into production on mature, amortized equipment, and it continues to increase as time passes. *SF-200 (j = 5)* shows no sign of saturation by t = 10 years.

For the *LEM*, *LEM + 0.5y*, *LEM + 1.0y*, *LEM-200* and *FF* scenarios, the results that are displayed in Fig. 7 are consistent with those that are depicted in Fig. 6. This suggests that profitability is correlated to return on investment and capital productivity. Making large investments results in large profits, but only if the majority of these investments is recovered within two years. Delays are deadly. By contrast, realizing product lines that are not at the leading edge on mature processes using amortized equipment constitutes a business practice that is financially sustainable in perpetuity, even though it is not nearly as profitable as manufacturing advanced integrated circuits with leading-edge process technology.

VI. Conclusion

This paper has presented an empirical study of organizational learning and capital productivity in semiconductor manufacturing. What has emerged from the data of this study is a theoretical framework for the cost and value of learning that suggests organizational learning and capital productivity are linked. This framework integrates variables that characterize deliberate volume learning and quality learning efforts with endogenous constraints, such as fab capacity and the cost of learning, and with environmental factors, such as the average unit price of the good to be sold and the opportunity cost of capital [9]. Net present value [36] and cumulative return on cumulative investment are the output variables of the CoVaL model; they respectively act as proxies for profitability and capital productivity.

Empirical evidence from the study described in this paper suggests that learning practices in the semiconductor industry are consistent with extant theory on organizational learning [3]–[6]. New experiences are gained when production volume is increased in a nearly linear manner [4]. Quality learning follows Lotka-Volterra models that simulate the behavior of 'predator and prey' [3]. As a result, the CoVal model in this paper can characterize how organizational learning phenomena impact time to market, time to volume and time to payback [25], as well as capital productivity in semiconductor manufacturing [1].

The CoVaL model in this paper illustrates in particular how organizational learning impacts profitability and capital productivity in an urgent environment. For example, Process Quality Learning, which has a highly leveraged impact on the quantity of chips supplied, is literally in a race with the average unit price of the good to be sold. The requisite cash outlays for Commercial Startup are affordable only after fault density drops below an average of one fault per part, the point at which die-sort-yield surges. If this surge occurs while the average unit sales price is still high, then substantial revenue can be generated—profit and capital productivity can be high. If this surge is delayed, then profitability and capital productivity can fall below expectations very dramatically (see Figs. 6 and 7). Profitability and capital productivity consequently critically depend on whether revolutions in organizational performance occur in a timely manner [9], [14].

The CoVaL framework helps semiconductor manufacturing managers make fundamental strategic decisions pertaining to capital investment and point of entry. Three basic strategic options – LEM, SF and FF – were explored in this paper by developing six scenarios: *LEM (j = 1)*, *LEM + 0.5y (j = 2)*, *LEM + 1.0y (j = 3)*, *FF (j = 4)*, *SF-200 (j = 5)* and *LEM-200 (j = 6)*. Profitability and return on investment for each of these scenarios are summarized in Figs. 6 and 7, respectively.

The following conclusions can be drawn from the six scenarios under consideration.

1) In semiconductor manufacturing, profitability and return on investment can be conflicting metrics. Investment strategies that maximize profit limit return on investment, and conversely. The profitability of a leading-edge venture may be an order of magnitude higher than that of a slow follower. However, under no circumstances that the respondents have considered realistic could the leading-edge manufacturer obtain the return on investment that the slow follower did. Conversely, under no circumstances could a well-run slow follower become as profitable as a well-run leading-edge manufacturer. The average sales price of the goods to be sold is simply too low.
2) The exponentially decaying unit price of the good to be sold limits profitability and capital productivity in a state-of-the-art product line [10], [14]. Early entry is strongly recommended for LEMs and FFs; delays will severely impede profitability.
3) Looking forward, only two investment scenarios are financially viable: *LEM (j = 1)* and *SF-200 (j = 5)*.

Fast follower strategies are no longer feasible, because a delayed Commercial Startup prevents the fast follower from recovering his/her investment in capital equipment. Avoiding development costs does not make up for the difference.

4) Leading-edge manufacturing forces the LEM to increase wafer size whenever that becomes possible. An LEM that owns a 300-mm fab could lower the price of a particular part below the production costs of a 200-mm fab and still make a profit. An LEM with a 200-mm fab would then be driven out of business [2]. Equipment suppliers consequently have no economic incentive to provide their customers with 200-mm equipment that keeps up with Moore's Law. A manufacturer that does not upgrade to larger wafer sizes when they become available is thus *de facto* a slow follower [19], [20].

The findings of the empirical study that has been described in this paper have potentially significant implications for semiconductor manufacturing practice. For example, the CoVaL model in this paper can clearly determine if and when it makes sense for a particular manufacturer to advance to the next technology node, adopt the next lithography technology or to invest in a factory that runs the next wafer size. The model's scenario planning capabilities help practicing managers decide which of these options they should pursue. A failure to make these fundamental strategic decisions in a timely manner may result in multi-billion dollar losses. However, these losses can be avoided by proactively applying a properly customized model as a strategic planning tool.

The CoVaL model in this paper has three clear limitations that need to be addressed before it can be applied on a broad basis. These limitations can all be overcome by further research, much of which is already being pursued.

1) The model simulates a base case, which, according to the expert opinion of the respondents, describes the economic environment of early 2014. The model can consequently be applied directly to decisions that need to be made in 2014. However, trajectories for average sales price have been known to vary dramatically over the last 30 years [2], [21]. It is therefore necessary to characterize the impact on profitability and return on investment of varying the initial value, the decay rate and the floor of the average unit sale price. This work is currently in progress [7], [9].
2) The respondents have indicated that no conceivable 'killer app' can possibly completely recover the total investment in a 300-mm wafer fab. LEMs will therefore have to run multiple product lines to achieve the profits suggested in Fig. 6 or the capital productivity that can be inferred from Fig. 7. Research that addresses this problem has been conducted, but requires empirical validation in real wafer fabrication facilities [18].
3) For LEMs, the cost of designs and the cost of photomasks are escalating along with the cost of plant equipment. These costs could constrain product development at leading edge manufacturers because large volumes of a particular design have to be realized for these costs to be amortized. Prior work that has been done in this area [16] suggests that design-specific CoVaL models need to be developed to help semiconductor manufacturers decide whether they should realize a particular design or not.

Finally, it should be noted that the line of reasoning that led to the conclusions of this paper will most likely be repeated when the semiconductor industry will consider a move to extreme ultra-violet (EUV) lithography and to 450-mm wafers. The Design Learning that results from EUV can in principle increase the capital productivity of EUV equipment to the point where it can be amortized. Manufacturers that run on EUV equipment would still be able to make a profit, if they were to charge unit sales prices that are below the unit cost at which manufacturers without EUV equipment could produce. Analogously, manufacturers that run on 450-mm wafers should be able charge unit sales prices that are below the unit cost at which manufacturers that run on 300-mm wafers can produce and still make a profit. A manufacturer that does not invest in EUV and in 450-mm wafer lines will subsequently be relegated to slow follower status. When the time comes, a CoVaL model can help the individual manufacturer decide whether to make the required additional investment or whether to abandon the Moore's Law trajectory.

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