The Potential for Economic Application of Maskless Lithography in Semiconductor Manufacturing

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***Abstract*—Maskless lithography has never played more than a niche role in semiconductor manufacturing, but with costs of masks for hard layers rising and the numbers of masks purchased over product lifetimes increasing, there is renewed interest today in maskless lithography. We assess the economics of production application of maskless lithography at the 45-nm technology node assuming the availability of a maskless lithography tool with various throughput capabilities. The analysis finds that selective and shrewd application of maskless lithography to layers with the most expensive masks and shortest mask lives would be economically attractive to many fabrication operations even for 300-mm maskless tool throughputs less than five wafers per hour. While a vendor of the desired maskless tools does not now exist, the business case for such a vendor is shown to be promising.**

***Index Terms*—Economic analysis, electron beam lithography, maskless lithography, semiconductor manufacturing, silicon processes.**

I. Introduction

DIRECT writing of patterns onto semiconductor wafers in volume production has been a goal of many in the semiconductor industry since the early 1960s. The elimination of the mask required for optical lithography not only would simplify the process but also would greatly enhance the flexibility, control, and speed of new product and process introductions. Yet despite extensive research and development, maskless lithography (ML) has been used in production only in a few limited instances [1] and has not been an economically viable manufacturing lithography alternative since the early 1990s. However, the approach has received renewed interest recently as the cost of masks for advanced subwavelength semiconductor processes has become prohibitive for many semiconductor device designers and users because of the combination of increased mask unit cost and decreased mask life in production [2]. It therefore seems an appropriate time to assess the economic potential for application of maskless lithography in mainstream CMOS production.

In this paper, we assess the economic issues associated with implementing maskless lithography in production at the 45-nm node for both semiconductor manufacturers and lithography tool suppliers in order to evaluate the potential of the technology for semiconductor manufacturing. Maskless lithography user financial assessments usually start with an economic analysis of the costs associated with ML implementation in production, particularly as compared to a conventional optical masked alternative. A number of authors have carried out such assessments based on tool cost-of-ownership considerations [3], [4]. However, comprehensive economic analyses are very complex because there are a variety of manufacturing mix-and-match strategies involving maskless and masked lithographic tools that can be implemented, each having its own effects on the manufacturing flow and efficiency within a production line, each having a different number and complexity requirement of masks that are needed for a given process, and each having its own advantages and disadvantages as a function of the average number of wafers processed per mask set and product mix. Furthermore, it is expected that implementation of maskless tools for any strategy will result in different product yield than that of a conventional masked approach and will also result in different design rule possibilities at a given semiconductor node that might alter the die size and performance of a given product. Since a simple tool cost-of-ownership analysis does not adequately address many of these important complexities, the economic analysis provided here is based on modeling the entire lithography portion of a complete fabrication facility for each of the several different potential ML manufacturing strategies considered, then comparing the total lithography cost per wafer and per die for each.

In carrying out the economic assessment, it has been assumed that both maskless and masked systems are available at the considered semiconductor process node for some known capital cost. Both kinds of tools are assumed to meet the nominal resolution and other patterning specifications associated with that node at some characteristic wafer throughput rate and clean room footprint. While there is considerable information on availability, cost, throughput, and footprint of masked tools through at least the 30 nm generation, there is little comparable information available on maskless tools that might be practical for production applications. Currently available maskless systems have very low throughput and are used primarily in R&D applications. However, there are research and development programs on higher throughput maskless lithography systems at a number of companies worldwide. In January 2005, SEMATECH organized and hosted a workshop on maskless lithography with more than 100 attendees and where more than a dozen different ML approaches under study were described and discussed. Most of these schemes were projected to result

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in tools capable of 300-mm wafer throughputs in the 5 wafers/h range, but none of the schemes was projected to deliver throughputs comparable to the 50+ wafers/h throughputs of current and projected masked lithography systems. Nonetheless, the analysis provided here shows that even at these lower throughputs, the implementation of maskless tools in production can provide significant economic advantages in a semiconductor fabrication facility over an all-masked lithography approach depending on the implementation strategy and the product mix.

The next section provides a description of the model for the lithography portion of a production facility that is used in the analysis. This model was developed by the authors as part of a Sematech-funded study of the ML business cases in 2005. Parameters for a representative 45-nm production facility scenario are entered into the model, and a description of the six alternative lithography strategies within such a facility that were chosen for analysis—two masked strategies, one totally maskless strategy, and three mix-and-match strategies with maskless and masked tools—are provided. The final section of this paper provides the economic assessment of the model results both from a maskless tool user and a maskless tool supplier perspective.

II. Economic Model for Lithography Manufacturing Analysis

A. Model Overview

The model we have developed is a spreadsheet-based model for assessing the economics of alternative strategies for lithography manufacturing. It computes lithography-related costs borne by a semiconductor manufacturer, considering costs for exposure equipment, mask cleaning equipment, masks, lithography materials and chemicals, staff, and clean-room space. This model is an outgrowth of the Cost-Resource Model [5] used for many years by Sematech and its member companies.

With our model, we go beyond cost analysis to also calculate lithography cycle times and their impacts on revenues. The model computes predicted lithography cycle times and also fab revenues associated with the lifetime die output. The calculated fab revenue is a function of an assumed initial die price, an assumed rate of decline in unit die prices with time, the calculated lithography cycle time, and an assumed nonphoto cycle time. Major outputs of the model are as follows:

- lithography-related wafer cost, broken down by tool capital cost (including vendor service), mask cost, materials cost, and staffing cost;
- lithography-related die cost;
- lithography cycle time (total and by mask layer);
- average revenue per die (over entire product life);
- average contribution per die (average revenue less lithography-related die cost).

B. Input Parameters

The input parameters of the model are classified into fab-level parameters (i.e., parameters assumed to be independent of lithography strategy) and tool-level parameters (i.e., parameters that may vary as a function of lithography strategy). Table I lists the input parameters along with the notation used in this paper.

Mask layers are classified into "hard," "medium," and "easy" categories. (Hard layers include the layers for gate definition; medium layers are mostly metal and via layers; and easy layers are mostly implant layers. The different categories of layers are amenable to the application of lithography tools with different levels of sophistication and cost.)

As suggested by the entries in Table I, the way that mask costs are integrated into the model is to assume a specific average cost for each of the three different kinds of masks over the life of the product and an average number of wafers processed/mask during the two stages of production. Such an approach was chosen because it is convenient from a modeling point of view, but it places more demands on the user of the model to assure that the parameters entered are reflective of the actual product manufacturing situation. First, mask costs are known to be more expensive during the early stages of a new process technology node, so the average mask costs entered in the model need to reflect this variation. Secondly and more important, however, an accurate financial analysis of different lithographic manufacturing schemes requires that all masks purchased over a product life, from the early development stage through to end of life, need to be included. Certainly one set of masks represents the minimum lifetime mask cost for any product. However, there are many reasons why the actual mask cost may be considerably higher. For example, there may be several design iterations during the development phase. During early production, there may be additional partial or complete mask set revisions for reasons such as yield enhancement, process changes, minor layout modifications, or mask damage/breakage. For some higher volume products, the production life of the hard-layer masks is often limited in wafer exposures to values below the lifetime wafer build, and therefore may need to be replaced one or more times prior to end of production life. In addition, there may be strategic reasons for purchasing additional mask sets, such as having a spare mask set always available within the fab to avoid production delays in case of mask breakage. The model allows for these complexities to be addressed by entering appropriate values for the average number of wafers processed per mask set during each of the two production stages that take them into account.

C. Analytical Formulas Concerning Cost

Let W denote the average wafer starts rate per day per product. In terms of the user-specified parameters, W is given by

$$W = \frac{\mathrm{PLB}}{\mathrm{RT} + \mathrm{AT}} \tag{1}$$

where PLB is the average device lifetime build volume, RT is duration of the device ramp (in days), and AT is the duration of device life after ramp (in days). The wafer starts rate for each product is assumed to ramp up linearly during the ramp time RT from 0 to 2 W and then ramp down linearly during the life after ramp from 2 W to 0. The total ramp volume (RV) for a product is

$$\mathrm{RV} = \left(\frac{52 * \mathrm{FSR}}{N}\right)\left(\frac{\mathrm{RT}}{360}\right) \tag{2}$$

TABLE I
INPUT PARAMETERS FOR LITHOGRAPHY ECONOMIC ANALYSIS

Fab-level input parameters	*Notation (if any)*
Total fab wafer starts per week	*FSR*
Number of products in production	*N*
Average lifetime build quantity (wafers) per product	*PLB*
Average duration for ramp-up following transfer to production (months)	*RT*
Average duration for mature production (months)	*AT*
Wafer size (diameter in mm)	*D*
Manufacturing lot size (wafers)	
Lithography tool utilization limit (as a fraction of availability)	*UMAX*
Lithography tool life (years)	*EQL*
Clean room life (years)	*CRL*
Staffing costs for engineers, technicians and operators ($ per year)	*LC*
Initial average selling price per die	
Rate of price erosion (fraction lost in one year)	*ER*
Line yield	*LY*
Number of lithography mask layers by layer category (hard, medium, easy)	*ML*
Product- and Tool-level input parameters	*Notation (if any)*
Die size	*ds*
Die yield	*DY*
Lithography processing rates by layer category	*WPH*
Lithography rework rate	*RW*
Lithography materials cost per wafer (cost for resist and other chemicals)	
Lithography tool availability	*AB*
Lithography tool investment cost	*CC*
Vendor service cost (per tool per year)	*VS*
Lost time to change between lithography recipes by layer category	*st*
Average number of lots processed between recipe changes, by layer category	*b*
Number of qualified tools available to a manufacturing lot, by layer category	*m*
Mean duration of lithography tool downtime events	*MTTR*
Squared coefficient of variation for duration of lithography tool downtime events	cr^2
Staffing requirements per lithography tool	*HC*
Lithography tool clean-room footprint	*SC*
Mask cost for each of the three types of layers	*RC*
Number of layers processed using same mask	*NLR*
Average wafers processed/mask during ramp, by layer category	*RLR*
Average wafers processed/mask during mature production, by layer category	*RLA*
Mask cleaning tool investment cost	*CC*
Clean-room footprint for mask cleaning tool	*SC*
Staffing requirements per mask cleaning tool	*HC*
Processing rate for mask cleaning tool	*UPH*
Number of wafers passes between mask cleans	*WBC*

where FSR is the total fab starts rate per week and N is the number of product types in production. The total product volume after ramp AV is

$$\mathrm{AV} = \left(\frac{52 * \mathrm{FSR}}{N}\right)\left(\frac{\mathrm{AT}}{360}\right). \tag{3}$$

The count of masks required by layer category RQ is computed as

$$\mathrm{RQ} = \mathrm{CEILING}\left\{\left[\mathrm{CEILING}\left(\frac{\mathrm{RV}}{\mathrm{RLR}}\right) + \mathrm{CEILING}\left(\frac{\mathrm{AV}}{\mathrm{RLA}} - \left[\mathrm{CEILING}\left(\frac{\mathrm{RV}}{\mathrm{RLR}}\right) * \mathrm{RLR} - \mathrm{RV}\right]\right)\right] * (1/\mathrm{NLR}) * (\mathrm{ML})\right\} \tag{4}$$

where CEILING denotes the roundup to the next integer, RLR denotes the mask life during ramp (wafers), RLA denotes the mask life after ramp (wafers), NLR denotes the number of layers per mask (greater than one in the case of multilayer masks), and ML denotes the number of masked layers (equal to zero if maskless lithography is employed).

The mask cost per wafer is computed as

$$\frac{\sum_i \mathrm{RC}_i * \mathrm{RQ}_i}{\mathrm{LY} * (\mathrm{RV} + \mathrm{AV})} \tag{5}$$

where RC_i is the unit cost for mask type i, RQ_i is the required quantity of mask type i calculated as above, and LY is the line yield.

The count of lithography tools required TC is calculated as

$$\mathrm{TC} = \mathrm{CEILING}\{[(\mathrm{FSR}) * (1 + \mathrm{LY})/2 * (1 + \mathrm{RW}) * (\mathrm{ML}) * (1/\mathrm{WPH} + st/b)]/(\mathrm{AB} * \mathrm{UMAX})\} \tag{6}$$

where RW is the rework rate, ML is the number of mask layers performed by the subject tool type, WPH is the wafer process rate, *st* is the recipe change time, b is the number of wafers between recipe changes, AB is the availability, and UMAX is the specified maximum utilization of availability. For mask cleaning tools, a similar formula is developed

$$\mathrm{TC} = \mathrm{CEILING}\left\{\left[(\mathrm{FSR})*(1+\mathrm{LY})/2 *(1+\mathrm{RW})*\left(\sum_i (\mathrm{ML}_i)*(1/\mathrm{WBC}_i)\right) *(1/\mathrm{UPH})\right]/(\mathrm{AB}*\mathrm{UMAX})\right\} \quad (7)$$

where ML_i is the number of mask layers of type i, WBC_i is the allowed number of wafers processed in layer type i between mask cleans, UPH is mask cleaning rate (expressed in masks per hour), AB is the availability of the mask cleaning tool, and UMAX is the specified maximum utilization of availability.

The lithography-related capital cost per wafer, accounting for lithography tools, mask cleaning and inspection tools, and required clean room space is computed as

$$\frac{\sum_i \mathrm{TC}_i * \mathrm{CC}_i}{52*\mathrm{FSR}*\mathrm{LY}*\mathrm{EQL}} + \frac{\sum_i \mathrm{SC}_i * \mathrm{CR}}{52*\mathrm{FSR}*\mathrm{LY}*\mathrm{CRL}} \quad (8)$$

where TC_i is the tool count for equipment type i as computed above, CC_i is the unit capital cost for tool type i, FSR is the fab starts rate per week, EQL is the equipment life (years), SC_i is the space count for equipment type i, CR is the unit clean room space cost, and CRL is the clean room life (years).

The tool vendor support cost per year is calculated as

$$\frac{\sum_i \mathrm{TC}_i * \mathrm{VS}_i}{52*\mathrm{FSR}*\mathrm{LY}} \quad (9)$$

where VS_i is the vendor support cost per year per tool.

The lithography labor cost per wafer is computed as

$$\frac{\sum_j \sum_i \mathrm{LC}_j * \mathrm{HC}_{ji} * \mathrm{TC}_i}{52*\mathrm{FSR}*\mathrm{LY}} \quad (10)$$

where LC_j is the unit labor cost for labor type j (engineers, engineering technicians, and manufacturing operators) and HC_{ij} is the head count of labor type j per tool of type i. The material cost per wafer is simply computed as the user-specified material cost per wafer divided by the line yield.

Die costs are developed as follows. The gross die per wafer are computed according to

$$\frac{\pi(D/201)^2}{ds} \quad (11)$$

where D is the wafer diameter in millimeters and ds is the die size in square centimeters. (It is assumed that one centimeter of wafer radius accounts for edge and k_{erf} losses.) Die yield is applied to the gross die figure developed as above to obtain the net die per wafer. The lithography wafer cost is divided by the net die per wafer to obtain the lithography die cost.

D. Analytical Formulas Concerning Cycle Time and Revenue

The utilization of lithography tools is calculated as

$$[(\mathrm{FSR})*(1+\mathrm{LY})/2*(\mathrm{ML})(1/\mathrm{WPH}+st/b) *(1+\mathrm{RW})]/[\mathrm{TC}*168] \quad (12)$$

where ML is the number of mask layers performed by the subject tool type, WPH is the wafer process rate, *st* is the recipe change time, b is the number of wafers between recipe changes, RW is the rework rate, and TC is the tool count as calculated above.

Analytical formulas from queuing theory are applied to estimate lot wait times contributing to total lithography cycle time [6]. Queuing-theoretic waiting time ("queue time") has two components: the wait time for setup of a batch of lots with a common product and mask layer plus the average time for a lot to wait for its turn within the batch once it starts to be run. The general formula for queue time that is applied is

$$\mathrm{QT}_{jk} = \left(\frac{\frac{ca^2}{b_{jk}} + ce_{jk}^2}{2}\right)\left(\frac{u_k^{\sqrt{2(m_j+1)}-1}}{m_j(1-u_k)}\right) \times \left(\frac{b_{jk}\mathrm{PT}_{jk}+st_k}{\mathrm{AB}_k}\right) + (b_{jk}\mathrm{PT}_{jk}+st_k)\left(\frac{1}{\mathrm{AB}_k}-1\right)+\mathrm{BT}_{jk} \quad (13)$$

where we have (14) and (15) as shown at the bottom of the page. Here, QT_{jk} is the expected queue time at a photo step of layer type j processed on equipment type k, ca^2 is the squared coefficient of variation of the lot interarrival time (taken to be unity in this analysis), u_k is the utilization of availability of equipment type k, m_j is the number of qualified tools available to the lot at a layer type j, PT_{jk} is the process time per lot for layer type j when assigned to tool type k, AB_k is the availability of tool type k, st_{jk} is the setup time for layer j when performed on tool type k, b_{jk} is the average number of lots per layer-batch, ce_{jk}^2 is the squared coefficient of variation in lot service time for layer j when assigned to tool type k (including contributions of variability from lot process time, machine downtime, and setup batches), c_0^2 is the squared coefficient of variation of lot process time (taken to be unity in this analysis), cr_k^2 is the squared coefficient of variation of down time

$$ce_{jk}^2 = \frac{b_{jk}c_0^2\mathrm{PT}_{jk}^2 + st_{jk}^2 + \left(1+cr_k^2\right)\mathrm{AB}_k(1-\mathrm{AB}_k)(\mathrm{MTTR})_k)(b_{jk}\mathrm{PT}_{jk}+st_{jk})}{(b_{jk}\mathrm{PT}_{jk}+st_{jk})^2} \quad (14)$$

$$\mathrm{BT}_{jk} = \left[\frac{b_{jk}-1}{2}\right]\mathrm{PT}_{jk} \quad (15)$$

events on tool type k, MTTR_k is the average length of a downtime event on tool type k, and BT_{jk} is the average time for a lot to wait for its turn within a batch of lots in mask layer j that are being processed on equipment type k. The first term in (13) is the queuing-theoretic wait time until the layer-batch is set up to run, the second term is a relatively small correction factor for the difference between the queuing-theoretic process time for a batch $(b_{jk}\mathrm{PT}_{jk}+st_k)/(\mathrm{AB}_k)$ and the actually observed process time for the batch $b_{jk}\mathrm{PT}_{jk}+st_k$, and the last term is the average time a lot must wait for its turn within a layer batch.

Total cycle time CT in layers of type j is computed according to

$$\mathrm{CT}_{jk} = \mathrm{ML}_j * (\mathrm{QT}_{jk} + st_k + \mathrm{PT}_{jk} + 0.5) \tag{16}$$

where ML_j is the number of layers of type j, QT_{jk} is the queue time as calculated in (13), st_k is the setup time for layer-batches, PT_{jk} is the lot process time for a layer of type j performed by equipment type k, and 0.5 (hours) term is an allowance for the coat/develop lot cycle time in each layer.[1] The cycle time is thus the sum of the waiting time, the batch setup time, the lot process time, and the coat/develop time.

The price erosion per year specified by the user is translated into an equivalent exponential discount rate per day α. That is

$$e^{-\alpha 360} = 1 - \mathrm{ER} \tag{17}$$

or

$$\alpha = \frac{-\ln(1-\mathrm{ER})}{360} \tag{18}$$

where $\ln$ denotes the natural logarithm and ER denotes the given erosion rate per year. The total lifetime revenue per product is then given by

$$\int_0^{\mathrm{RT}+\mathrm{AT}} R_0 W(t) e^{-\alpha(t+CT)} dt \tag{19}$$

where R_0 is the initial revenue per wafer (initial die ASP times line yield times the net die per wafer) and $W(t)$ is the wafer starts rate per day at time t.

The wafer starts rate is assumed to ramp up linearly during the ramp time RT from zero to $2W$ and then ramp down linearly during the life after ramp from $2W$ to zero. While this may not accurately model the actual situation for a given product, it has been found that most of the analysis results are relatively insensitive to the specific production rate assumptions as a function of time. The wafer starts rate function is therefore expressible as

$$W(t) = \begin{cases} 2W\frac{t}{\mathrm{RT}} & t \in (0, \mathrm{RT}] \\ 2W - 2W\frac{(t-\mathrm{RT})}{AT} & t \in (\mathrm{RT}, \mathrm{RT}+\mathrm{AT}] \end{cases}. \tag{20}$$

[1]Excluding the correction factor (second term) in (13), (13)–(16) are applications of [6, Table 8.2, Eq. 8.28, Eq. 9.5].

Plugging (20) into (19), we express the total device lifetime revenue as

$$\begin{aligned} &\int_0^{\mathrm{RT}} R_0 \frac{2W}{\mathrm{RT}} t\, e^{-\alpha(t+\mathrm{CT})} dt \\ &\quad + \int_{\mathrm{RT}}^{\mathrm{RT}+\mathrm{AT}} R_0 \left[2W - \frac{2W}{AT}(t-\mathrm{RT})\right] e^{-\alpha(t+\mathrm{CT})} dt \\ &= 2WR_0 e^{-\alpha \mathrm{CT}} \left\{ \int_0^{\mathrm{RT}} \frac{1}{RT} t\, e^{-\alpha t} dt \right. \\ &\quad \left. + \int_{\mathrm{RT}}^{\mathrm{RT}+\mathrm{AT}} \left[1 - \frac{1}{\mathrm{AT}}(t-\mathrm{RT})\right] e^{-\alpha t} dt \right\}. \end{aligned} \tag{21}$$

The first integral is equal to

$$\frac{1}{\mathrm{RT}} \int_0^{\mathrm{RT}} t\, e^{-\alpha t} dt = \frac{1}{\mathrm{RT}} \left[\frac{1}{\alpha^2} - \frac{\alpha \mathrm{RT}+1}{\alpha^2} e^{-\alpha \mathrm{RT}}\right] \tag{22}$$

and the second integral is equal to

$$e^{-\alpha \mathrm{RT}} \left[\frac{1}{\alpha}(1 - e^{-\alpha \mathrm{AT}}) - \frac{1}{\mathrm{AT}} \left(\frac{1}{\alpha^2} - \frac{\alpha \mathrm{AT}+1}{\alpha^2} e^{-\alpha AT}\right)\right]. \tag{23}$$

The coefficient term

$$2\mathrm{WR}_0 e^{-\alpha \mathrm{CT}} \tag{24}$$

is evaluated with W given by (1) and CT given by (16) plus an assumed allowance of 30 days for nonphoto cycle time.

III. Lithography Manufacturing Alternatives Considered

A. Scenario for Study

We exercised the model with a range of inputs and assumptions, but here we provide a specific scenario that illustrates most of the key economic issues related to ML as a baseline for discussion. We consider a hypothetical 45-nm process technology for fabrication of CMOS circuits on 300-mm wafers in standard 25-wafer lots as well as half-size 13-wafer lots. The process includes six "hard" mask layers, 16 "medium" layers, and 18 "easy" layers. Costs incurred by a fabrication line starting 10 000 wafers per week are assessed. We assume a nominal average lifetime number of production wafers, or lifetime product build, processed in the factory per product as a parameter that is varied in the analysis, and assume that all products experience 12 months of ramp-up after development and 16 months of mature production. For an average lifetime build of 25 000 wafers, this leads to an average of about 48 products in production at any given time. If the lifetime wafer build is 5000 wafers, there will be an average of about 240 products in production at any given time.

Mask costs at the 45-nm technology node are assumed to average \$5000 for easy layers, \$75 000 for medium layers, and \$200 000 for hard layers over the life of all products.[2] For con-

[2]These figures were obtained in private communication and are based on actual expenditures at a large IC manufacturer that wishes to remain anonymous.

ventional all-optical lithography, this translates into a mask-set cost of $2.49 million.

Lithography tool throughputs are as follows: for optical tools assigned to hard and medium layers, a throughput of 70 wafers per hour of utilization is assumed. For optical tools assigned to easy layers, a throughput of 62 wafers per hour is assumed.[3] For maskless tools assigned to a variety of layers, an average throughput of five wafers per hour is assumed. For maskless tools assigned to gates and contact layers only, a throughput 50% higher than the nominal throughput of a maskless tool is assumed, i.e., the maskless tools used only for gates and contacts have an average throughput of 7.5 wafers per hour. The higher throughput assumed for these layers reflects the fact that some maskless tool architectures lead to higher throughputs for simple and sparse patterns than for more complex and dense patterns, and in this alternative, only sparse and simple patterns are exposed by the maskless tool to take advantage of this maskless tool feature. The lithography rework rate is assumed to be 0.02, regardless of lithography tool type or layer category.

Investment costs for optical tools are assumed to be $30 million for tools assigned to hard layers, $12.5 million for tools assigned to medium layers, and $7.5 million for tools assigned to easy layers. The investment cost for maskless tools is assumed to be $20 million. All tool investment costs are assumed to include the cost of the associated track systems. Vendor support costs of $150 000 per hard-layer tool, $100 000 per medium-layer tool, and $50 000 per easy-layer tool are assumed, regardless of whether the tool is optical or maskless. Materials costs of $50 per wafer are assumed, again independent of tool type. The utilization limit is assumed to be 90% of availability, regardless of tool type. Availabilities achieved are assumed to be 95% for optical tools performing easy layers, 92% for optical tools performing medium layers, and 90% for optical tools performing hard layers as well as all maskless tools. The equipment life is assumed to be eight years for all types of lithography tools.

Mask cleaning tools are assumed to cost $5 million, achieve a throughput of two masks per hour of utilization, and achieve 90% availability. The number of passes between mask cleans is known to be highly dependent on the particular fabrication line and its chosen manufacturing methodology. Here we have assumed an aggressive cleaning regimen with mask cleaning every 100 exposures for hard layers, 300 for medium layers, and 900 for easy layers, although we found that the results and conclusions of our analysis are relatively insensitive to the cleaning values assumed.

Staffing requirements are assumed as follows: 0.25 engineers, 0.5 technicians, and 0.75 operators per lithography or cleaning tool, regardless of type. Staffing costs per year are assumed to be $150 000 for engineers, $75 000 for technicians, and $50 000 for operators.

Clean-room footprints are assumed to be 10 m^2 for any lithography or mask cleaning tool. The mask storage footprint is assumed to be 1 m^2 per 200 masks. Clean-room space costs are assumed to be $25 000/$m^2$. The clean-room life is assumed to be 16 years.

Assumed values for input parameters affecting cycle time and revenue calculations are as follows. The lost tool time to change between recipes is assumed to be 0.1 h for optical tools and zero for maskless tools. The average run size between recipe changes is assumed to be five lots for hard or medium layers performed on optical tools and four lots for easy layers performed on optical tools. The number of qualified tools available to a lot is assumed to be only one for hard layers performed on optical tools, two for medium layers performed on optical tools, five for easy layers performed on optical tools, and 50 for layers performed on maskless tools. The mean duration of a downtime event on an optical tool performing hard layers or on a maskless tool is assumed to be 2.5 h. For an optical tool performing medium or easy layers, the mean duration is assumed to be 2.0 h. The variance of the duration of a downtime event is assumed to be 6.25 for an optical tool performing a hard layer or for a maskless tool. For an optical tool performing medium or easy layers, the variance of a downtime event is assumed to be 4.0.

The die yield is assumed to be 90% and the die size is assumed to be 0.5 cm^2, regardless of lithography strategy. The die selling price is assumed to be $50 at start of the development/ramp phase, declining 50% per year.

B. Alternative Lithography Strategies Analyzed

The lithography manufacturing model was used to analyze the following six alternative strategies for 45-nm lithography, all using the same assumed parameter values listed above to assure that relative comparisons would be meaningful.

- Conventional all-optical lithography. A mix-and-match strategy is assumed, with different-cost tools applied to hard, medium, and easy layers. Each production lot is assumed limited to only one scanner at difficult layers (lot-to-lens dedication), two machines at medium layers, and five machines at easy layers. This alternative is believed to be representative of conventional semiconductor manufacturing today and provides the basis for comparison to all other schemes.
- All-optical lithography with reduced-investment masks. Under this strategy, masks for four of the same category layers (or for the same layer of four different products) are accommodated on a single mask. This strategy reduces masks investment cost but degrades lithography tool throughput and limits the maximum die size to one-quarter of the stepper or scanner field. It is included here because it is a strategy that is currently implemented by some mask users to reduce mask costs for low-volume products or product development. We assume the masked lithography tool throughput is reduced by the same factor of four.
- All-maskless lithography.
- Metal and via layers maskless, the rest optical with conventional masks. The rationale for assessing this strategy is that it has been successfully applied before in production to gate-array product structures.

[3]These figures were obtained in private communication and are based on actual tool performance at a large IC manufacturer that wishes to remain anonymous. Tool capital costs, vendor support costs, utilization limits, tool availabilities, space footprints, and recipe changeover times also reflect actual experience at that IC manufacturer. No data exist for maskless tool costs, staffing, and space requirements; the assumed figures are simply the authors' judgments.

TABLE II
45-nm NODE LITHOGRAPHY-RELATED WAFER COSTS—ALL-MASKED LITHOGRAPHY

Lithography Cost Contributor	Wafers/Mask Set = 5,000	Wafers/Mask Set = 15,000	Wafers/Mask Set = 25,000
Tool Capital	$156.25	$156.25	$156.25
Mask Cost Amortization	$524.21	$174.74	$104.84
Materials	$52.63	$52.63	$52.63
Other (incl. labor)	$18.70	$18.70	$18.70
Total Wafer Litho Cost	**$751.79**	**$402.32**	**$332.42**

- Hard layers maskless, the rest optical with conventional masks. The rationale for assessing this strategy is that it focuses application of maskless technology on the layers with the most expensive and shortest-lived masks.
- Gate definition and contact layers maskless, dual masked and maskless exposure of the poly layer, the rest optical with conventional masks. The rationale here is that it is primarily the gate definition on the poly layer that makes this layer a hard layer, so by defining the gates only using a maskless tool in a double exposure strategy, it may reduce mask costs. All layers selected for application of maskless technology for this alternative are hard layers with expensive masks yet have relatively sparse and simple patterns, enabling higher than average throughput for certain types of maskless tools, as discussed previously.

While many other possible alternatives exist, and various time-dependent schemes (such as maskless during development and masked during production) can be envisioned, it was felt that these six alternatives serve to illustrate most of the key economic issues associated with maskless lithography used for production. In all cases, it is assumed that the entire fab capacity is used for each alternative, although a more likely scenario particularly during early adoption is that the fab capacity will be split between several of the alternatives. It is felt that sufficient results from the model are presented in this paper to allow the interested reader to interpolate and address such combination strategies.

IV. THE ECONOMIC POTENTIAL FOR MASKLESS LITHOGRAPHY

A. Maskless Tool User Perspective

There are two different potential user groups for maskless lithography. One group of users typically has products with low enough volumes that once a working mask set is achieved, the entire lifetime product volume is realized from that mask set. This might be because mask replacement costs resulting from wearout or damage in production are negligible because there may be no revisions to the product design that are required and/or because there is no economic justification for yield-improving mask modifications at such low volumes. This is the user group that is usually considered when addressing cost issues related to maskless lithography. However, there is a second potential group of users whose product volumes are high and whose original working set masks may be replaced over the product life several times because of mask wearout or damage, to resolve yield issues, to address volume issues, to accommodate revisions to the product design, or for other volume-related reasons. In order to accommodate both kinds of users in our analysis, we use the parameter "wafers per mask set" that is defined as the lifetime build of a product measured in wafers divided by the total number of equivalent mask sets purchased over the life of the product. This equivalent number of mask sets is determined as the total cost of masks purchased over a product life, including all development masks and all masks subsequently purchased during production, divided by the cost of a complete mask set.

The basic issue facing all users assessing the economic advantages and disadvantages of maskless lithography is the tradeoff of investment in masks used in optical lithography versus the increased tool and clean room investments required for maskless lithography. The question is: At what point and under what conditions are mask costs high enough to render maskless lithography attractive?

1) Conventional Masked Optical Lithography Baseline: In order to address this question, we must first determine the breakout of lithography-related costs per wafer from our model for fab operation using conventional masked lithography since it is this alternative that is used as a basis of comparison for the five other lithographic alternatives considered. Table II shows the wafer lithography costs for our assumed 45-nm node scenario as calculated for tool capital, masks, materials, and other at three assumed average number of wafers processed per mask set over the product life. As defined above, these three values are the average product lifetime build in wafers divided by the equivalent number of mask sets purchased over the production life. If only one mask set is purchased, then these values are identical to the lifetime wafer build; if more than one mask set is purchased, then these values represent the corresponding fraction of the lifetime wafer build. The cost of a mask set is therefore amortized over the average number of wafers processed per mask set to determine the portion of the mask cost assigned to each wafer. Note that for the assumptions made here, the mask costs are larger than any other lithography cost component up to average wafers processed per mask set over 15 000 and are larger than all other components combined at average wafers processed per mask set below approximately 10 000. This result illustrates why there is such strong interest today in maskless lithography and why the mask cost issues are so important.

2) Lithography Alternatives Cost Comparisons: Table III shows the 45-nm node lithography cost per wafer for the various manufacturing alternatives considered, excluding the cost of masks. It is seen that using maskless for all layers increases the lithography cost compared to the conventional all-optical masked alternative by more than an order of magnitude, reflecting the strong sensitivity of this cost to tool throughput. Even for the maskless mix-and-match strategies, the lithography

TABLE III
LITHOGRAPHY COST/WAFER FOR THE SIX ALTERNATIVES, EXCLUDING MASK COSTS

Lithography Strategy	Lithography Cost/Wafer Excluding Mask Costs
All-Optical	$227.58
Reduced-investment masks	$686.76
All-Maskless	$3,179.71
Maskless hard layers	$635.79
Maskless gates/contacts, dual exposure on poly	$363.14
Maskless metal and via layers	$1,415.49

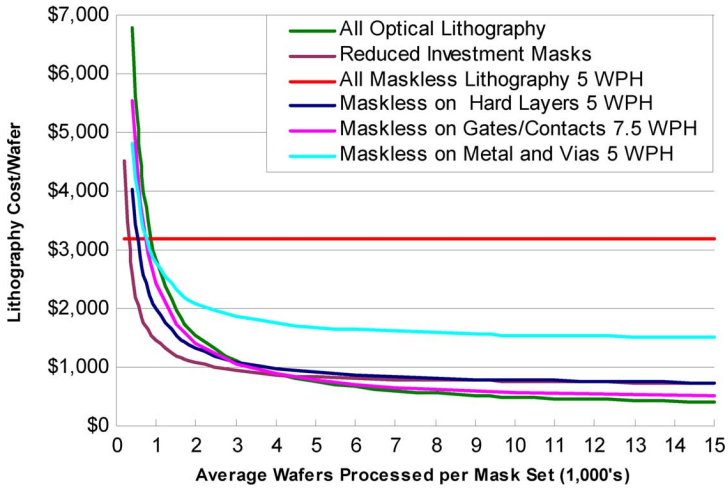

Fig. 1. Lithography cost per wafer versus average number of wafers processed per mask set.

cost is considerably increased relative to the all-optical masked alternative. It is also noted that the reduced-investment masks alternative is more than three times more expensive than the conventional optical alternative because of its impact on stepper and scanner throughputs, and more expensive than two of the four maskless alternatives.

If mask costs are included, the total lithography cost/wafer for each alternative is dependent on the number of wafers over which the mask cost is amortized and on the cost of a mask set for each alternative. This is illustrated in Fig. 1, where the lithography costs per wafer for the six alternatives are plotted against the average number of wafers processed per mask set. In most product situations of interest, the average number of wafers processed per mask set will be approximately the same for all of the optical and mix-and-match maskless alternatives, so representative comparisons of the different alternatives can be made using wafers per mask set as the variable. The maskless-on-metal-and-via-layers alternative is seen to be always more expensive than one or more of the other four maskless alternatives and is therefore the least attractive of the three maskless mix-and-match strategies considered. All-maskless lithography is less costly than conventional optical and the three maskless mix-and-match schemes only for average numbers of wafers processed per mask set less than approximately 500; for average numbers of wafers processed per mask set above approximately 4000, conventional optical lithography is always most cost-effective; for average numbers of wafers processed per mask set up to 4000, the maskless-on-hard-layers-only and the maskless-on-gates-and-contacts-only strategies are both comparable to or less expensive than the conventional optical alternative. The advantage of the reduced-investment-masks alternative is apparent in Fig. 1, as it is seen to be less expensive than all four maskless schemes as well as less than conventional optical lithography for average numbers of wafers processed per mask set between approximately 300 and 4000.

The model results for the all-maskless alternative are consistent with previously published tool cost-of-ownership analyses and confirm that the alternative likely will not be practical in routine production from a user perspective except for very low-volume products unless maskless tool throughput is significantly improved beyond the assumed 5 WPH. However, the model results for the two mix-and-match alternatives, maskless on difficult layers only and maskless for gates and contacts, and suggest that these alternatives might be surprisingly cost-effective at the 45-nm node compared to conventional masked optical production for average numbers of wafers processed per mask set requirements up to 4000. Given that many products require multiple mask sets before getting an acceptable working mask set, the maskless mix-and-match alternatives may offer more cost-effective manufacturing for a large fraction of the semiconductor devices produced by the industry, even products that have lifetime wafer builds well in excess of 4000 wafers. If the cost and complexity of difficult layer masks continues to increase as projected, such mix-and-match maskless schemes are likely to become increasingly attractive to users.

3) Cycle Time Considerations: Across recent technology nodes, it has been commonplace in the fabrication of many advanced digital products to practice lot-to-lens dedication on hard layers and to restrict tools for medium layers to only a few. This has resulted in longer lithography cycle times than

in previous nodes with more flexible routing. As set forth in Section III-A, we assume for the conventional masked lithography alternative that there is only one qualified machine at hard layers, two at medium layers, and five at easy layers. We further assume the average recipe batch size is 75 wafers at all masked layers and 25 wafers for all maskless layers. Setup time for recipe changes is assumed to be 6 min for masked layers and none for maskless layers.

It is believed to be technically feasible for maskless tools to be calibrated to one another such that any lot can be routed to any tool with no yield impact. For this assumption, the cycle time penalty associated with the slow processing rate of the maskless lithography tools is offset by the flexibility to route lots to more alternative tools and by the smaller batch size. For the standard 25-wafer lot size, the increases (decreases) in total photolithography cycle time (relative to the model-estimated 7.4 days for conventional all-optical lithography) are estimated using the queuing formulas described previously as follows:

— 46.7% for the all-maskless alternative;
— (8.9%) for the maskless-on-hard-layers-only alternative;
— (9.5%) for the maskless-on-gates-and-contacts/dual masking-at-poly alternative;
— 15.7% for the maskless-on-metals-and-vias alternative.

In the case of a 13-wafer lot size, the increases (decreases) in total photolithography cycle time (relative to the model-estimated 6.8 days for conventional all-optical lithography) are estimated as follows:

— (10.2%) for the all-maskless alternative;
— (17.6%) for the maskless-on-hard-layers-only alternative;
— (12.6%) for the maskless-on-gates-and-contacts/dual masking-at-poly alternative;
— (6.8%) for the maskless-on-metals-and-vias alternative.

Considering the slow speed of maskless tools, it seems likely that coat/develop tools would need to be stand-alone, as opposed to linked to exposure tools as they are in the case of optical lithography. Separation of coat/develop and exposure steps is likely to add lithography cycle time. Thus the promising cycle times for the alternatives involving selective application of flexible maskless lithography tools must be tempered by the prospect of decoupling coat/develop tools.

If maskless tools cannot be sufficiently calibrated to one another to avoid lot-to-tool dedication, then assuming the same numbers of qualified tools for various layers as in the all-optical case lithography cycle time would be increased by maskless alternatives as follows in the case of a standard 25-wafer lot size:

— 537.5% for the all-maskless alternative;
— 171.6% for the maskless-on-hard-layers-only alternative;
— 45.9% for the maskless-on-gates/contacts/poly alternative;
— 236.4% for the maskless-on-metals-and-vias alternative.

In the case of a 13-wafer lot size and lot-to-maskless-tool dedication, the increase in lithography cycle time by maskless alternatives is as follows:

— 288.1% for the all-maskless alternative;
— 92.1% for the maskless-on-hard-layers-only alternative;
— 22.1% for the maskless-on-gates/contacts/poly alternative;
— 127.3% for the maskless-on-metals-and-vias alternative.

For all maskless alternatives except the maskless-on-gate/contacts/poly alternative, the figures portray substantial and possibly prohibitive increases in manufacturing cycle time. For the maskless-on-gates/contacts/poly alternative, lithography cycle time penalty is almost 50% in the case of conventional 25-wafer lots. It would seem, then, that the ability to calibrate maskless tools to one another sufficiently to eliminate the need for lot-to-tool dedication is an important requirement for successful application of the technology to semiconductor manufacturing.

In the case of standard 25-wafer lots, the lithography cycle time for the reduced-investment-masks approach is found to be about 3.4 times that for conventional all-optical lithography (i.e., about 18 days longer than cycle time when using conventional masks). In the case of half-size 13-wafer lots, the lithography cycle time for the reduced-investment-masks approach is about 3.3 times that for conventional all-optical lithography (i.e., about 16 days longer than cycle time when using conventional masks). These increases reflect the much lower throughput of the optical tools for this technique.[4] As a result, it is important for users of this strategy to weigh the previously described cost advantages at total average number of wafers processed per mask sets less than 4000 wafers against this increased manufacturing cycle time.

It is also important to point out that the time it takes for a user to obtain hard-layer masks from mask vendors may be quite long, particularly during the early stages of a new semiconductor process node. As a result, the two maskless mix-and-match alternatives that focus on hard layers may provide significant reduction in new product development time. The corresponding product time-to-market improvement needs to be considered in any cost assessment of the different lithography alternatives.

4) Sensitivity Analysis: The fab and tool parameters that have been assumed, while believed to be representative for the 45-nm node, are likely to be different in detail from those applicable to a particular user. As a result we provide here a discussion of the sensitivity of the model results to some of the more critical parameters. One of the more commonly used measures of a maskless lithography approach is the break-even average number of wafers processed per mask-set-equivalent purchased. This is the average number of wafers processed per complete mask set equivalent at which the lithography cost per die for the maskless approach is equal to that for the conventional all-optical approach. At higher average numbers of wafers processed per mask set, the all-optical masked approach is less expensive; at lower average numbers of wafers processed per mask set, the maskless alternative is less expensive. Note that by defining this metric in terms of cost per die rather than cost per wafer, the effect of differences in die yield and size is inherently included. This measure will be used as the basis for the sensitivity analysis discussion.

One sensitivity of this break-even average number of wafers processed per mask set that is of interest is its dependence on hard layer mask cost. Fig. 2 shows this dependence for the two most promising maskless alternatives: maskless on hard layers only and maskless on gates and contacts with dual exposure on

[4]These figures are the cycle times when the reduced-investment-mask strategy is applied to all products of the fab. If the strategy is applied to only a small portion of the portfolio of products in the fab, the cycle time for the reduced-investment-mask products would not be so large.

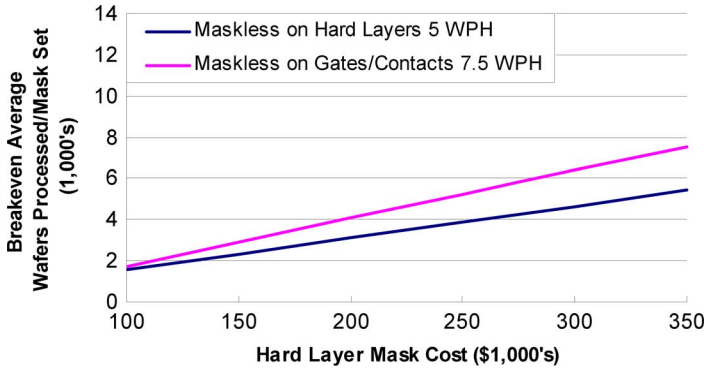

Fig. 2. Breakeven wafers per mask set versus hard-layer mask cost for the two most promising maskless alternatives.

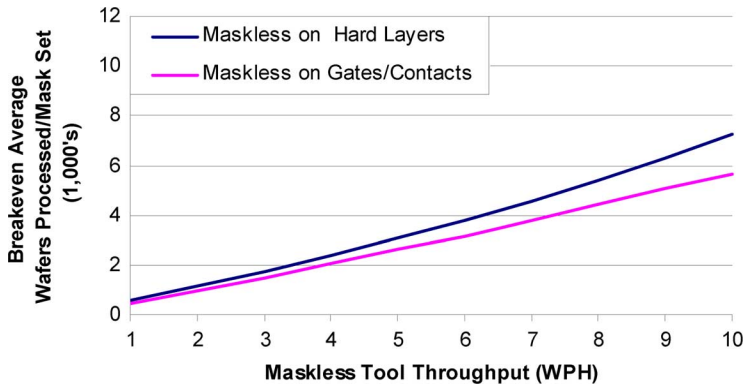

Fig. 3. Breakeven wafers per mask set versus maskless tool throughput for the two most promising maskless alternatives.

poly. As may be seen, the break-even average number of wafers processed per mask set at which application of maskless tools become more cost-effective ranges approximately linearly from 1700 when difficult-layer masks cost $100 000 to approximately 7 500 when they cost $350 000 for the former maskless alternative, and from 1 700 when difficult-layer masks cost $100 000 to over 5000 when they cost $350 000 for the latter maskless alternative.

Another sensitivity of interest is the dependence of the break-even average number of wafers processed per mask set on maskless tool throughput. Fig. 3 shows this dependence, again for the two most promising maskless alternatives. The breakeven average number of wafers processed per mask set is very similar for both at all throughput values. Both are found to be nearly linear with maskless tool throughput, increasing from approximately 1000 wafers per mask set when throughput is 2 WPH to approximately 3000 when maskless tool throughput reaches 5 WPH and approximately 6000 when maskless tool throughput reaches 10 WPH. As mentioned previously, it should be possible for tool manufacturers to achieve higher throughputs for a maskless tool designed only to expose gates and contacts than for a maskless tool designed to expose arbitrary patterns at any given maskless technology generation, so the gates and contacts alternative may be more attractive at all maskless tool technology generations for this reason.

Since it is expected that die yield will be different for maskless alternatives than for masked alternatives, it is also of interest to examine the sensitivity of the break-even average number of wafers processed per mask set to die yield. In all of the other figures and analysis provided in this paper, it is assumed that yield is independent of the lithography strategy selected. However, in Fig. 4, potential differences in yield for maskless alternatives from the nominal value of 90% achieved by the conventional optical alternative are considered. The change in die yield shown in the figure is the percentage change from the nominal, either better (positive) or worse (negative). The analysis indicates that the break-even value for the maskless-on-gates-and-contacts alternative is very sensitive to yield changes, changing by approximately a factor of two when yields change by 10%. This is a reflection of the fact that this alternative replaces fewer hard layer masks than the maskless-on-hard-layers-only alternative. The maskless-on-hard-layers-only alternative is less sensitive to yield changes, with a given percentage change in yielding die per wafer resulting in approximately three times that percentage change in break-even average number of wafers processed per mask set.

5) Tool Requirements, Clean Room Space, and Investment Cost: Table IV summarizes the counts of lithography tools for the six alternative strategies required for the assumed scenario described in Section III.A. As may be seen, tool counts for configuring a fab to fully implement one of the alternatives to conventional lithography range from 1.6 to 13 times and tool investment cost ranges from 1.8 to 20 times the values for conventional optical lithography. Even if the all-maskless and the maskless-on-metal-and-via-layers alternatives were economically attractive, it would be a formidable challenge to build a fabrication facility large enough to accommodate and utilize effectively all of the tools required. The other two mask-

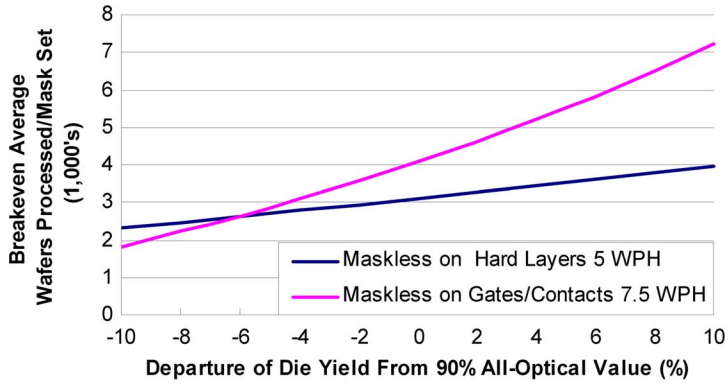

Fig. 4. Breakeven wafers per mask set versus die yield for the two most promising maskless alternatives.

TABLE IV
LITHOGRAPHY TOOLING REQUIREMENTS

Lithography Strategy	No. of Photo Tools	No. of Mask Cleaning Tools	Total Tool Capital ($B)
All-Optical	45	5	0.6
Reduced-investment masks	171	5	2.2
All-Maskless	574	0	11.5
Maskless hard layers	124	3	2.1
Maskless gates/contacts, dual exp. on poly	72	4	1.1
Maskless metal and via layers	258	3	5.0

less alternatives, maskless on hard layers and maskless on gates and contacts, require fewer total tools than a fab configured for reduced-investment-mask operation, but still considerably more than required by an all-optical fab. However, it is noted that the capital investment required for both these maskless alternatives is less than that for the reduced-investment-mask alternative. Similarly, the clean-room space required, assuming clean-room space scales with the number of photo tools, is greater for the reduced-investment-mask alternative. In all cases, implementation of any one of these schemes will involve a major change in fab layout and either a significant increase in total clean-room space to maintain the assumed wafer processing capability or a reduction in fab processing capacity.

Even if the financial analysis of a maskless implementation from a cost perspective is attractive, there are a number of important issues relating to manufacturing insertion that need to be resolved. The necessity for verifying that the yield of the maskless implementation is acceptable has already been pointed out. Several other important considerations relate to the fact that all of the more attractive ML implementations will involve a mix-and-match strategy with conventional optical steppers. This will necessitate, for example, that both optical and ML tool resist processing capability will be required in the fab; lithography tool compatibility issues such as alignment marks and alignment techniques will need to be addressed; wafer WIP tracking and the management of masks with the appropriate pattern files used for the maskless layers will have to be modified; resist coat and develop systems will need to be shared among a number of maskless tools because of the much lower throughput of each tool; machine-to-machine matching issues need to be resolved; and procedures will be needed to be put in place to protect the integrity of the maskless tool layer pattern data in the production environment.

While these manufacturing insertion issues appear daunting, it needs to be remembered that the comparisons of different lithographic alternatives assume that a viable masked alternative exists for the particular semiconductor process node of interest. If such an alternative is either too expensive or it is no longer available, but maskless tools that will meet the needs on the difficult layers are available, then one of the ML strategies described here will need to be considered despite the challenges of the manufacturing insertion issues that need to be addressed.

If the maskless-only-on-difficult-layers strategy is adopted, there are some other advantages that relate to new process and product development. First, the cost of a mask set will be significantly reduced because the very expensive difficult layers are not required. Secondly, the maskless tools have the capability to easily print different patterns at every die site on any wafer. This capability will, for example, increase the process engineering options available for design of experiments, and thus may enable more rapid development of new processes and more rapid yield enhancement.

6) Maskless Lithography Potential for High-Volume Users: Lithography tool users that produce high-volume products have not usually been considered as potential candidates for maskless tools. However, with the increasing cost of masks, the mask cost contribution to total manufacturing costs of such products has become an increasing factor. While maskless lithography has typically been ignored as a potential approach to addressing this issue because of its low throughput, the results provided here suggest that some manufacturing implementation schemes that incorporate maskless tools may provide economic advantage at maskless tool throughputs of five wafers per hour or less. Such a conclusion depends strongly on the mask use experience of such high-volume users with all-masked lithography as measured by the number of wafers processed per equivalent mask set. For ex-

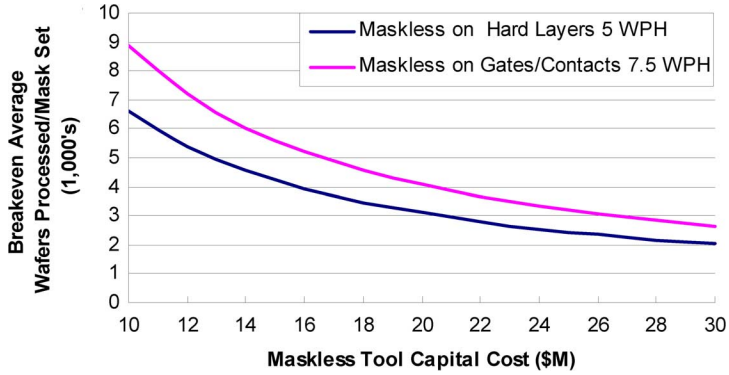

Fig. 5. Break-even wafers per mask set versus maskless tool capital cost for the two most promising maskless alternatives.

ample, if a high-volume product required 100 000 wafers over its life and the mask purchases over this period (including development masks, full- and partial-mask set modifications for yield improvement, mask sets for additional production capacity or for spares, mask breakage, mask wearout, etc.) added up to a cost equivalent to that of ten complete mask sets, then the number of wafers produced per mask set that should be used for the cost model and for interpreting the figures and tables in this paper is 10 000.

B. Maskless Tool Supplier Perspective

There are currently no maskless lithography tools available for semiconductor manufacturing applications from any supplier with throughputs in excess of five WPH. There are very low throughput electron beam systems available, but these are primarily used only for research and development. Over the past 30 or more years, many companies have attempted to develop maskless tools for semiconductor manufacturing. However, optical technology has continually been able to be extended far beyond its projected limitations and optical tool cost effectiveness has continually increased substantially. Maskless tools have been unable to compete on a cost-of-ownership basis, and there was no technical failing of optical tools that would drive the industry to look for an alternative. As a result, there has been little interest from tool suppliers to develop and market a production ML tool. Recently, a combination of factors driven primarily by high mask costs has led to increased interest in maskless tools. The analysis provided here illustrates why this is the case, and why there may now be a financially attractive opportunity for maskless lithography tools.

Given a viable technology approach that can result in a maskless system with throughput capability of approximately five wafers per hour or more, the cost to develop and bring to market such a tool would be substantial, perhaps in excess of $100 million. This cost would need to be weighed against the expected sales volumes and unit prices (and associated gross margins) that could be expected. Based on the analysis provided here, the number of tools demanded could be sizeable even if only one large-volume customer committed to one of the mix-and-match strategies. This one customer's tool requirements might be 100 or more systems. In fact, given broad industry acceptance of maskless strategies, the potential market for such a tool could become larger in units than that of optical masked lithography systems. Fig. 5 displays the sensitivity of the breakeven average number of wafers processed per mask set to the capital cost of the ML tool over the range from $10 to $30 million for the two most promising maskless alternatives. Depending on what this average number of wafers processed per mask set is for a given semiconductor company, the price point for an acceptable tool with our assumed performance capabilities can be estimated from the figure.

Even if the ML tool development costs, volumes, and prices are considered promising, there are a number of other tool supplier issues that need to be considered. The supplier would need to be able to ramp manufacturing quickly to rather large system volumes to meet the timeliness requirements of even one potential user and would have to put in place an ongoing development program to upgrade the maskless tool to match the semiconductor industry roadmap needs over time. The former will involve considerable additional investment, and the latter will require a long-term commitment to the product line with its associated ongoing investment by the supplier.

V. Discussion and Conclusion

In order to illustrate the important economic issues associated with maskless lithography, the analysis of a specific 300-mm fab facility running a 45-nm process has been described in this paper based on a set of assumed operational parameters believed to be indicative of manufacturing at this semiconductor node. However, it is recognized that different users and potential users may have quite different facilities manufacturing under operational parameters that are different from those assumed here. As a result the authors have also examined a number of different fab facility alternatives under a variety of assumed parameters using the model. The discussion and conclusions presented here are based on a compilation of these analyses.

The wafer manufacturing cost comparison of different lithography alternatives to conventional all-optical lithography (other than all maskless lithography) centers around one key variable, the average number of production wafers processed over a product life per equivalent complete mask set purchased. The equivalent number of complete mask sets is calculated as the total mask purchases for the conventional all-optical alternative, including all development masks and masks purchased for production, over the product's life divided by the average cost of a complete set of masks for the all-optical alternative.

This variable allows the potential maskless tool user, whether a high-volume or low-volume product manufacturer, to conveniently assess the relative cost advantages and disadvantages of maskless lithography alternatives as they apply to his or her particular business. Using this variable, at a maskless tool throughput of 5 WPH at the 45-nm node, it is found for the example provided here that all-optical lithography is most cost-effective when the average number of wafers per mask set is greater than approximately 4000; all-maskless lithography is most cost-effective when the average number of wafers per mask set is less than 500; and one or both of the maskless-on-hard-layers and maskless-on-gates-and-contacts-only alternatives are more cost effective when the average number of wafers per mask set is between these values. Analyses of different fab configurations and assumed operational parameters suggest that the cost-effectiveness range of all-maskless 45-nm lithography for 5 WPH tools is relatively insensitive to assumptions and is constrained to wafers-per-mask-set values less than approximately 600 for a broad range of assumed conditions. However, these same analyses suggest that one or both of the maskless-on-hard-layers and maskless-on-gates-and-contacts-only alternatives, at the tool throughput values assumed here, are more cost-effective than the conventional all-optical alternative at wafers-per-mask-set values up to at least 2500 and sometimes up to as high as 10 000 over the same broad range of assumed conditions.

The cost conclusions for all-maskless lithography, consistent with previous analyses, show that this alternative is unlikely to be practical in semiconductor device production unless significant improvements in tool throughput beyond the 5 WPH assumed are achieved. In fact, the wafer processing cost excluding the cost of the masks is more than ten times more expensive as compared to a conventional all-masked process at the 45-nm node. However, a lithography manufacturing strategy in which some or all of the hard layers use maskless tools and the remaining layers use conventional masked tools may provide considerable cost savings for many applications. If average wafers per mask set is larger than 2500, such alternatives may not only be more cost-effective for production; they may also have other advantages. For example, mask set costs will be lower and maskless will allow more rapid and less expensive layout changes on critical layers, advantages of some significance given that harder layers have the most expensive masks and often such masks have the shortest life.

While not a focus of this paper, it is interesting to note that the reduced-investment-masks alternative for the example analyzed here is more cost effective than any other alternative between 300 wafers per mask set and approximately 4000 wafers per mask set. However, its broad application in a production line will lead to about 18-day increases in wafer manufacturing cycle time (16-day increases in the case of half-size 13-wafer lots) if the fab practices lot-to-lens dedication. As a result, this alternative may be viable only when it is used for a fraction of the total wafers manufactured so that impact on cycle time will be minimal.

The break-even number of wafers processed per mask set, while an important metric for assessing the potential of maskless lithography in production, addresses only the cost issues of the alternative lithography strategies. Cycle time and revenue issues also are important. In particular, competitive manufacturing cycle times will require the calibration of maskless tools to be such that lot-to-tool dedication is unnecessary and manufacturing lots may be flexibly routed to any maskless tool. Assuming that is the case, maskless lithography can be expected to positively impact revenue-related aspects of semiconductor operations. Reduced new product/process development time could also lead to both improved revenue and improved market share for a semiconductor company. Easier to quantify will be the impact on manufacturing yield. If the fab is production-limited, a given percentage change in die yield will result in an identical percentage change in fab revenue, all of which will contribute directly to profitability since operating costs will not have changed. It is evident, therefore, that the financial attractiveness of maskless lithography may be as strongly dependent on its impact on the number of good die per wafer as it is on lithography cost per wafer.

Any of the mix-and-match strategies using maskless tools will involve both a major capital expense outlay and a considerable increase in clean-room lithography space if a fab implements the strategy for all wafers processed. Because of the aforementioned uncertainty in yield impact as well as these cost considerations, fabs choosing to implement a maskless strategy might be expected to start by running only a fraction of their total wafer capacity on the maskless alternative while running the majority of their wafers on a fully masked process. Expanded maskless processing could then be added as financially justified. Such an approach would allow the fabs to validate the potential cost savings and yield impact for their particular processes and product mix without requiring the major commitment involved in total conversion from the outset.

No major semiconductor manufacturer currently implements maskless lithography in production, and a production maskless tool with throughput at or higher than 5 WPH is not yet commercially available. However, the analysis provided here suggests that at and beyond the 45-nm node, maskless lithography (even at lower throughput values) may be a very financially attractive manufacturing strategy for semiconductor companies from a cost perspective even if fully masked alternative approaches are available. In particular, if mask costs continue to escalate as they have in the past few semiconductor generations, there will be increasing motivation for semiconductor tool suppliers to develop such tools and for semiconductor companies to use them in production. In addition, if it is found that the number of good die per wafer can be increased using maskless lithography, through either improved yield or design rules that allow die size reduction, then maskless lithography may finally find a major role in mainstream semiconductor manufacturing.

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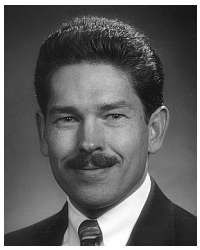

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