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Process costing of microchip

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ABSTRACT

Process Costing of Microchip

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The CMOS microchip is the workhorse of the semiconductor industry. An estimated price of a CMOS chip for an 8” wafer was stated as $1.65/chip (65). The manufacturing model was formed with practical processing times, number of machines, steps of manufacturing process, labor required, construction costs, land costs, etc as input parameters. This cost model attempts to analyze costs and calculate the cost per chip. Different sections of costs have been individually analyzed in turn to reflect their impact on the finished product. A simulation model has been run to reflect an actual semiconductor manufacturing scenario. Simulation model is also used to estimate labor required for the process.

The cost was calculated based on yield, number of chips/wafer and total expenditure by the fab. A simulation model was created in Arena 6.0 professional version, which allows the user to make changes to the model to reflect the changes in the fab. The calculated cost of the model for a CMOS chip was obtained as $0.75/chip.

ACKNOWLEDGEMENT

I would like to sincerely thank my advisor Dr. B. Gopalakrishnan without whose continued support, invariable supervision and encouragement, this research work would not have been completed. I also wish to thank my committee members Dr. R. Creese and Dr. D. Korakakis for their advice and support. A special word of thanks goes to my family and friends who made this possible.

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1.0 Introduction

The invention of the transistor at AT&T Bell Labs, in 1947, gave birth to the semiconductor industry. The first important event in the growth of the semiconductor industry was the Integrated Circuit (IC), which was invented in the 1960's and resulted in extensive research in the industry. Its effect was so huge that it has made it possible to integrate a billion components onto a single piece of silicon having an area of one square centimeter today. In the beginning ICs were used in only a limited number of applications, but as the technology grew, it gradually found use in many small day-to-day applications.

The semiconductor industry accounts for 150-200 billion dollars of the total one trillion dollars earned from sales turnover by the electronics industry. The semiconductor industry is growing and plays a large part in the electronics industry because of progress in technology. Improving technology has made it possible to continuously increase semiconductor performance and decrease price.

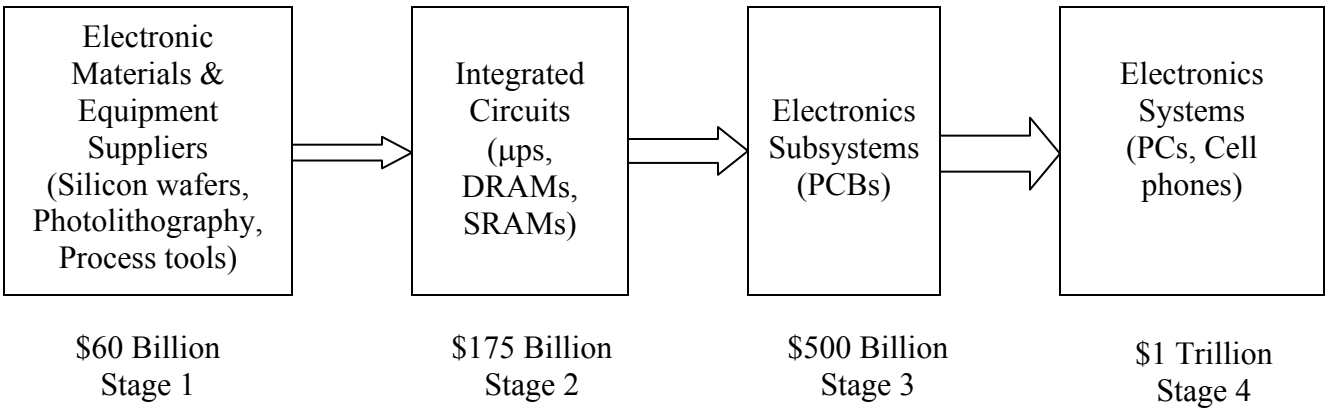


Figure 1: Sales at different stages in the electronics industry (49)

The total worth of the world's electronics industry in 2001 is shown in figure 1 (49). At the extreme right of figure 1 is the end-product electronic systems sold to the final customers. The end product levels are fed by electronic subsystems consisting of printed circuit boards (PCBs), which are an integral part of every electronic product. The worth of all the printed circuit boards produced in 2001 was about $500 billion. Integrated circuits, integrated on the printed circuit boards at the next stage, are worth about $175 billion. The

last stage consists of companies, which supply the equipment and materials used to manufacture ICs. The sales of these supplies on the last stage were around $60 billion in 2001 (49).

1.1 Semiconductor Industry

Infrastructure (supporting companies and institution) of the semiconductor industry is shown in figure 2. The semiconductor industry consists of many groups of companies and institutions, all of which contribute according to their strengths. Most important of them are chip manufacturers supported by outside organizations, including the manufacturers of chip-processing and metrology tools, suppliers of materials and chemicals, analytical laboratories, industry associations, that provide highest manufacturing standards and manage co-operative research efforts**.** Colleges and universities usually provide technically skilled and trained workers. These groups are referred to as inputs to the chip manufactures in figure 2 (49).

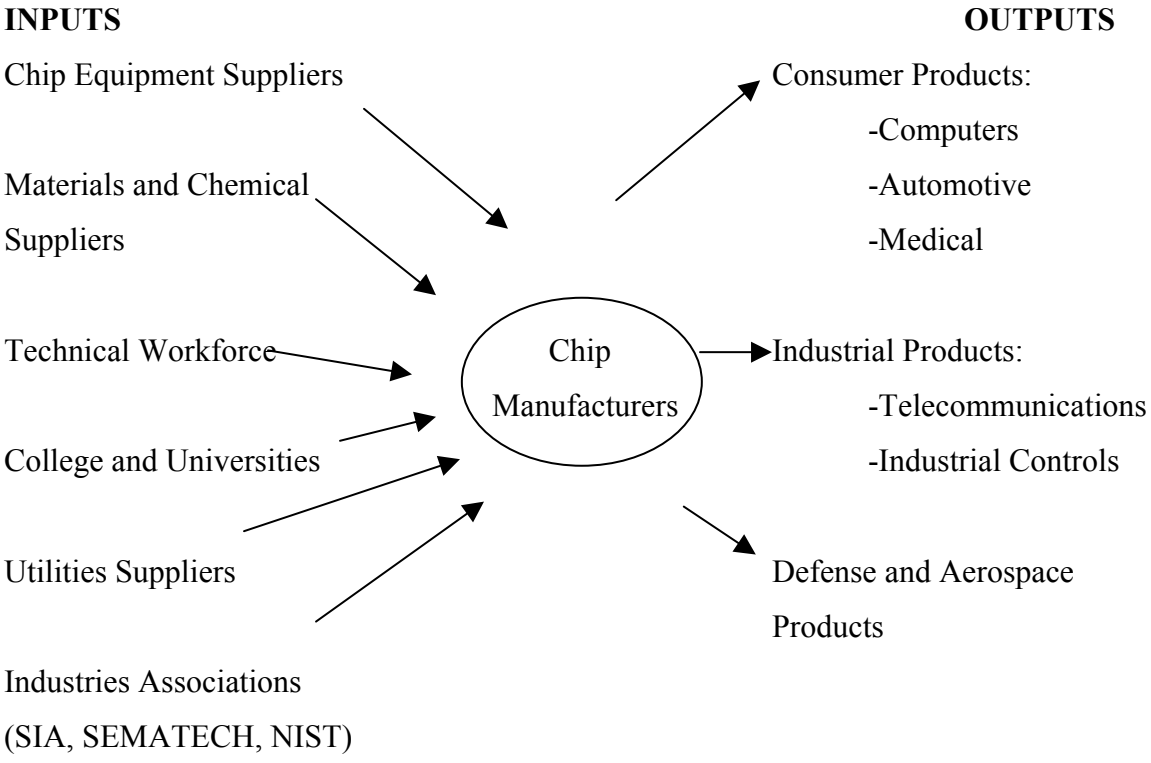


Figure 2: Infrastructure of the semiconductor industry (49)

The chip manufacturers are suppliers/vendors to other customers in many groups including automotive electronics, computers, communications electronics, medical instrumentation and industrial electronics. These groups are connected through the intermediary levels of the printed circuit board (PCB) manufacturers and other final system assemblies. These groups are referred to as outputs of the chip manufacturers in the figure 2 (49).

1.2 History of the Semiconductor Industry

Bell Labs invented a transistor on December 23, 1947. Its first commercial use was in products for the hearing impaired. Bell Labs grew a single germanium crystal, offering more uniform electrical conduction and fewer defects. The grown junction transistor became the first devise with enough predictability and dependability to be used in a range of consumer goods. In 1951, Univac delivered a computer to the Census Bureau. In 1952, Texas instruments (TI) entered the semiconductor business. Motorola established a solid-state electronics R&D lab in Phoenix to capitalize on the recent inventions of the transistor. At the same time IBM unveiled the 701, the first computer to store electronic programs. Simultaneously Motorola applied for its first semiconductor related patent to develop low cost transistors for audio power stages of radio communication receivers and auto radios (35, 49).

In 1955, Bells Labs introduced Photolithography, a technique still used today to mass produce batches of identical circuits. "Explorer," the first U.S. orbiting satellite, used transistor technology. Fairchild Semiconductor became the first company to work exclusively with silicon. The semiconductor industry surpassed $100 million in sales for the first time. Cray introduced an all-transistor supercomputer. Texas Instruments' Jack Kilby demonstrated a first integrated circuit (IC). U.S. Air Force incorporated semiconductors in Minutemen Missile design. The Pentagon and NASA quickly became two of the industry's major customers (35, 49).

In 1959, National Semiconductor opened in Danbury, Connecticut. Fairchild Semiconductor's Robert Noyce commercialized the process for making ICs. Digital Equipment Corp. produced the first mini-computer named PDP-1. AT&T invented the first modem. In 1965, Gordon Moore predicted exponential growth (biannual doubling) in chip power. It was later known as "Moore's Law." In 1967, Intel invented SRAM and EPROM and introduced microprocessors, which enabled the "brains" of a computer to be on one chip for the first time. Shortly Intel introduced the 4004; TI introduced a single-chip microprocessor. Alan Shugart of IBM invented the floppy disk. Hewlett-Packard introduced the first scientific pocket calculator, which put slide rule manufacturers out of business. The UPC symbol became ubiquitous. Motorola introduced the portable cellular, radiotelephone, and the precursor to the modem cell phone. In 1975 Altair, the first personal computer was on the market. Bill Gates and Paul Allen launched Microsoft (35, 49).

In 1979, Motorola introduced a16-bit microprocessor. Apple Computer adopted its two-million-calculations-per-second capability for its Macintosh PCs. Bell Labs introduced a single-chip digital signal processor, which performed speech compression, filtering, error corrections and other functions much faster and better than multiple chips. The semiconductor industry surpassed $10 billion in sales turnover. Motorola's first cellular phone was launched. In 1992, Microsoft introduced Windows 3.1. IBM and Motorola introduced a RISC chip for PCs. Harris Corp. introduced Monster Power ICs (MCT), which helped motorized products from refrigerators to jet fighters function more efficiently (35, 49).

In 1996, U.S. fabrication facility growth exploded, as chips became increasingly prevalent in new consumer products. High-end chips made computer networking, telephone communications and internet connections faster and smarter. U.S. and Japan approved a new trade agreement on semiconductors as foreign share in Japan approached 30 percent. Agreement calls were made for the establishment of the World Semiconductor Council (WSC). AT&T spun off Lucent, the portion of the telephone giant once known as Bell Labs. In 2000, worldwide semiconductor sales exceeded $200 billion for the first time in semiconductor history. The semiconductor industry was recognized by the US Bureau of

Labor and ranked 2nd in the nation for the lowest injury and illness rate out of 208 durable goods manufacturing industries (35, 49).

1.3 World Capital spending scenario

From January 2002 there has been in an upsurge in the semiconductor industry, which has lasted more than two years (11). The upsurge is measured by increase in spending and increase in capacity. The common methodology is to compare the current growth rates of both capacity and spending with previous periods of expansion. Since January 2002, when chip sales started to move up, the ratio of equipment spending to chip sales stayed beneath 15% at very low levels. This was because until the beginning of 2004 the industry did not believe in the recovery. As recently as the third quarter of last year, industry leaders while reporting increased sales also expressed uncertainty about the direction of the world economy and the strength of end markets driving their sales.

A brief look at the ratio of equipment spending to chip sales is shown in figure 3 (11). During previous recoveries this ratio peaked to near the 25% level. As of March 2004 the ratio was at 18% and rapidly rising.

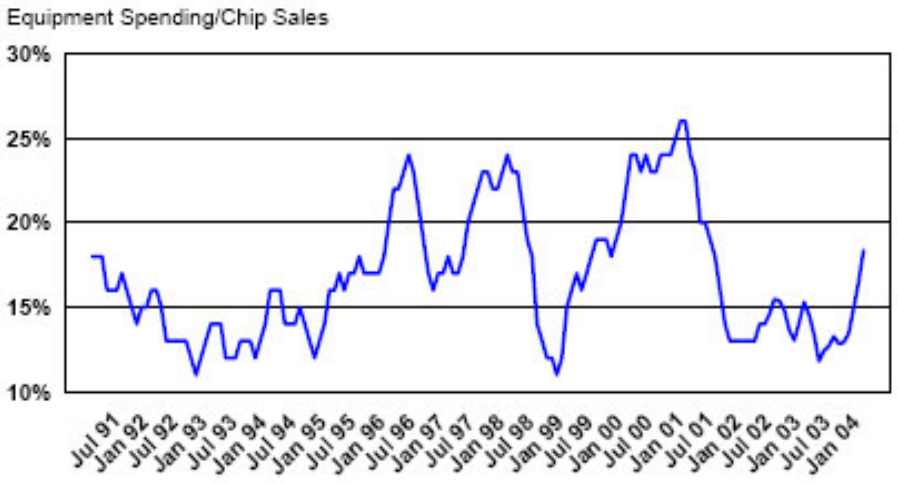


Figure 3: Ratio of equipment spending to chip sales (11)

The uncertainty resulted in low capital spending through most of fiscal year 2003. Thus as of June 2003, equipment spending was only 10 percent higher than its cyclical low while chip sales were 25 percent higher. However, since summer of 2003 and particularly since the first of fiscal year 2004, equipment sales have increased rapidly. The most recent industry statistics show that equipment sales are 33 percent below their peak in 2000 and chip sales are just 13 percent off their peak (see figure 4 below). Given the still low ratio of equipment sales to chip sales, the relatively small gains in spending compared to previous expansions and the reported high levels of capacity utilization, it does not appear that the current growth in spending is nearing its end.

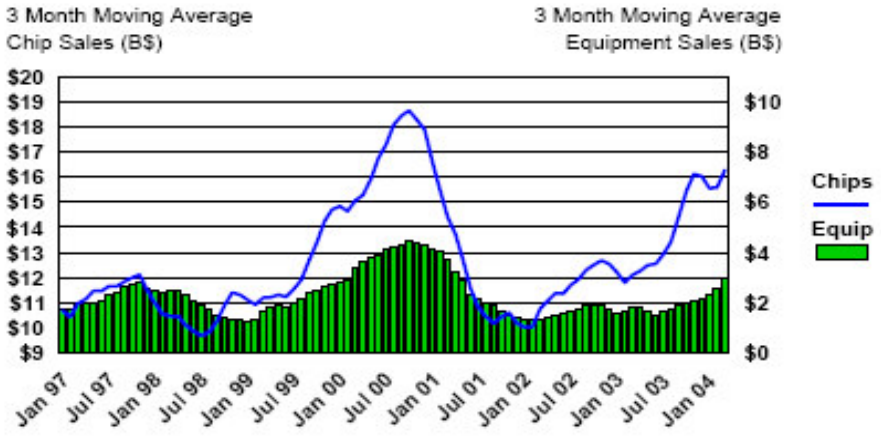


Figure 4: Chip sales and equipment sales over a period (11)

The industry had brought twenty new fabs online by end of 2004. The total capacity of these fabs is almost 600,000**,** equivalent to 200mm wafers a month (see figure 5) (11). Only eight of these twenty fabs will be 300mm fabs, but the capacity of these eight 300mm fabs is almost 500,000, equivalent to 200mm wafers, or about 82 percent of the total. By the end of year 2005, the semiconductor industry was expecting 20 more new fabs around the world with even more capacity, more than 700,000, equivalent to 200 mm wafers. Most of these fabs would be running on 300 mm wafers.

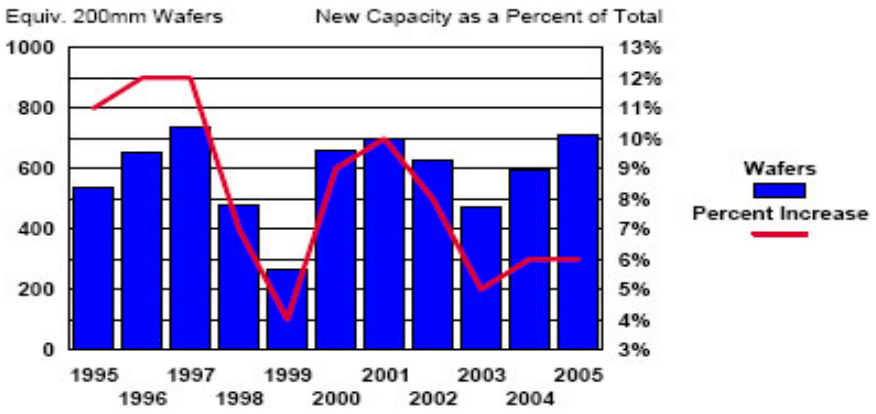


Figure 5: Capacities added over years in different fabs (11)

In 1998, US (ex-Intel) outspent all other regional companies. In 2004 their share was far behind the Japanese companies and at about the same level as Taiwan, South Korea, China and Southeast Asian companies. The main reason for this slide was outsourcing of a large share of the capacity of US companies to the foundries. In terms of the percentage increase in capital spending by regionally based companies for fiscal year 2004, Asia Pacific companies increased their spending to 88% in 2004 to $19.3 billion, almost as much as Japan and the US combined (table 1) (66). Taiwan and South Korea was the top spending countries within Asia Pacific at $6.3 billion and $6.2 billion respectively. This is slightly higher than the total spending by all US companies, except Intel. Spending by Chinese companies grew to 100% this year, from $2.3 billion to $4.6 billion. Southeast Asian companies increased their spending to 143%, the biggest percentage increase by any regional grouping of companies. Spending by European companies grew to 31%, $3.7 billion and Japanese companies to 48%, $10.3 billion.

Table 1: Capital spending by regional companies billions $/percent change from previous year (66)

	2003	2004
Asia - Pacific	$10.2/0%	$19.3/88%
China	$2.3/8%	$4.6/103%
Malaysia	$0.2/-40%	$0.3/37%
Singapore	$0.7/-51%	$1.8/176%
South Korea	%4.2/61%	$6.2/48%
Taiwan	$3.0/-23%	$6.4/115%
Europe & Mid East	$2.8/12%	$3.9/38%
Japan	$7.2/38%	$10.3/49%
US	$9.3/-12%	$10.2/11%
Total	$29.6/3%	$43.8/49%

Japan spent more than any other country, although it was less than what was spent by several Asia Pacific countries together. US showed the smallest percentage gain in spending: 11%. Spending by Korean companies rose to 48%, from $4.2 billion to $6.2 billion, in 2004. Taiwan spent more than double in 2004, increasing to 114%. Singapore will nearly triple its spending, increasing by 176 percent to $1.85 billion. Malaysia will up its spending in excess of 37% to $282 million, when compared to its spending in 2003.

Semiconductor industry expects that 14 new fabs will open between April 2004 and the end of Q1 in 2005. The list of different fabs opening around the globe is given in table 2 below (66). The value of these fab openings is about $14.2 billion. The long awaited return to growth in equipment sales is clearly underway and the semiconductor industry may have entered the next boom in fab construction.

Table 2: New fab openings in 2005 (66)

Company	Location	Product	Cost ($M)/Capacity (wpm)/Wafer size
Inotera/Fab III	Kueishan, Taiwan	DRAM	$2200/54000/300mm
Intel/Fab 24	Leixlip, Ireland	MPU	$2100/30000/300mm
Keysi-STL/Fab 1	Shenyand, China	Discrete	$77/6000/150mm
Maxim Integrated Prod	San Antonio, Texas, US	Logic	$60/20000/200mm
MEMSIC	Wuxi, China	MEMS	$100/1000/150mm
Prima/Fab 1	Changzhou, China	Fab	$450/20000/200mm
SinoMOS/Fab 1	Ningbo, China	Fab	$110/30000/150mm
SMIC Fab 4	Beijing, China	Fab	$3500/45000/300mm
Song/Fab 2	Nagasaki, Japan	MPU	$1670/17000/300mm
Toshiba/N/A	Oita, Japan	Logic	$1850/12500/300mm
TSMC/Fab 14	Tainan, Taiwan	Fab	$1600/35000/300mm
UEC	Hsinchu, Taiwan	Opto	$NA/450/150mm
Ultimate Fab 1	Shanghai, China	Fab	$230/27000/150mm
University of New York	Albany, New York, US	R&D-Pilot	$300/500/300mm

1.4 Semiconductor industries and its Cost

The semiconductor industry is the groundwork/base for the trillion-dollar electronics industry, and it has been propelled by high technology to become one of the leading sources of economic growth for a country in this industrialized world. These benefits are largely due to technology and its ability to consistently double the number of transistors on a chip.

The manufacturing facility where chip manufacturing occurs consists of three main elements—clean rooms, highly specialized equipment and highly skilled labor. The ever-increasing cost of materials, process complexity and labor costs, in addition to the cost for building such as facility under the present stringent standards is more than a billion dollars (49, 66). Even though all these costs are increasing, the individual chip prices continue to drop because of continuously improving productivity. To stay profitable chip manufacturers must continuously improve their efficiency, yield, and cost-control at all levels. The expenses of building and operating semiconductor fabs have grown so large that many firms find it difficult to produce chips in their own fabs for less than the chip's selling price. Thus, many firms are turning to wafer-foundries to do some of their manufacturing. By sharing the

cost of fab-operations, the production costs could be reduced, in turn enabling chip manufacturers to remain profitable.

1.5 Wafer Fab operating costs

Figure 6 below illustrates the major factors that contribute to production costs of devices manufactured in wafer fabs.

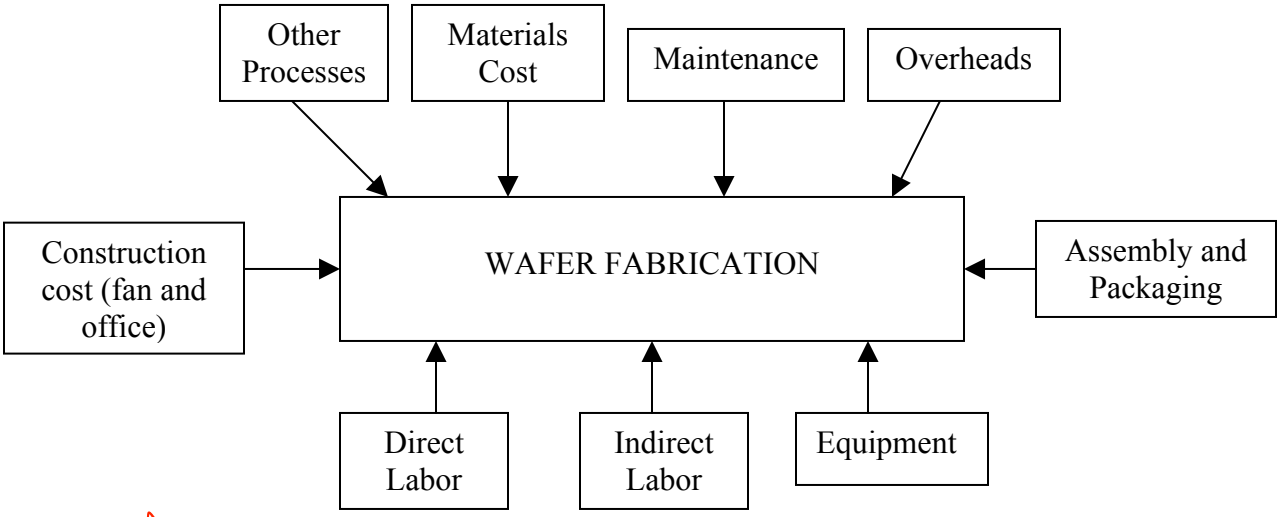


Figure 6: Cost associated with operating a wafer fab

The facility, overhead, equipment and labor costs shown in figure 6 are fixed costs. These fixed costs lay a financial burden on any semiconductor fab irrespective of whether any chips are manufactured. Over a long period of time labor costs could be considered variable costs, as the level of staff and operators change to meet the production requirements. Another variable cost is the materials in the fabrication, since they also fluctuate with the volume of wafers produced. Generally, in these industries fixed costs such as land, construction and maintenance of fab and equipment are high followed by labor and overhead costs. Overhead costs can grow significantly when fabs are expanding.

1.5.1 Overhead costs

Overhead costs are associated with salaries or wages of administrative and executive staff of wafer fabs with the additional cost of providing and maintaining the facility. This cost grows faster than manufacturing costs for as a fab grows more data needs to be handled from customers and suppliers. Providing clean conditions and maintaining a facility is also a major expenditure. Clean room occupies about 30% of a square footage of a wafer-fab (56), yet, it requires a major share of the expenses to build and operate. Air conditioning, utilities, and many other costs of building and operating a clean room contribute significantly towards overhead costs.

1.5.2 Material costs

The materials used in manufacturing chips or any industries are divided into two groups, direct and indirect material costs. The materials that are considered direct costs are those materials, which are integral parts for a final chip. This includes starting wafers, added metal layer-materials and packaging materials. Indirect material costs are those materials that are required for manufacturing the chip, but do not develop into an integral part of a chip, e.g. masks, gases, cleaning chemicals, photo resists.

1.5.3 Equipment costs

The cost of equipment involves tools, which are directly used in the fabrication of wafers. It is considered a major fixed overhead cost or depreciation. The cost of tools has increased tremendously with time. In 1975, cost for wafer processing equipment was about $10,000; it rose to $100,000 in 1985. In 1995 the price was around $500,000- $1 million and by the year 2003 it ranged between $5 million to $10 million per-tool (for 300mm wafer) (49, 51).

1.5.4 Labor costs

Labor costs consist of two components: direct labor costs and indirect labor costs. Direct labor costs are associated with those workers who actually handle the wafers and equipment. Indirect labors costs involve those personnel who support the production and direct labors, e.g. supervisors, engineers, technicians, office workers.

1.6 Semiconductors

The integrated circuits of electronic products consist of semiconductor materials such as silicon, gallium arsenide, and gallium phosphide. The unique physical and electrical properties of these semiconductor materials permit fabrication of such ICs. Semiconductors are those materials, which have electrical-conductivity in the range of a conductor and an insulator. They show one set of electrical properties when pure, but if impurities such as dopants are added then their electrical properties are controlled by these dopants. Germanium was the first semiconductor material used to make bipolar-transistor in 1947, but was largely replaced by silicon for the following reasons (49).

- Narrow band gap (0.66 eV) limits the operation of Ge-devices to temperatures below 212^{o} F (100^{o} C)
- Ge melts at a relatively low temperature of about 1700^{o}F (937^{o} C).
- It is unstable at high process temperatures and dissolves in water.

Silicon is one of the most abundant elements found in nature. The cost to refine it to the very pure form required for semiconductor applications is about 1/10th of that of germanium. A larger band gap of silicon (1.1 eV) allows silicon devices to operate up to 300^{o}F (150^{o} C) with higher breakdown voltages. The oxide of silicon, SiO_2, is easy to form and is chemically very stable up to 2750^{o}F (1500^{o} C). SiO_2 also has mechanical properties similar to silicon, which allows high temperature processing without excessive wafer-warpage and it does not dissolve in water (49, 67).

There are two element semiconductors found in column IV of the periodic table, silicon and germanium. In addition, there are some compound materials that exhibit semi conducting behavior. These can be composed from the elements of columns III and V such as gallium arsenide, gallium phosphide and indium phosphide (49, 67).

1.6.1 Silicon - Semiconductor material

VLSI and ULSI technologies are completely based on Silicon (Si), a widely used semiconductor material for the electronics industry. Silicon is the second most abundant element found on earth. Its atomic number is 14 and it is found in column IV of the periodic table. Silicon has a high melting point (1420^{o}C). It is a dense, hard and brittle material, silver gray in color. There are about 5 x 10^{22}atoms/cm^{3} in single crystal silicon. This number is important because it guides us while dealing with impurity-dopants in silicon.

1.6.1.1 Intrinsic Silicon (Pure Silicon)

Pure-silicon contains no contaminants or impurities. Since silicon has four electrons in its valence shell it shares each of them with neighboring silicon atoms to form four covalent bonds. This bonding completes the valence shell in all of the silicon atoms. Many of the silicon properties arise from such covalent bonding. These bonds are strong, making silicon a stable-solid at room temperature. Resistivity of silicon is high, about 220,000Ω-cm. But in its pure form silicon is not of much practical use in semiconductor technology (49, 67).

1.6.1.2 Extrinsic silicon (Doped silicon)

Adding small quantities of dopants i.e. certain other elements, through a process called doping, decreases the high-resistivity of intrinsic silicon. This process allows such doped silicon to become suitable for fabricating semiconductor devices. Even the presence of small quantities of such dopants can dramatically decrease the resistivity of intrinsic silicon

eg: adding one dopant atom like boron or phosphorus can decrease the resistivity by a factor of over 1 million (49). The more impurities are added; better the conductivity of the silicon. Doping of silicon also helps in the flow of current of either negative charge or positive charge through the flow of holes (vacant spot in the covalent bond). A dopant type will determine that silicon can be made either electron rich (n type), or hole rich (p type). The ability to create these regions allows devices, such as pn-diodes and bipolar transistors, to be built in silicon (49, 67).

1.6.2 Dopants in silicon

Si has four valence electrons in its outermost orbit and is found in column – IV of the periodic table. Electrons from the adjacent columns in the periodic table are most commonly used for doping Si, namely in column III (eg. Boron) has three vacant electrons while those in Column V (Phosphorus or arsenic) have five. When column III dopants (Boron) are added to Si, the material is called p-type silicon, or acceptor. When column V dopants (Phosphorus) are added to silicon, the material is called n-type silicon or donor (49, 67).

1.6.3 Other semiconductor materials

Silicon (Si) and Germanium (Ge) are the two elemental-semiconductor materials from column IV of the periodic table. Si is the widely used material for semiconductor applications, while germanium is used in some specialty semiconductor devices, such as high-power pn-diodes.

Other types of semiconductor materials are compound semiconductors; this kind of semiconductor materials consists of two or more elements. The applications of devices using these alternative semi conductor materials are optical devices, (LEDs, infra red detectors, solar cells, semiconductor lasers, etc), high frequency communication chips (microwave circuits for wireless applications), and special high power devices. Also**,** these devices are important, but they consist of around 2% of the total sales of semiconductor devices (49).

The most widely used alternative semiconductors consist of materials from column III and V of the periodic table (eg. compounds like GaAs, GaP, and InP). GaAs is the most widely used alternative semiconductor material and is primarily used for high frequency devices needed for communications. High mobility of electrons in GaAs allows these devices to operate at speeds that are about 3 times faster than other silicon devices. GaP and GaAsP are used in manufacturing light emitting diodes (LEDs). GaN is used in manufacturing blue and white LEDs. Other compound semiconductors are II-VI materials such as CdSe and ZnSe. These alternative semiconductor materials made up a small market around $179 million in 2001. CdTe is used to make infrared detectors and ZnSe to make blue LEDs (49, 67).

1.7 Manufacturing Microchips

The integrated circuits used in electronic systems are fabricated on silicon wafers in a wafer-fabrication facility. A number of the main processes used to fabricate are given in figure 7 (49). The manufacturing flow for makings ICs is basically a sequential layering process. In an IC, a silicon wafer is the substrate and layers of silicon dioxide, polysilicon, metal-layers, and dopants are added, and are covered with an overcoat to make the end product. The design, fabrication, tests and packaging of integrated circuits is the most complex manufacturing sequence carried out in the world.

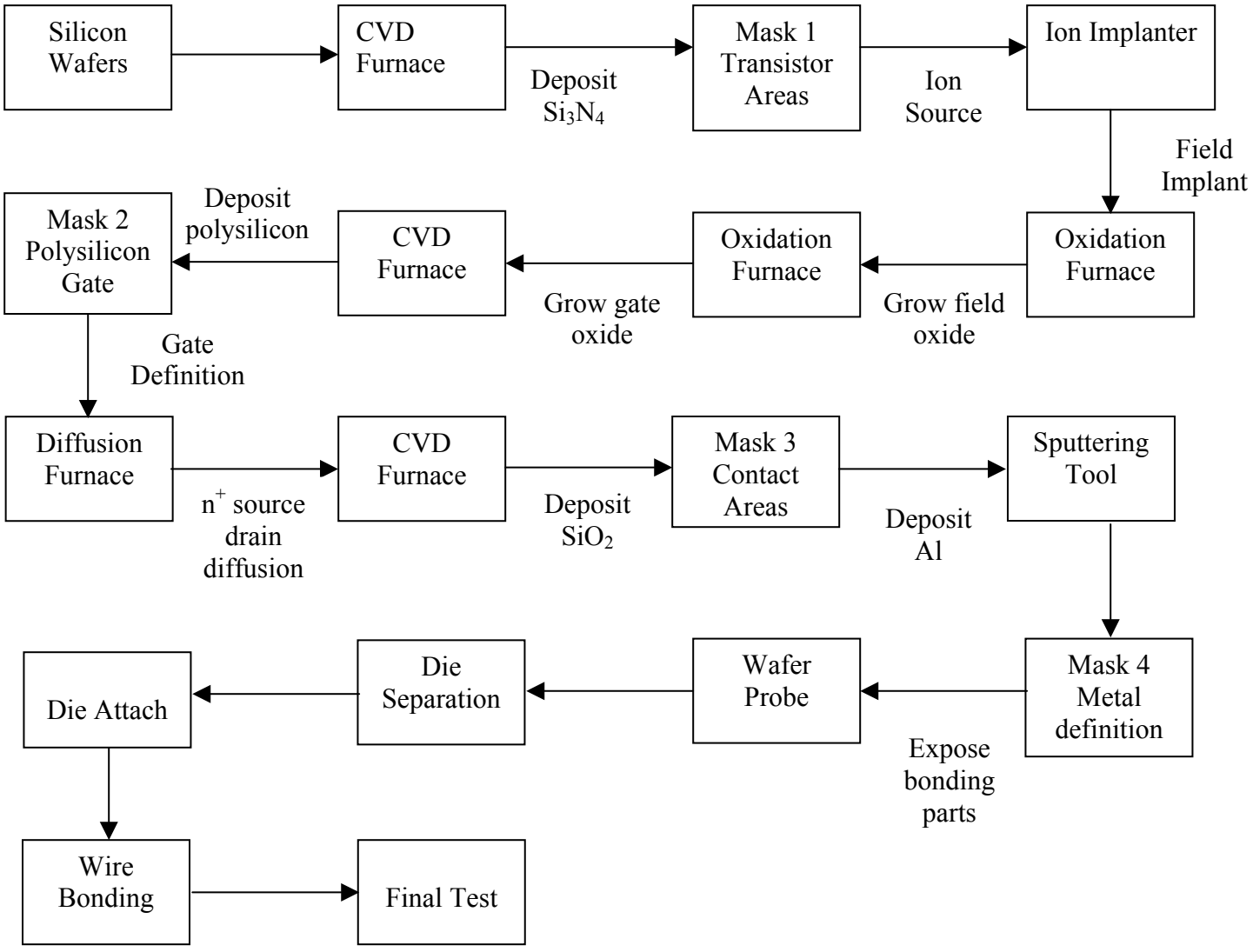


Figure 7: Overview of the sequence of process steps involved in manufacturing microchips (49)

ICs are manufactured in a wafer fabrication facility, and then the finished wafers are sent to another plant (or to an assembly line), called assembly/packaging plant where the wafers are cut apart and mounted into chip-packages. The packaged-ships are sent to the PCB-factory for mounting onto the PCBs. The breakdown of types of ICs sold in 2000 as a percentage of total sales is shown in the pie chart below (figure 8) (49). It can be clearly seen that CMOS was the most widely IC-device technology in use, while other types of ICs are having a smaller share.

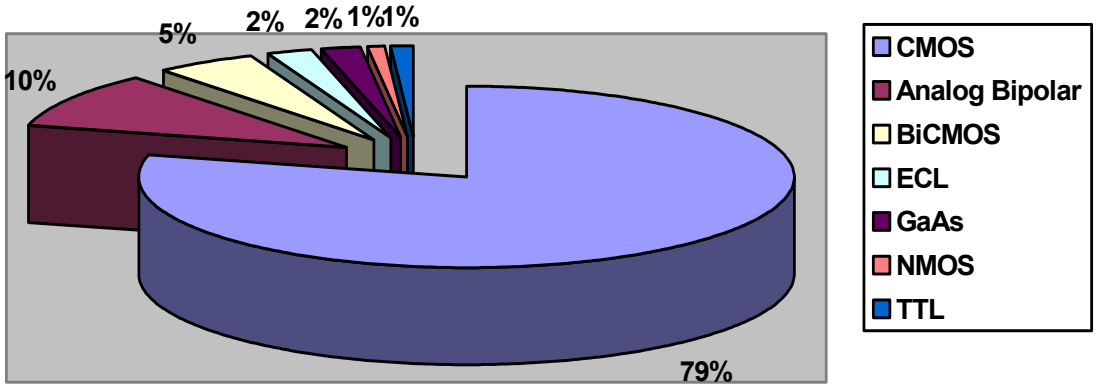


Figure 8: Pie chart showing percentage of total sales for ICs (49)

1.8 Semiconductor Fabrication

Important steps involved in manufacturing process of microchips comprises of four major operations (49):

1. Oxidation
2. Deposition
3. Lithography
4. Diffusion/Ion implantation

The process that allows growth of high quality oxide films to appropriate thickness on the silicon surface is known as thermal oxidation. These layers are grown by oxidation process in which silicon wafers are exposed to high quality oxygen. Thermal oxides provide a uniform, stable protective layer on the silicon wafer. Another important application for thermal oxide is to act as a blocking barrier to the diffusion of most of the electrically active impurities used for doping of silicon.

Chemical Vapor Deposition (CVD) is the process in which a film is deposited by chemical reaction or decomposition in the gas phase in the neighborhood of substrate. CVD is usually necessary to deposit silicon dioxide or silicon nitride on the top of the existing oxide, metal or nitride layers. These are high quality oxides but inferior to thermal oxides.

Silicon nitride is used as a passivation layer in some circuits and also serves as a constituent in multilayer gate insulators in certain types of MOS circuits.

The patterns that define structures in ICs are created by lithographic process. A layer of Photolithography material is first spin coated onto the wafer substrate, and then the resist is selectively exposed to some form of radiation, such as ultraviolet light or electrons. An exposure tool and mask are used to produce the desired selective exposure.

Diffusion is a natural phenomenon by which substances move from regions of higher concentration to regions of lower concentration. Diffusion ceases when the concentration becomes uniform everywhere. Ion implantation is a process through which energetic, charged atoms are directly introduced in the substrate. Ion implantation is primarily used for adding dopants in the silicon. Adding small amounts of impurities through a process called doping can decrease high resistivity of silicon. This process allows such doped silicon to become suitable for fabricating semiconductor devices.

1.9 Assembly and Packaging

Chip packaging is the final procedure carried out in the manufacture of integrated circuits. Various steps performed on a chip after wafer fabrication is completed are (49):

1. Wafer mounting
2. Wafer sawing
3. Die separation
4. Die attach
5. Wire bonding
6. Package

Wafers are mounted on myplar-tape frames for the preparation of sawing. After the chips have been subjected to preliminary testing for functionality the wafer is cut apart by a process called dicing. Die separation is done with a circular diamond impregnated dicing

saw, which cuts through the wafer. The wafer surface is prepared for die separation. The frames mounted into a cassette are loaded in the dicing machine and each frame is moved from cassette to an alignment station, where wafer is aligned with the cutting blade.

After the wafer is sawed the backside is separated and functional die must be attached to a package or substrate, and this procedure is known as die attach or die bonding. The quality of this adhesive bond is critical to the long-term stability of the assembled parts. The connection between the die and substrate must be in the form of a total intimate contact, without any voids that would lead to crack causing stress to the die.

The wire bonding process is carried out after the die-attach step. Flexible wires are attached, one at a time, from bonding pads on the top of the chip to the package. One of the three methods is used to join the wire to the chip and substrate (49):

- Thermo compression bonding
- Ultrasonic bonding
- Thermo sonic bonding

The materials used for bonding are either Au or Al because these materials are highly conductive and ductile enough to withstand the deformation that occurs during the bonding steps. They also bond well to metallization used both on chips and package.

IC chips are usually encapsulated in an IC package prior to their being installed into electronic systems. The IC package performs four key functions (49):

- Sturdy leads that allow an IC to be connected to the system
- Physical protection for the chip against breaking or scratching
- Environmental protection against damage from chemicals, moisture, or gases
- Dissipation of the heat generated by the chip during operation

IC package technology is generally divided into two categories: hermetic and non-hermetic packages. In hermetic packages the chip is housed in an environment isolated from the external world by a vacuum tight enclosure. In non-hermetic packages the chip is not

completely isolated from the outside ambient (moisture or other substances can penetrate the polymer material which encapsulates the chip) after the chip to package connections are complete. A metal or ceramic lid is placed over the cavity and it is sealed to the base. The most widely used method for sealing process is welding, because it is a rapid, reliable and highly reproducible technique.

1.10 Need for Research

In the present era, manufacturing companies have to deal with unprecedented opportunities in the national and the world market, matched by unrelenting competition in its own nation and even throughout the world. However efficient a manager is in seizing opportunities and facing challenges, he is also expected to achieve and maintain good standards in the following five priorities or even necessities:

- Productivity
- Cost determination
- Pricing
- Dealing with competition
- Quality control

From the above priorities, cost is a major factor in all of priorities; so reducing costs can help the manager achieve many of these priorities. So now a big question arises in the mind i.e. *what are the costs?*

The capital investment needed to build the next generation wafer fabrication facilities has grown above the one billion dollars mark. The industry is in the process of determining the transition to the next generation of semiconductor technology. This includes the transition from 200mm to 300mm or advanced production at 200mm. A decision that many organizations have to consider is whether to upgrade the existing facilities or build a new one. With investments of over a billion U.S. dollars for recently completed wafer fabs, and 1.3-1.5 billion dollars U.S. projected for 300mm or advanced technology 200mm facilities, a

well-formulated business plan is paramount. All possible options and scenarios must be considered to achieve dependable estimates of profit/loss, cash flow, rate of return, or Return of Original Investment (ROI) (45).

There are three non-traditional manufacturing ways by which semiconductor industry has been successful in reducing cost per die:

1. Make smaller dies, thereby increasing chip/wafer
2. Increasing wafer size
3. Improving yield

Semiconductors have been successfully decreasing the size of microchips and doubling the transistors on a chip every 1.5 years (as per Moore's Law). This ability to double the transistors depends on being able to reduce the feature sizes with time. Presently these feature sizes are less than a micron. Semiconductor industries have found it challenging to reduce feature sizes like gate dielectric in the near future; additionally it also needs new and highly accurate instruments to achieve those features (68).

Increasing wafer size increases the area and each wafer can carry more dies on it. Additionally, as the size of wafer increases percentage of partial dies on a wafer decreases. There was a trend in semiconductor manufacturing to increase the wafer size by 50mm after every 5 years. Semiconductor industry has found it challenging to do so due to large investment costs. It has skipped 250mm and is now set to skip 350mm and 400mm wafer size (Next generation wafer size is 450mm). These wafers are huge in size and are not easy to transport (heavy for an operator to handle). Many material handling problems have also started surfacing with increased wafer size.

Improving yield still remains a low cost option for the semiconductor industry for new product lines in order to decrease cost per chip. Many mature products are already at very high yield and semiconductor industry has again found it a challenge to improve on their yield without big investments.

All the above three ways needs technology leaps and heavy investments (new and expensive equipments). In future, semiconductor industries will have to look at alternate ways to reduce its costs and be competitive. In traditional manufacturing many industrial engineering techniques or methods like scheduling, layout, optimization techniques and other production control processes are being applied to reduce cost and increase productivity without high investments. Semiconductor industry can benefit from some of these tools.

1.11 Research Objective

Every operating wafer fab is required to improve its effectiveness and reduce the cost of manufacturing to meet constant demands of competition. In today's economic environment existing fabs must increase their productivity by focusing on improving tool utilization, better labor management, improving yields, adding new processing technologies and increasing capacity while pursuing lower overall manufacturing costs. Couple this with the increasing capital costs for new factories and it is no wonder that companies are placing more emphasis on how to get more from existing resources (48). To achieve this, semiconductor fabs must know the optimum resources needed to run their fab and must try to achieve it. All the resources can be tied to a cost, which requires a fab to do its cost analysis.

As, in our competitive business world, accurate cost analysis and pricing are the key to success. Managers need an effective managerial accounting and product costing system. Product costing offers insight into production processes, competitive advantages, and avoidance of cross-subsidization, integration of strategic plans and focuses on continuous improvement in the processes and activities that create costs to add value, developing an understanding of factors contributing towards the cost of a product. This in turn helps to calculate a sales price suitable for both fab and the customer.

1.12 Conclusion

For semiconductor fab to stay profitable and be competitive managers must know the cost of the product, and since the competition in microchip industry is growing rapidly, managers must know the cost incurred on a single chip to determine the fabs profit levels or selling price. It can also help the managers to predict the cost of new chip or ICs for the semiconductor fab. It is also important to know the optimum resources (equipment and labor) needed for a specific product for a specific production quantity. Knowing these resources helps a manager determine an estimated price for new product or accurately calculate manufacturing cost of a specific product.

2.0 Literature Review

2.1 Manufacturing process and its details

Some of the steps involved in the processes of manufacturing a microchip chip consist of digging holes in silicon wafers and coating them with materials. At various stages, level set methods can be used to track the progress of the surface profile as it is shaped and formed (1). Various complex manufacturing processes for semiconductor industries like etching, deposition and lithography with different dimensional methods are used in semiconductor manufacturing (2, 3, 4, 5, 6). Hyper-pure silicon is referred to as polysilicon in the industry. Molten polysilicon is drawn into single-crystal ingots via Czochralski (CZ) or Floating Zone (FZ) methods, which are then sliced into wafers. Wafers are polished and cleaned via a chemical, mechanical polishing process (17). Assembly includes the encasing of rectangular segments of fabricated wafer, called dies, into a protective package with external leads (black box with silver legs). Plastic and ceramic packages are very commonly used in the packaging of microchips (17).

Different machining methods are available to transform silicon ingot into wafers (30). The manufacture of silicon wafer from the ingot stage to the wafer stage is a complex machining process (31). By varying the position of the central chip and computing the number of chips per wafer, the chip replacement that maximizes the chip count can be determined (32, 33). Detailed fabrication of a microchip from raw silicon to chip is a long and tightly controlled manufacturing process (34).

2.2 Energy and Material flow

Energy and materials are consumed in varying quantities in different processes for the production of semiconductor devices. Harmful chemicals & gases that are released and disposed while manufacturing microchips can have stern environmental impacts (7). Material flow analysis is examined for the semiconductor production chain as well as a life cycle

assessment of a computer memory chip (8). Microelectronics and Computer Technology Corporation (MCC) published results for electricity use, water consumption and aggregate chemical wastes for production of a complete set of microchips for a computer (9). The United Nations Environment Program (UNEP) and the United Nations Industrial Development Organizations (UNIDO) jointly published a report on the semiconductor industry surveying waste management issues, which included detailed data on materials inputs for "generic" integrated circuit fabrication process on a 4 - inches diameter wafer (10).

2.3 Clean room details

Examining first the structure of energy use in the fabrication stage, International Semiconductor reports that clean room heating, ventilation, and air conditioning are apparently major energy consuming operations, accounting for around 50% of the total, while wafer processing tools account for 30-40% (12). A Lawrence Berkeley Laboratory website reports the following structure of energy use: 35% for process tools, 26% for ventilation, 20% for chilling, 7% for production of liquid nitrogen, and 5% for purification of water (13).

2.4 Chemical and water usage details

A typical 6-inches wafer fabrication plant processing 40,000 wafers per month reportedly consumes 2-3 millions of gallons per day, which corresponds to 18-27 L per centimeter of silicon (14). Raw silicon is typically 98.5%-99.0% pure and must be purified in order to meet the demands of semiconductor fabrication. Powdered raw silicon is reacted with chlorine to yield trichlorosilane ($HsiCl_3$) that can be conveniently purified via distillation (15). The resulting trichlorosilane is at least 99.9% pure with few metallic impurities (to the level of several hundred parts per billion). In widely used Siemens process trichlorosilane is reacted with hydrogen to yield pure elemental silicon via chemical vapor deposition; resulting in 99.9999% pure (metals less than 0.4ppb) (16). Different chemicals

used and harmful gases emitted in semiconductor fabrication per square centimeter of input wafer are listed for a fab (9, 10).

2.5 Cost awareness in the industry

A cost model is needed to better plan IC product design and reduce cost by predicting the IC manufacturing test cost at an early stage of the design cycle without relaying on detailed information (18). Combining the Operation Costing technique with a modeled performance analysis system provides for opportunities such as cost planning, product costing and other what if analysis (19). Test costs represent a major and rapidly increasing percentage of IC manufacturing costs. Embedded Deterministic Test (EDT) is a new design-for-Test (DFT) technology that reduces manufacturing test costs by providing up to 10 times reduction in test data volume and scan test time (20). A new quality engineering technique called the robust design method drastically reduces the number of time-consuming tests needed to determine the most cost-effective way to manufacture microchips while maintaining high quality standards (21).

1998 is remembered as the worst year for the UK semiconductor industry since 1971. The most extraordinary shut down was of the Siemens fab in North Tyneside - the only example of a modern fab being shut in the recession. In 1998, $1.2 billion loss for its semiconductor operation was the nail in North Tyneside's coffin. Hyundai and LG both completed fabs to the point of hooking up the production machinery before the slump in chip prices made them commercially unviable (46).

A study of 29 wafer fabs conducted for benchmarking semiconductor manufacturing, conducted by a research program at university of California at Berkeley suggested different best practices for semiconductor industry. Making manufacturing error-proof, automate material handling, integrate process, equipment and product data, developing problem solving organization, reduced division of labor, management and introductions of new technology with proper scheduling are some of the recommended practices. It also listed

some of the successful approaches such as proper leadership, communication, complete accountability, and responsibility for improvement and drive for improvement (47).

2.6 Chip manufacturing yield details

Chip's manufacturing yield can be estimated by using one of the many available yield prediction models (22, 23, 24, 25, 26, 27, 28). Each of the IC yield models has its own strengths and limitations. A detailed discussion on these IC yield models is also found in the literature (29). Achieving high yields over 100-200 complex process steps are a key challenge for the semiconductor industry. Overall yield varies between 16% and 94% depending on the complexity and maturity of the technology (17).

An integrated approach towards MEMS manufacturing is required where CMOS compatibility has been taken as the primary constraints (65).

2.7 Economic Analysis

A cost and productivity learning process was carried out on a large capacity CMOS manufacturing line at IBM Burlington facility from 1991 to 1993. Major productivity gains were realized through process and tool improvements affecting yield and through work in progress optimization and scrap reduction (70).

According to John Heaton, President & CEO, Nanometrics Inc, Integrated Metrology (IM) lowers manufacturing risk at a reduced cost. He added that it also helps eliminate bottlenecks inherent in standalone metrology while keeping a relentless watch on process window (69). According to Gideon Argov, President & CEO, Entergris Inc, right process, with the right tool provider, at the right device manufacturer, is the key to growth and sustained profitability (69).

2.8 Conclusion

The semiconductor industry is a billion-dollar industry, which is still in the growth phase. This kind of electronic manufacturing is different from traditional manufacturing processes and it has been using new technologies instead of traditional cost reduction methods to achieve productivity. According to many top executives connected with the semiconductor industry, it is getting tougher to achieve productivity through leaps in technology. Semiconductor industries are now looking at some traditional methods of manufacturing to achieve productivity and remain in competition (69).

3.0 Research Approach

3.1 Methodology

The goal here is to identify the process and cost that governs the production of microchips and study its effects on the manufacturing sequence and production control. The manufacturing sequence for a CMOS chip is given below (Section 3.2.1). An effort is made to apply the research approach to determine the cost of manufacturing a microchip. Before going into analysis, the manufacturing sequence and its relevant information is described in this chapter.

3.2 Manufacturing process for a CMOS chip

A CMOS integrated circuit involves around 350 manufacturing steps. The manufacturing process mentioned below is of 15 masks; twin well and 2 level metal CMOS inverter process flow. Most of the CMOS integrated circuits are fabricated from the silicon wafers with an (100) orientation (49). This orientation is mainly preferred because when silicon (100) wafers are oxidized during CMOS processing, these orientation wafers yield the lowest residual charge at the oxide-semiconductor interface compared to the other silicon wafer orientations. There are typically two types of starting silicon wafers for the CMOS manufacturing, the first is lightly p-doped wafer known commonly as p-bulk wafer and the second material is a heavily p-doped wafer on which a thin lightly p-doped epi-layer is grown. The concentration of phosphorus in both the bulk wafer and the surface p epi-layer is around $8 \times 10^{14} - 1.2 \times 10^{15}$ cm^{-3}. The surface below the epi-layer, p^+ is Boron doped around 10^{20} cm^{-3} (49). Generally, the semiconductor industry tends to use p-epi-on p^+ wafers due to the following advantages (49):

- Improved latch up protection
- Gate oxides with better dielectric reliability are grown on epi-layers than on bulk-Si surfaces.
- Improved gettering capability is obtained

- Low source/drain to substrate capacitance
- High source/drain to substrate voltage
- High carrier mobility
- Low sensitivity to source substrate bias effects

The only major disadvantage with the epi-wafers as compared to p bulk wafer is their higher purchase cost.

3.2.1 Detailed manufacturing process for a CMOS inverter

1. Formation of Active regions, Channel stops and LOCOS-Isolation Structures
    - Cleaning of the Wafers
    - Thermally grown thin pad oxide (Thickness: 40-50 nm)
    - Silicon Nitride deposition by LPCVD process
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 1
    - Dry etch nitride layer
    - Implant boron ions for a channel stop dopant layer
    - Strip the resist
    - Thermal oxidation for field-oxide layer (Wet oxidation: 350-400 nm)
    - Strip the silicon nitride

2. Well-Formation
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 2
    - Implant boron ions for p-wells
    - Strip the resist
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 3
    - Implant phosphorus ions for n-wells

- Strip the resist
- Diffuse the well-dopants

3. Threshold-Adjust Implantation Step
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 4
    - Implant boron ions to adjust V_{Tn}
    - Strip the resist
    - Apply a layer of photoresist
    - Exposure resist layer using Mask # 5
    - Implant boron ions to Adjust V_{Tp}
    - Strip the resist
    - Etch the pad oxide layer

4. Gate-Oxide Growth
    - Carefully cleaning the wafers
    - Gate oxide (thickness: 10-20 nm)

5. Polysilicon-Deposition and Patterning
    - Deposition of undoped polysilicon film by LPCVD
    - Doping of phosphorus on polysilicon film
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 6
    - Dry Etch the polysilicon film (By anisotropic polysilicon etching)
    - Strip the resist

6. Formation of Source/Drain Regions
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 7
    - Implant Arsenic ions for self aligning

- Strip the resist
- Apply a layer of photoresist
- Expose resist layer using Mask # 8
- Implant light dose of Boron ions for source and drain
- Strip the resist
- Silicon nitride or silicon dioxide layer deposition by CVD
- Anisotropic etching to clear layer from flat areas
- Apply a layer of photoresist
- Expose resist layer using Mask # 9
- Implant heavy dose of Arsenic ions for source and drain
- Strip the resist
- Apply a layer of photoresist
- Expose resist layer using Mask # 10
- Implant heavy dose of Boron ions for source and drain
- Strip the resist
- Furnace annealing for active device formation

7. Formation of $TiSi_2$ Salicide
    - Etch the thin oxide
    - Clean the water surface
    - Deposition of Titanium by sputtering (Thickness: 50-100 nm)
    - Heat the wafers at 600^oC in N_2 ambient
    - Wet Etch Titanium
    - Heat the wafers at 800^oC in N_2 ambient

8. Premetal-Oxide Deposition and Planarization and Contact-Formation
    - Doped silicon dioxide layer deposition by CVD
    - Planarity by CMP
    - Apply a layer of photoresist
    - Expose resist layer using mask # 11

- Contact windows are open by dry-etch step

9. Metal-1 Deposition and Patterning
    - Thin layer of Ti/TiN deposition by sputtering
    - Deposition of blanket-W layer by CVD
    - Planarity by CMP
    - Deposition of Al:Cu alloy films by sputtering
    - Apply a later of photoresist
    - Expose resist layer using Mask # 12
    - Al:Cu metal lines are created by anisotropic Al dry-etch process

10. Intermetal-Dielectric Deposition, Via Patterning, and Metal-2 Deposition and Etch
    - Intermetal Dielectric is deposited
    - Planarity by CMP
    - Apply a layer of photoresist
    - Expose resist layer using Mask # 13
    - Al:Cu metal lines are created by anisotropic Al dry-etch process
    - Thin layer of Ti/TiN deposition by sputtering
    - Deposition of blanket-W layer by CVD
    - Planarity by CMP
    - Deposition of Al:Cu alloy films by sputtering
    - Apply a later of photoresist
    - Expose resist layer using Mask # 14
    - Al:Cu metal lines are created by anisotropic Al dry-etch process
    - Number of metal layers can be multiplied by repeating this step and at the end of the step an annealing process in H_2 is carried out for reducing the interface trap density in the gate oxide.

11. Passivation Layer and Pad Mask
    - Deposition of a passivation layer

- Expose passivation layer using Mask # 15

12. Assembly and Packaging
    - Wafer sort – probe test
    - Die separation – wafer saw
    - Die attach – bonding
    - Wire bonding
    - Packaging IC chip.

3.3 Cost structure for a semiconductor fab

A huge amount of dollars are spent in constructing a semiconductor fab. For any semiconductor business to be profitable, cost of sales should be higher than amount of dollars spent to manufacture the product. Cost of semiconductor equipment have been increasing rapidly and are the main cost drivers for a chip, along with the fab, plant personnel and other overhead costs.

For building a semiconductor fab the initial costs are for plant location (area and its cost), construction costs of a fab and equipment needed for the product line. For construction of plant and fab a layout of a specific capacity for the factory is needed. The average load of a United States semiconductor is about 11,000wafers/week, 5 days/week (2 days for scheduled maintenance) (50). To achieve that goal, a schedule (minimum completion time) and layout is required.

Table 3 shows the list of machines essential for the CMOS manufacturing process.

Table 3: List of processes and machines required

Process	Machine
Cleaning	Centrifugal Washer/Dryer
Oxidation	Vertical Furnace
Deposition	LPCVD/PECVD
Photolithography	Resist track/Stepper island
Etching	Plasma Etch (dry)
Ion Implant	Medium current implanter
Resist Strip	Centrifugal stripper
Diffusion	Diffusion furnace
Deposition	Sputtering system
Polarity	CMP
Wafer sort test	Wafer probe
Die separation	Dicing saw
Die attach	Die bonders
Wire connection	Wire bonder
Packaging	Direct chip attach
Inline parametric test	PCMs

The nature of manufacturing sequence makes the wafer visit the same machines (or cells). It would be very expensive to have different machines for every step and hence a cell formation is preferred over straight-line flow.

3.4 Processing time

Every machine has a different processing time; hence it is important have appropriate number of specific machines (with right capacity) in order to ensure a good schedule and flow. The processing time of some specific semiconductor equipment depend upon step sequence or thickness needed (deposition, oxidation, etc), while others are general and take the same amount of time for all other sequences (cleaning, strip, etc). Table 4 shows the step sequence and amount of time needed at each machine.

Table 4: Time calculations for different steps in manufacturing sequence

Process	Machine	Seq #	Time/step (Mins)	M/c (Mins)	Labor (Mins)	Total wafers
Cleaning	Spray processor	1, 23, 46	30	90	36	25
Oxidation	Vertical Furnace					
	Oxide growth 40-50nm	2	57	12	12	150
	Oxide growth 350-400nm	7	125	80	12	150
	Gate oxide 6-20nm	24	50	5	12	150
	Furnace anneal	44	75	30	12	150
Deposition	LPCVD/PECVD					
lpcvd	100nm silicon nitride	3	60	60	12	150
lpcvd	0.4-0.5um polysilicon	25	200	200	12	150
lpcvd	20nm silicon nitride	36	5	5	12	150
pecvd	1um doped Sio2	50, 60	2	4	24	150
lpcvd	Blanket layer 30nm W	55, 65	4	8	24	150
pecvd	Passivation layer 0.5um	70	2	2	12	150
Photolithography	Stepper island					
	4,9,12,16,19,27,30,33,37,41,52,58,62,68,71		30	450	180	25
Etching	Plasma Etch (dry)					
	5,22,28,38,45,53,59,63,69,72		25	250	120	25
Ion Implantation	Medium current implanter	6,10,13,17,20, 26,31,34,39,42	7	70	120	25
Resist Strip	Wet/Dry etching Stripper					
	8,11,14,18,21,29,32,35,40,43		11	110	120	25
Diffusion	Diffusion furnace	15	300	300	12	150
Deposition	Sputtering system - PVD					
1200nm/min	50-100nm	47-49	44	44	12	25
	50nm	54, 64	10	20	24	25
	1000-1500nm	57, 67	30	60	24	25
Polarity - CMP	CMP	51,56,61,66	40	160	24	25
Wafer sort	Probe card	73	30	30	12	25
Wafer dicing	Dicing saw	74	16	16	12	25
Die attach	Die bonder	75	64	64	12	25
Wire bonding	Wire bonder	76	256	256	12	25
Inline test	PCMs		60	60	12	25

3.3.1 Cleaning – Spray processor

Since there are different levels of contamination, there exist separate cleaning procedures to remove them. Many different procedures or techniques can be used to remove different types of contaminations from the wafer. Special care must be taken so that the later steps do not re-contaminate or degrade the effectiveness of the former cleaning procedures. Wafer cleaning operations use highly reactive chemicals that do not attack corrosion resistant materials.

FEOL (Front End of Line) is defined as the cleaning step, which begins with a starting wafer and continues up to the first metal contact. Wafers processed up to the end of FEOL generally contain only silicon, silicon dioxide, or silicon nitride on their surfaces prior to high temperature operations such as oxidation. Bare silicon should be chemically clean before any furnace process; a two-step chemical cleaning procedure known as RCA-clean is used. It takes about 30 minutes to complete the cleaning cycle. A detail break down of time and chemicals is given in table 5 (49). Centrifugal spin rinser/dryer (SRD) and spray processor is the most commonly used cleaning equipment in the fabs. Spray processor has been considered for the cost analysis. Spray processor can process one cassette at a time (51).

The many advantages of spray cleaning over rinser/dryer are:

- Smaller volume of chemicals and water
- Fresh chemicals on wafer surfaces
- Well controlled environment and automation

Table 5: Steps and time for cleaning (49)

Chemical	Time (mins)	Temp (^{0}C)	Task
H_2SO_4/H_2O_2	10	120-150	Strip resist/organics
H_2O/HF	1	Room	Strip chemical oxide
H_2O	1	Room	Rinse
$NH_4OH/H_2O_2/H_2O$	10	80-90	Strip organics, metal and particles
H_2O	1	Room	Rinse
HCL/H2O2/H2O	10	80-90	Strip alkali ions and metals
H_2O	1	Room	Rinse

3.3.2 Oxidation – Vertical Furnace

The goal of a thermal oxidation process is to grow a defect-free, uniform layer of silicon dioxide to the desired thickness. These are high quality insulators that can be used as barriers during impurity diffusion. In addition, it exhibits high electrical stability, a critical factor for building reliable MOS/CMOS chip.

Prior to loading, the furnace is in the idle mode, at an elevated temperature of 800°C and nitrogen purge gas is continuously passed through it. The wafers are loaded onto the fused silica or silicon carbide boat, and the boat with the wafers is slowly pushed into the chamber with nitrogen gas flowing in the chamber.

Temperature is ramped up at a rate of 10-20°C/min. After the required temperature is reached (950°C), the furnace is given a few minutes to stabilize under nitrogen flow. Then dry oxygen with a gas containing chlorine is turned on, and nitrogen is turned off. The oxide grows while oxygen flows through the chamber. After the oxide has been deposited to the specified thickness, the oxygen and gas containing chlorine are turned off. The wafer then undergoes a post oxidation anneal for about another 30 minutes at the process temperature to reduce the oxide fixed charge. Then the furnace is slowly ramped down and when the idle temperature is reached, the tower is withdrawn slowly from the furnace. To allow adequate wafer per hour and higher machine utilization, a large number of wafers must be processed at

once. Dry oxidation is generally used for producing thin oxide films of up to 100nm, while thicker films are grown by wet oxidation.

Vertical furnaces are preferred over horizontal furnaces due to following reasons (49):

- Superior process control
- Fewer particles per wafer
- Better automation compatibility

Even though vertical furnaces are expensive, the semiconductor industry prefers vertical furnaces. Process control is improved as temperature within the vertical furnace is uniform and the wafers are held flat on the backs and are well centered in the tower, which in turns allows the gas flow dynamics to be optimized. Many furnaces have an automated wafer-stocking feature in which multiple cassettes of 25 wafers (up to 6 cassettes) can be maintained in an ultra clean environment (49).

3.3.3 Deposition – LPCVD/PECVD

Chemical Vapor Deposition (CVD) is a process, which produces a solid film by reacting with vapor phase chemicals that contain the constituents of the required film. The reactant gases do not react with any substrate surface material. Wide ranges of thin films are deposited by CVD.

3.3.3.1 Low Pressure CVD reactors (LPCVD):

LPCVD reactors operate in the surface reaction rate under medium vacuum (30-250-Pa) and moderate temperature (550-700^{0}C). At such reduced pressures, the diffusive capacity of the reactant gas molecules is sufficiently increased so that mass transfer to the substrate no longer limits the growth rate. The surface reaction rate is very sensitive to the temperature, but precise temperature control is relatively easy to achieve. The two main disadvantages of LPCVD are their relative low deposition rates (25nm/min) and relatively high operating

temperature (49). Attempt to increase deposit rates will tend to initiate gas phase reactions and attempt to decrease temperature will reduce film deposition rate by a substantial amount. Horizontal and vertical LPCVD are the two LPCVD reactors mainly used in the semiconductor industry. In vertical reactors wafers are perpendicular to the direction of the main gas flow. The gases flow by forced convention through the annular space between the wafers and the walls of the circular cross-sectioned tube. It is similar to the vertical furnace in construction and possesses many similar advantages.

3.3.3.2 Plasma Enhanced CVD reactors (PECVD):

PECVD use rf induced glow discharge to transfer energy into reactant gases allows higher deposition rates (600nm/min) at lower temperatures than LPCVD (49). The plasma is generated by applying an rf field to a low-pressure gas, thereby creating free electrons within the discharge region. Electrons gain sufficient energy from the electric field so they collide with reactant gas molecules. These molecules decompose into radicals, ionic-species, atoms and molecules in excited state, causing chemical reactions to take place at lower temperature.

3.3.4 Photolithography – Resist Track/Stepper Island

The basic sequences of steps that complete photolithography process are:

1. Wafer cleaning & priming
2. Spin coat (0.5-1.5 micron thick)
3. Pre bake (120^{o}C)
4. Expose (Radiation of light intensity waves)
5. Post exposure bake (130^{o}C)
6. Develop (Uniform thickness)
7. Post bake (130^{o}C)

In early days, individual steps for creating a mask were done by stand-alone tools (different tools for the above steps). By 1990 these tools were integrated into resist

processing systems. The systems were then linked to a stepper to form an integrated stepper track photo island. A cassette of wafer is loaded onto the input station and 30 minutes later they emerge as patterned wafer, ready for next step (49). Ion implantation and etching follow after photolithography.

3.3.5 Etching – Plasma Etch

After the resist is formed on the wafer, the next process involves permanently transferring that image into a layer under the resist by etching. Etching is a process by which material is selectively removed from the silicon substrate or from thin films on the substrate surface. Two basic types of etch process are used wet chemical etching and dry etching. Wet etching was used to etch patterns until 1980, but the emergence of smaller sizes has led a shift towards dry etching. Dry etching has been developed so that it can successfully serve as a replacement for wet etching processes. Dry etching also provides important manufacturing advantage by eliminating handling, consumption and disposal of dangerous chemicals. Dry etching uses comparatively small amount of chemicals. Plasma etching is generally used in the semiconductor industry for most of its processes. An rf glow discharge produces chemically reactive species from an inert molecular gas. This etching gas is selected to generate species that can chemically react with the material to be etched.

Etch tools for submicron applications also have a vacuum load lock that isolates the chamber from ambient, and a robot to transfer wafers from cassettes through the load dock to the etch chamber. Barrel etches are the simplest plasma etches to be developed. It consists of a cylindrical reaction vessel, usually of quartz, with rf power supplied by metal electrodes. Most barrel etchers operate at a high-pressure range of dry etching up to 250pa (49).

3.3.6 Ion Implantation – Medium current implanter

Ion implant is a process in which highly energetic, charged atoms are directly introduced into a substrate. Ion implantation is mainly used to add dopant ions on the surface

of silicon wafers. Medium current implanters are more applicable to semiconductor applications as compared to high current implanters.

Medium current implanters have beam currents from a few micro amps to about 1 milliamp, which can operate over a useful energy range of 20-200 KeV. Such machines produce lower dose implants and are used in majority of doping steps. Medium current implanters are single wafer processing machines. A typical implant time is 10 seconds. Using vacuum load locks with cassette-to-cassette loading, wafer-handling time is 2-4 seconds (49). Due to small processing time production rates of implanters are typically higher than other front-end process tools.

3.3.7 Photoresist strip – Wet/Dry etching Stripper

Resist must be removed after following processes (49):

1. Etching
2. Ion implantation
3. Rework

The main objective of resist stripping is to insure that all resist is removed as quickly as possible without attacking underlying surface materials. Wet inorganic strippers are used when the under laying material is SiO_2. It cannot be used when metal films are present on the wafer surface, since the metal would be stripped of its mixtures (Plasma dry etch is used for metal films). A detail break down of time and chemicals is given in table 6 (49).

Table 6: Steps for resist strip (49)

Chemical	Time (mins)	Temp	Task
H_2SO_4/H_2O_2	10	120-150 C	Strip resist/organics
H_2O	1	Room	Rinse

3.3.8 Diffusion – Diffusion furnace

Diffusion is a natural phenomenon by which substances move from regions of higher concentration to regions of lower concentration. Diffusion ceases when concentration is uniform everywhere.

Two conditions must exist for diffusion to take place:

1. Material must exist in higher concentration at some location
2. Material must have the ability to move elsewhere from the regions of higher concentration.

Most diffusion in IC fabrication (Including CMOS) is done in two stages; pre-deposition (pre-dep) and limited diffusion (drive in). In pre-dep, a dopant oxide is formed on silicon surface by passing dopant-containing gas, oxygen and a carrier gas into a heated furnace tube containing wafers. Dopant gas and oxygen react to form an oxide layer on silicon surface containing the dopant. During the short, high temperature pre-dep step ($950^{o}C$ for 30min), dopant from this surface oxide layer enters the silicon at solid solubility concentration at process temperature and diffuses a very short distance into silicon. Despite the fact that the diffusion front moves deeper into silicon as time progresses, pre-dep step is kept short. This is intended to limit the distance that dopant moves into silicon. A second longer (3-10hours) and higher temperature step called drive-in is used to move the dopants to their desired location. Diffusion furnaces are similar to oxidation furnaces in construction and capacity (49).

3.3.9 Deposition – Sputtering PVD

Sputtering is a term used to describe the mechanism in which atoms are ejected from the surface of a material when it is struck by sufficiently energetic particles. Sputtering has become the dominant technique for depositing a variety of metallic films.

There are four stages to a sputter process

1. Ions are generated and directed at target
2. Ions sputter atoms from the target
3. Ejected atoms are transported to substrate
4. Atoms are condensed and form a thin plan

Sputtering systems for 200mm and larger wafers are large and configured cluster tools. In a cluster tool a number of sequential steps can be carried out together without exposing the wafer to the atmosphere between steps. This is accomplished by moving the wafer from one process chamber to another, through an evacuated transfer chamber, using a robotic transfer mechanism. Normal deposition rates for these tools are very high at about 1200nm/min (49).

3.3.10 Polarity – CMP

As the numbers of interconnected layers are increased, planarization of dielectric and metal layers has become more critical (to achieve high yield). All these processes provide only a limited degree of smoothing and local planarization. CMP (Chemical Mechanical Polishing) makes it possible to achieve high manufacturing yields and high device speeds with multilevel interconnects.

CMP polisher differs from Si-wafer polishing tools in many ways. In wafer polishing tens of microns of material are removed, while in CMP only up to 1 micron is removed and uniformity is also stringent. New CMP tools costs ranges from 2-2.5M and are capable of polishing 50-60 wafers/hour (200mm).

3.3.11 Wafer sort – Wafer probe

At the end of wafer fabrication every die is subjected to functional test while the wafer is intact; this test is called as wafer sort. Electric signals are applied to the chip using

probes, which contact the wire-bonding area of every pad. These tests are carried out as high speed dynamic testing is difficult after die packing is completed. A finished wafer is loaded onto a vacuum chuck and the probes of the card are automatically aligned to test the first die on the wafer to be tested. These probes make contact with the bond-pads of the chip. The ratio of working die to total die on the wafer gives the sort yield for each wafer. Dies that fail the wafer sort are not packaged. These failed chips are identified by placing an ink dot on them or by storing the location of the failed part on the wafer in computer. Automated wafer sort machines cost around $600,000 and can run a fully load cassette of 200mm wafer in half an hour (53).

3.3.12 Die separation – Dicing saw

After chips on uncut wafers have been subjected to preliminary testing for functionality (wafer sort), the wafers are cut apart, so that each functional die can be mounted into its own package. Die separation is done with a circular diamond impregnated dicing saw rotating at speed of 20,000 rpm to cut through 100% of the wafer. One dicing saw can support 3-5 die bonders that in turn can keep 15-20 wire bonders supplied. Dicing saws generally range from $150,000 - $250,000 with the speed up to 50mm/sec (49).

Prior to dicing, the wafer is mounted on a sticky flexible tape that is itself attached to rigid frame and the tape continues to hold the die after the sawing operation and during transportation to the next assembly step.

3.3.13 Die attach – Die bonders

After the wafer is sawed**,** the backside of the wafer is separated, and functional die must be attached to a package**.** This procedure is known as die attach. The connection between the die and the substrate must be one of a total intimate contact, without any voids that would lead to crack causing stresses in die. Systems are now capable of die bonding up to 4000 – 6000 parts/hr.

Wafers are presented in sawed wafer form, attached to an adhesive tape. The die bonder has a pock and place unit, and the pickup arm moves in to position over the die to attach. The arm is so lowered that the vacuum collet can pick up the die. Simultaneously an ejector needle pushes the die from underneath, causing die and the adhesive tape to disengage. Fully automated systems for die attach equipment cost around $250,000.

3.3.14 Wire bonding – Wire bonder

Wire bonding process is carried out after the die-attach step. Flexible wires are attached, one at a time, from bonding pads on top to the chip of the package. Materials used for wire bonding are either Au or Al because these metals are highly conductive and ductile enough to withstand deformation during the bonding steps. Fully automated wire bonders can run at a speed of 18,000 bonds per hour and its price is around $250,000 (49).

3.3.15 Packaging – Packageless technology

IC chips are usually encapsulated in an IC package prior to their being installed into electronic systems. Traditionally, IC package technology is generally divided into two packaging categories:

1. Hermetic (Ceramic)
2. Non hermetic (Plastic)

Packageless is new technology that has attracted many semiconductor industries. It has been argued that the package does not add any value to the product. Instead it enlarges the physical presence of the IC and robs some of its performance potential. As the result, semiconductor industries have sought to get rid of the IC package by interconnecting ICs directly to PWBs. These direct chip attachment methods as flip-chip & beam leaded chip technologies were introduced by IBM and AT&T in the mid-1960. By 1990's, the cost of IC package has increased, which led the industries to use this technology. Since rework of failed

circuits is not yet feasible in packageless applications, this technology is limited to high yielding, mature products.

3.3.16 Inline parametric testing

After some process test, measurements are taken to verify that it was done properly. These tests are referred to as inline parametric testing. Final parametric tests are used to provide several kinds of data. First, wafers that fail the test criteria are not processed further. This saves expending production resources. Second, it supplies information about how wafers are processed and the presence of a flaw in the process flow. Yield management teams use such data to find the correlation between different parameters and finished product specification.

All processing time calculations carried out are based on rates (deposition rates, oxidation rates, etc) or fixed time for the equipment. All the intake capacities are based on actual machine capacity from equipment manufactures (51).

3.3.17 Cost of semiconductor manufacturing equipment

The cost of each machine selected for the CMOS manufacturing process mentioned is as listed in table 7 (51, 52).

Table 7: Cost of semiconductor machines (51, 52)

Process	Machine	$/mc
Cleaning	Spray processor	$1,000,000
Oxidation	Vertical Furnace	$1,350,000
Deposition	LPCVD/PECVD	$3,000,000
Photolithography	Resist track/Stepper island	$ 800,000
Etching	Plasma Etch (dry)	$1,000,000
Ion Implantation	Medium current implanter	$2,500,000
Resist Strip	Wet/Dry etching Stripper	$1,000,000
Diffusion	Diffusion furnace	$1,350,000
Deposition	Sputtering system	$1,300,000
Polarity – CMP	CMP	$2,500,000
Wafer sort - probe	Wafer probe	$ 600,000
Wafer Dicing saw	Dicing saw	$ 600,000
Die bonders	Die bonders	$ 540,000
Wire bonding	Wire bonder	$ 250,000
Packaging	Direct chip attacher	$ 250,000
Inline parametric test	PCMs	$1,000,000

Based on processing time, table 8 shows calculations of the number of machines required for a 11,000wafer/week load. Many semiconductor factories tend to have an additional 25% capacity to match and peak demand variations (50). Photolithography, etching, cleaning and deposition equipment makes more than 60% of the total equipment needed, which is pretty close, according to SEMATECH (72)

Table 8: Number of machines need to run an average weekly load of 11,000 wafers with an additional 25% capacity

Process	Mc time (Mins)	Load/ unload time (Mins)	Total time (Mins)	Wafer capacity	# of batch	Total time reqd (Mins)	Round up mc	25% excess
Cleaning	90	36	126	25	440	55440	8	10
Oxidation	307	48	355	150	73	26033	4	5
Deposition	279	96	375	150	73	27500	4	5
Photolithography	450	180	630	25	440	277200	39	49
Etching	250	120	370	25	440	162800	23	29
Ion Implantation	70	120	190	25	440	83600	12	15
Resist Strip	110	120	230	25	440	101200	15	19
Diffusion	300	12	312	150	73	22880	4	5
Deposition	124	60	184	25	440	80960	12	15
Polarity - CMP	160	24	184	25	440	80960	12	15
Inline parametric test	60	12	72	25	440	31680	5	7
Wafer sort - probe	30	12	42	25	440	18480	3	4
Wafer Dicing saw	16	12	28	25	440	12320	2	3
Die bonders	64	12	76	25	440	33440	5	7
Wire bonding	256	12	268	25	440	117920	17	22
Packaging	64	12	76	25	440	33440	5	7

3.4 Depreciation of semiconductor equipment

Deprecation of semiconductor manufacturing equipment is at 5 years (52). Five years of depreciation period relates to the jump to next wafer size every five years as shown in table 9 (as every new wafer size mostly requires new machines). With the passing time, IC manufactures have been fabricating ICs on wafers with even larger diameters.

This has happened for 3 basic reasons.

1. Its area is increased, each wafer can carry more dies

2. Percentage of chips on periphery of a wafer that are partial dies declines as wafer diameter is increased.
3. It becomes economically more effective to manufacture ICs on big wafers.

Table 9: Year vs Wafer size in semiconductor industry

Year	Wafer size
1985	125 (mm)
1990	150 (mm)
1995	200 (mm)
2005	300 (mm)

Increase in wafer size has continued every five years and suggests a trend. If it had continued in 2000 the wafer size should have been 250mm. However the next wafer size chosen was 300mm and it is expected to reach its prime in 2005-06.

Equipment Depreciation (ED):

The following tables—table 10 and table 11 gives you the depreciation values for the above semiconductor equipment (mid year convention with straight line and MACRS depreciation methods). Table 12 gives you the MACRS percentages used.

Table 10: Depreciation of equipment with mid year straight line method (58)

Machine	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Cleaning	$1,000,000	$2,000,000	$2,000,000	$2,000,000	$2,000,000	$1,000,000.0
Oxidation	$675,000	$1,350,000	$1,350,000	$1,350,000	$1,350,000	$675,000.0
Deposition	$1,500,000	$3,000,000	$3,000,000	$3,000,000	$3,000,000	$1,500,000.0
Photolithography	$3,920,000	$7,840,000	$7,840,000	$7,840,000	$7,840,000	$3,920,000.0
Etching	$2,900,000	$5,800,000	$5,800,000	$5,800,000	$5,800,000	$2,900,000.0
Ion Implantation	$3,750,000	$7,500,000	$7,500,000	$7,500,000	$7,500,000	$3,750,000.0
Resist Strip	$1,900,000	$3,800,000	$3,800,000	$3,800,000	$3,800,000	$1,900,000.0
Diffusion	$675,000	$1,350,000	$1,350,000	$1,350,000	$1,350,000	$675,000.0
Deposition	$1,950,000	$3,900,000	$3,900,000	$3,900,000	$3,900,000	$1,950,000.0
Polarity - CMP	$3,750,000	$7,500,000	$7,500,000	$7,500,000	$7,500,000	$3,750,000.0
Inline parametric test	$420,000	$840,000	$840,000	$840,000	$840,000	$420,000.0
Wafer sort - probe	$240,000	$480,000	$480,000	$480,000	$480,000	$240,000.0
Wafer Dicing saw	$162,000	$324,000	$324,000	$324,000	$324,000	$162,000.0
Die bonders	$175,000	$350,000	$350,000	$350,000	$350,000	$175,000.0
Wire bonding	$550,000	$1,100,000	$1,100,000	$1,100,000	$1,100,000	$550,000.0
Packaging	$700,000	$1,400,000	$1,400,000	$1,400,000	$1,400,000	$700,000.0
Total	$24,267,000	$48,534,000	$48,534,000	$48,534,000	$48,534,000	$24,267,000

Table 11: Depreciation of equipment with mid year MACRS method (58)

Machine	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Cleaning	$2,000,000	$3,200,000	$1,920,000	$1,152,000	$1,152,000	$576,000
Oxidation	$1,350,000	$2,160,000	$1,296,000	$777,600	$777,600	$388,800
Deposition	$3,000,000	$4,800,000	$2,880,000	$1,728,000	$1,728,000	$864,000
Photolithography	$7,840,000	$12,544,000	$7,526,400	$4,515,840	$4,515,840	$2,257,920
Etching	$5,800,000	$9,280,000	$5,568,000	$3,340,800	$3,340,800	$1,670,400
Ion Implantation	$7,500,000	$12,000,000	$7,200,000	$4,320,000	$4,320,000	$2,160,000
Resist Strip	$3,800,000	$6,080,000	$3,648,000	$2,188,800	$2,188,800	$1,094,400
Diffusion	$1,350,000	$2,160,000	$1,296,000	$777,600	$777,600	$388,800
Deposition	$3,900,000	$6,240,000	$3,744,000	$2,246,400	$2,246,400	$1,123,200
Polarity - CMP	$7,500,000	$12,000,000	$7,200,000	$4,320,000	$4,320,000	$2,160,000
Inline parametric test	$840,000	$1,344,000	$806,400	$483,840	$483,840	$241,920
Wafer sort - probe	$480,000	$768,000	$460,800	$276,480	$276,480	$138,240
Wafer Dicing saw	$324,000	$518,400	$311,040	$186,624	$186,624	$93,312
Die bonders	$350,000	$560,000	$336,000	$201,600	$201,600	$100,800
Wire bonding	$1,100,000	$1,760,000	$1,056,000	$633,600	$633,600	$316,800
Packaging	$1,400,000	$2,240,000	$1,344,000	$806,400	$806,400	$403,200
Total	$48,534,000	$77,654,400	$46,592,640	$27,955,584	$27,955,584	$13,977,792

Table 12: Rates of mid year straight line and MACRS depreciation (58)

Year	SL rates	MACRS Rates
1	10%	20%
2	20%	32.00%
3	20%	19.20%
4	20%	11.52%
5	20%	11.52%
6	10%	5.76%

3.4.1 Depreciation of office buildings

Office Building (OB) construction is the cost of the building and nearby premises from where the semiconductor plant is operated. Table 13 and table 14 give the depreciation values for the office buildings (mid year for straight line and MACRS depreciation).

Table 13: Office building line depreciation for 20 years (California rates) (52, 54, 55)

Office sq ft	$/sq ft	Total cost
130,000	$203	$26,390,000

Table 14: Office building MACRS depreciation for 20 years (California rates) (52, 54, 55, 58)

Year	SL	MACRS
1	$ 659,750	$ 989,625
2	$ 1,319,500	$ 1,905,358
3	$ 1,319,500	$ 1,762,852
4	$ 1,319,500	$ 1,630,902
5	$ 1,319,500	$ 1,506,869
6	$ 1,319,500	$ 1,393,392
7	$ 1,319,500	$ 1,290,471
8	$ 1,319,500	$ 1,192,828
9	$ 1,319,500	$ 1,176,994
10	$ 1,319,500	$ 1,176,994
11	$ 1,319,500	$ 1,176,994
12	$ 1,319,500	$ 1,176,994
13	$ 1,319,500	$ 1,176,994
14	$ 1,319,500	$ 1,176,994
15	$ 1,319,500	$ 1,176,994
16	$ 1,319,500	$ 1,176,994
17	$ 1,319,500	$ 1,176,994
18	$ 1,319,500	$ 1,176,994
19	$ 1,319,500	$ 1,176,994
20	$ 1,319,500	$ 1,176,994
21	$ 659,750	$ 593,775

3.4.2 Depreciation of fab

The total fab space required is around 100,000 sq ft and total costs according to clean rooms are stated below (56, 57). Table 15 below shows the different rates to construct a fab. Table 16 and table 17 are Fab Depreciation (FD) costs for mid-year straight line and MACRS depreciation. The model does not deal with plant layout issues. Table 18 is the MACRS percentage used to calculate MACRS depreciation for office building and fab. Safety aspects related to fab and buildings are part of the construction costs.

Table 15: Individual clean room class cost (52, 55)

Class	Cost	Sq ft	Total cost
100,000	$100	0	$0
10,000	$200	0	$0
1,000	$300	10,000	$5,000,000
100	$1,000	40,000	$80,000,000
10	$5,000	40,000	$200,000,000
1	$15,000	10,000	$150,000,000

Table 16: Total fab cost (52, 55)

	Fab sq ft	Construction cost
Total	100,000	$435,000,000

Table 17: Fab cost with mid year straight line and MACRS depreciation for 20 years (52, 55, 58)

Year	Straight Line	MACRS
1	$ 10,875,000.00	$ 16,312,500
2	$ 21,750,000.00	$ 31,407,000
3	$ 21,750,000.00	$ 29,058,000
4	$ 21,750,000.00	$ 26,883,000
5	$ 21,750,000.00	$ 24,838,500
6	$ 21,750,000.00	$ 22,968,000
7	$ 21,750,000.00	$ 21,271,500
8	$ 21,750,000.00	$ 19,662,000
9	$ 21,750,000.00	$ 19,401,000
10	$ 21,750,000.00	$ 19,401,000
11	$ 21,750,000.00	$ 19,401,000
12	$ 21,750,000.00	$ 19,401,000
13	$ 21,750,000.00	$ 19,401,000
14	$ 21,750,000.00	$ 19,401,000
15	$ 21,750,000.00	$ 19,401,000
16	$ 21,750,000.00	$ 19,401,000
17	$ 21,750,000.00	$ 19,401,000
18	$ 21,750,000.00	$ 19,401,000
19	$ 21,750,000.00	$ 19,401,000
20	$ 21,750,000.00	$ 19,401,000
21	$ 10,875,000.00	$ 9,787,500

Table 18: Rates used for mid year straight line and MACRS deprecation (58)

Year	SL Rates (%)	MACRS Rates (%)
1	2.5	3.75
2	5	7.22
3	5	6.68
4	5	6.18
5	5	5.71
6	5	5.28
7	5	4.89
8	5	4.52
9	5	4.46
10	5	4.46
11	5	4.46
12	5	4.46
13	5	4.46
14	5	4.46
15	5	4.46
16	5	4.46
17	5	4.46
18	5	4.46
19	5	4.46
20	5	4.46
21	2.5	2.25

3.5 Yield of wafer

One of the cost-effective ways for semiconductor industry for increasing productivity is increasing yield/wafer. If all chips produced on the wafers meet the product specification, they can be sold, thus maximizing sales and profit. However, not all chips work properly and some need to be scrapped and some wafers might need some reworking. This is the most fruitful way of achieving higher productivity as this does not require any high capital investment like increase in wafer size or decrease in size of microchip.

The cumulative die yield Y can be defined as a product of several other sub-yields (49)

"$Y = Y_f * Y_p * Y_s * Y_a * Y_t$ "

Where,

Y = die yield

Y_f = Fraction of wafers that complete the entire wafer flow

Y_p = Fraction of wafers that pass parametric test hurdle

Y_s = Fraction of wafer that pass the wafer sort test

Y_a = Die fraction that have passed wafer sort and are successfully packaged

Y_t = Fraction of packaged chips that passes final test

In modern IC manufacturing fabs, the value of Y_a and Y_t are close to unity. In addition, the increased use of automated wafer transport system (like over bay), and robotic movements of wafers within tools have also reduced the incidence of wafer break to a degree that Y_f can also be considered as unity. Thus, Y_p and Y_s are the major contributors to final yield (49).

In the high manufacturing scenario, a fab has complete volume ramp, and yield curve starts to plateau (around 92%). Additional yield gains can be achieved by new equipment or circuit redesigns. Table 19 shows a sample calculation of a yield.

Table 19: Ex. Yield calculation for a wafer

Yield type	Yield	Comments
Yf	1	Automation & Robotic movements
Yp	0.96	
Ys	0.95	
Ya	1	Modern machining technologies
Yt	1	Modern machining technologies
Y	0.912	Total yield

3.6 Number of chips on wafer

Designers design wafers to have maximum possible chips on it. Grids of chips are superimposed over the wafer, and the radial distance from the center of the wafer to the outermost vertex of each potential chip is computed. Only those chips are counted for which the radial distance is less than the effective radius of the wafer (33). To minimize edge related chip loss, chip fabrication is contained to a circle of radius of 1 to 2 mm less than the actual wafer radius (R_e). By varying the position of the central chip and computing the number of chips per wafer, the chip placement that maximizes the chip count can be determined. A sample calculation for possible number of chips on a wafer is shown in table 20.

For a chip of area (A), number of chips per wafer could be calculated as,

"$N = \pi (R_e - \sqrt{A})^2/A$"

Where,

N = Number of chips per wafer

R_e = Effective radius of wafer

A = Area of the chip (including area required for dicing saw)

Table 20: Sample calculation of number of chips on a 200mm wafer

Chip length	4	mm
Chip width	4	mm
Chip size	16	mm^2
π	3.14	
Radius	98	mm
√ A	4	mm
A	16	mm^2
Chips/wafer	1,734	

3.7 Other indirect processes and systems

Many semiconductor-manufacturing processes produce highly toxic gases and chemicals. Additional input purging and trapping systems are needed to ensure that all of the source gas and chemicals are removed from the system. This gases and chemicals must be processed by burning or by chemical or water scrubbing before being released or drained.

Scrubbed exhaust systems removes any air, which contains vapors from acids and/or caustics, as well as the process gases used in process equipment. The gases leaving a reaction chamber are often toxic, corrosive or flammable and must, therefore, be treated to prevent them from leaving the fab. These gases are treated in post-process, detoxifying chambers. The most commonly used systems are scrubbers and combustion reactors. In most cases, two systems are together with the exhaust of the combustion chamber being fed to a scrubber. This is necessary because gases from a reactor may contain flammable as well as non-flammable gases.

Combustion chambers are either burn boxes or flow reactors, both of which combust flammable gases by reacting them with oxygen. Scrubbers are used to treat the remaining by-products of combustion chambers. Gases are diluted, cooled and made to react in order to eliminate any harmful effects on the environment. Table 21 shows the number of scrubbers required for the CMOS manufacturing sequence. Table 22 shows the total cost of scrubbers.

Process that require scrubbers are (59):

1. Dry Etching
2. Ion Implantation
3. CVD (LPCVD and PECVD)
4. Diffusion

Table 21: Total number of machines that needs scrubber for 11,000 wafers/week

Process	# of m/cs
Deposition	5
Etching	29
Ion Implantation	15
Diffusion	5
Total	54

Table 22: Total cost of scrubbers (59)

	$/mc	# of M/cs	Total
Scrubber	$ 250,000	54	$13,500,000

Designing rules for new semiconductor devices in the nanometer scale demand greater yield under increasingly sophisticated environments. Contamination control is considered to be a critical issue in resolving of such challenges. Cleaning of wafer cassettes, carriers, and boxes becomes essential. Cassette cleaning system costs (CC) around $400,000 for wafer size up to 200mm (61). Cassette costs around $100/piece (60), based on simulation shown below. For 11,000wafers/week we need about 5,000 cassettes annually (including buffer) for production. Table 23 shows total cost of cassettes needed for the CMOS manufacturing fab with a weekly capacity of 11,000wafers/week.

Table 23: Total cost of cassettes

	$/Cassette	# of Cassettes	Total Dollars
Cassettes	$100	5,000	$500,000

Material movement for any semiconductor process is difficult as some process steps are skipped while others are repeated several times. So, to have an optimum layout, equipment is generally in a cell or clustered in one area. To transport wafers in the facility,

overhead loop systems are generally preferred, since they have a much higher throughput and require less floor space. The main purpose of having these automated systems (intrabay-transport systems) is to move wafers between production equipment. The cost of such systems, including installation, is around $10,000,000 (61). Other important costs incurred by semiconductor fab include designing and information system. These CAD systems and large professional information systems, designing costs are very high, about $100,000,000 (61).

Table 24 and table 25 show Other Processes Depreciation (OPD) for both mid year convention with straight line and MACRS depreciation methods.

Table 24: Mid year straight line depreciation for other processes

Other processes	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Scrubber	$1,350,000	$2,700,000	$2,700,000	$2,700,000	$2,700,000	$1,350,000
Cassettes cleaning system	$40,000	$80,000	$80,000	$80,000	$80,000	$40,000
Intrabay handling system	$1,000,000	$2,000,000	$2,000,000	$2,000,000	$2,000,000	$1,000,000
Designing and Information system	$10,000,000	$20,000,000	$20,000,000	$20,000,000	$20,000,000	$10,000,000
Total	$12,390,000	$24,780,000	$24,780,000	$24,780,000	$24,780,000	$12,390,000

Table 25: Mid year MACRS depreciation method for other processes

	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Scrubber	$2,700,000	$4,320,000	$2,592,000	$1,555,200	$1,555,200	$777,600
Cassettes cleaning system	$80,000	$128,000	$76,800	$46,080	$46,080	$23,040
Intrabay handling system	$2,000,000	$3,200,000	$1,920,000	$1,152,000	$1,152,000	$576,000
Designing & Information system	$20,000,000	$32,000,000	$19,200,000	$11,520,000	$11,520,000	$5,760,000
Total	$24,840,000	$39,744,000	$23,846,400	$14,307,840	$14,307,840	$7,153,920

3.8 Overhead and variable costs

3.8.1 Water costs

Large quantities of water are needed during microchip fabrication, mostly for rinsing wafers and wet cleaning and etching. About 1500 gallons of water is consumed in the course of passing a 200mm wafer in 400-step process. Raw water from city contains a lot of unacceptable contaminants including organic material, ionic impurities, gases and bacteria. These contaminants must be removed to make the water suitable for IC processing. It costs the semiconductor industry an average of $0.016/gallon of UPW and $0.003/gallon for water needed for cooling and other purposes (55). Figure 9 below shows the average consumption of water in a semiconductor fab. (55). Table 26 shows Water Cost (WC) spent annually for different types of water.

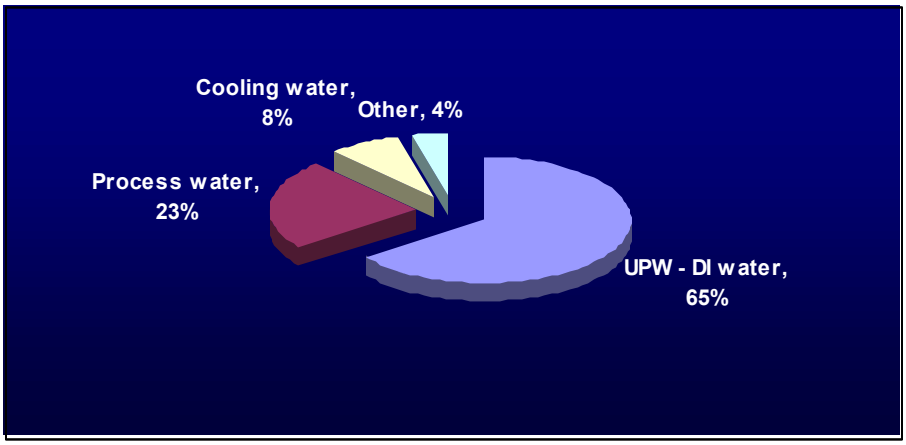


Figure 9: Water uses across a semiconductor fab (55)

Table 26: Annual cost of water for a semiconductor industry

Water type	Gallons/year	$/gallon	Total cost
UPW	792,000,000	$ 0.016	$12,672,000
Cooling process	158,400,000	$ 0.003	$ 475,200
Other process	79,200,000	$ 0.003	$ 237,600

3.8.2 Wafer cost

The size of silicon wafers has been continuously increasing. Larger and larger wafers are used to have an economic impact on reducing cost per chip. In twin well CMOS manufacturing, the starting material is either a p-doped wafer (bulk wafer) or a heavily p-doped wafer (epi wafer) on which a thin, lightly p-doped epi layer is grown.

Lightly p-doped epi layer gives several advantages and is generally preferred:

1. Improved latch up protection
2. Gate oxides with better dielectric reliability
3. Improved gettering capability

Its chief disadvantage is its cost. It costs around $150 compared to $80 for bulk wafer, but it is most commonly used because of the above advantages. Table 27 shows Starting Wafer Costs (SWC) for a semiconductor fab with a full load production capacity of 11,000wafers/week

Table 27: Annual cost for epi wafers for a fab with 11,000-wafer capacity for 50 weeks

	$/wafer	# of wafer/yr	Total cost
Wafer cost	$150	550,000	$82,500,000

3.8.3 Other costs

There are other major variable costs, which play an important role in determining the cost of a microchip.

1. Clean Room Maintenance costs (CRM)
2. Equipment and plant Maintenance Costs (MC)
3. Insurance Costs (IC)
4. Energy Costs (EC)

Performing wafer fabrication processes in clean rooms allows the environment of the wafer to be tightly specified. Many environmental conditions, including, temperature, relative humidity, number of air-borne particles and gases, chemical contamination and vibration, are controlled. Overall, the room is sealed and is supplied with clean air. The annual cost of maintaining a clean room is about $20/sq ft (71). Table 28 shows the total amount of dollars spent to maintain a clean room environment in the fab.

Table 28: Cost of maintaining clean rooms in a semiconductor fab (71)

	$/sq ft	Sq ft	Total cost
Clean room cost	$20	100,000	$2,000,000

Equipment and plant maintenance costs are generally estimated to be about 4% of the total equipment costs (63). Insurance costs for semiconductor industry is estimated to be around 10% of total equipment, fab and building cost. Table 29 shows an estimation of total maintenance costs incurred by a semiconductor fab.

Table 29: Maintenance and Insurance cost relative to equipment cost (63)

Equipment	Cost
Process Equipment cost	$242,670,000
Scrubber	$13,500,000
Cassettes cleaning system	$400,000
Intrabay handling system	$10,000,000
Clean room cost	$435,000,000
Office building cost	$26,390,000
Total cost	$727,960,000
Maintenance cost	$29,118,400
Insurance cost	$72,796,000

The energy consumed to manufacture a complete wafer is 336Kwh/wafer (64). An approximate break down of energy cost for a 200mm facility is given in figure 10 below. Table 30 calculates the annual energy cost incurred for a full load production of semiconductor fab capacity of 11,000wafer/week.

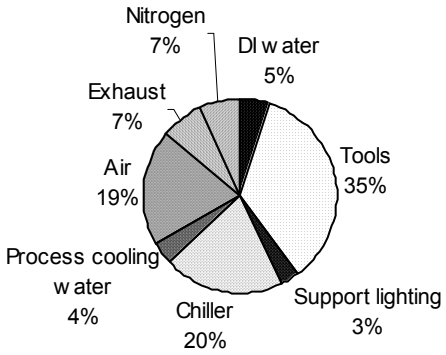


Figure 10: Break down of energy consumption for a semiconductor fab (64)

Table 30: Estimated annual energy cost

Energy consumed/rate	336Kwh/wafer	$0.06kwh
Elec/wafer	$ 20.16	
Annual Electric cost	$ 11,088,000	

3.9 Plant layout

Material movement in a wafer fab is complex. This led semiconductor manufacturing to have a cell or clustered type of layout. There are many reasons for this type of layout.

1. Facility costs are lowered
2. Allows operator specialization with less training

A typical layout of a semiconductor fab is shown in figure 11 below. Assembly line, from wafer sort to packaging is carried outside the main area of fab.

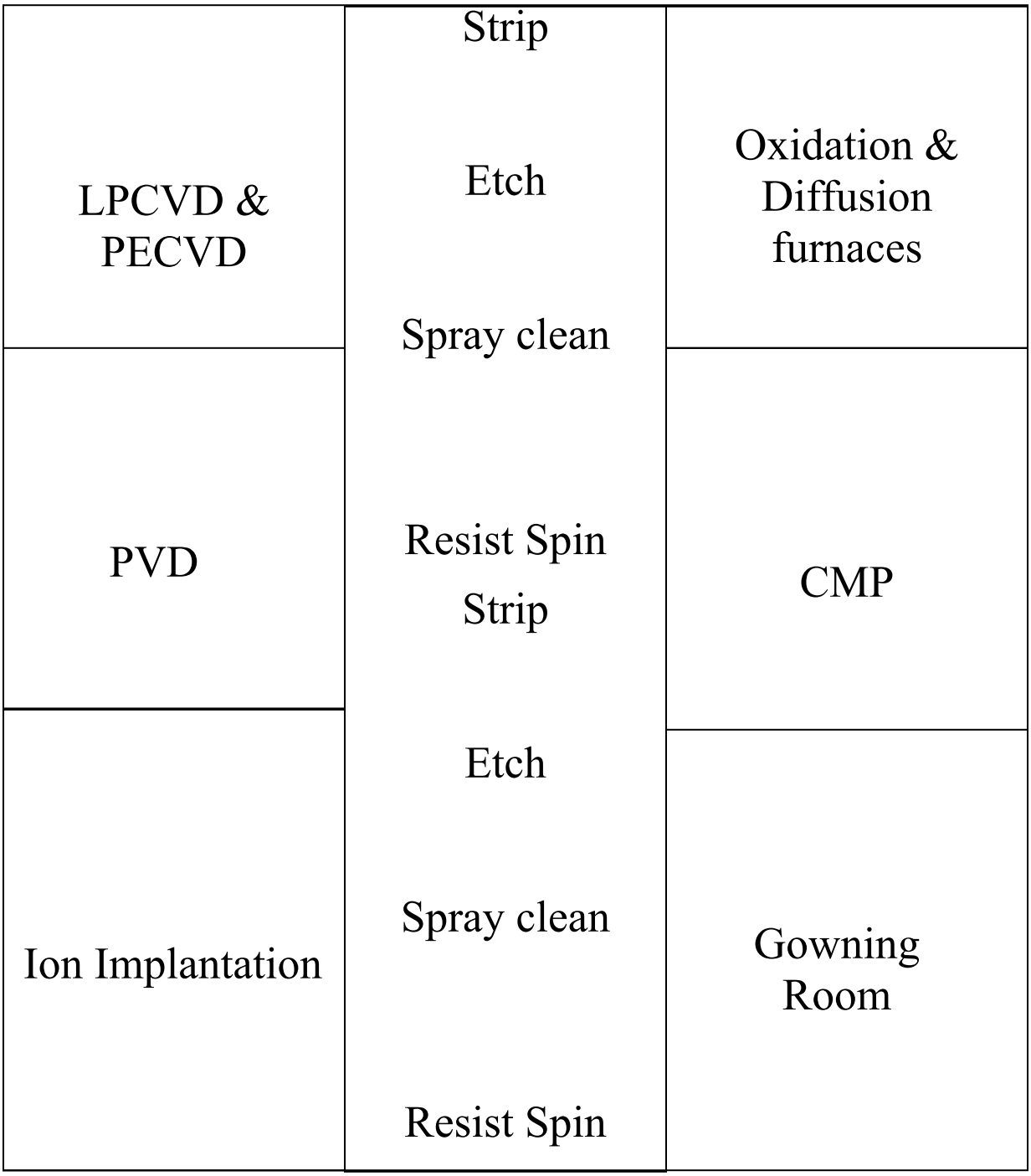


Figure 11: Wafer fab layout

3.10 Indirect labor cost

Indirect Labor Costs (ILC) involves the persons who support production work like managers, supervisors, maintenance, marketing, and engineering. They are essential for any manufacturing industry to be successful. Every industry has its own organizational structure. Organizational structure for the semiconductor industry for a mature product is estimated and shown in table 31 below (73). Table 32 shows annual wages for indirect workers (managers and support staff)

Table 31: Estimated labor needed for semiconductor plant

Job Type	People/shift	Total in 3 shifts	Comments
Dept supervisor	8	16	Each department
Engineering	16	16	Application and design each department
R&D + Planning	20	20	Future research and planning department
Quality control	8	8	To collect data, RCA & control
Marketing/Finance	10	10	
Materials	12	24	Each department direct + other indirect and receiving
Maintenance	16	40	Two people each department
Managers	9	11	Direct reports for each section
Plant Manager	1	1	
Administrative staff	10	10	Support staff

Table 32: Salary for supporting staff in a mature product semiconductor industry

Level	Pay with benefits	# of people	Salary paid
Administrative staff	$100,000	10	$1,000,000
Mid-level managers	$150,000	114	$17,100,000
R&D	$200,000	20	$4,000,000
Managers	$200,000	12	$2,400,000
Total		156	$24,500,000

3.11 Direct labor costs

Direct Labor Costs (DLC) is associated with workers who actually handle the wafers and equipment. A simulation model was run to schedule, assign and estimate the exact number of labor needed for a semi conductor plant. Operators have to load and unload the machine (most of the machines are automated). Some of the other things that an operator has to do are (73):

- Collect data (KeVdata, amp data, etc)
- Set machine for respective process (20nm or 200nm oxide)
- Attend meetings

A simulation model was designed to estimate appropriate amount of labor need for a fab with a capacity of 11,000wafers/week

Assumptions for simulation model:

- 11,000 wafers/week
- Only one product used in simulation
- Load/unload time is 1 min each
- Operator has to collect data (5-15 minutes)
- Fab operates 5 days a week
- Three full shifts a day
- Pre-emp is allow (For scheduling purposes on weekends)
- There is uniform delay for intrabay travel time (2-5 minutes)
- Operator can work on multiple machines
- Wafer cassettes are loaded to the factory after every 100 minutes (to match 11,000/week)
- Number of machines used based on calculations above
- A full cassette of wafers is should be on the machine (25 wafers)
- Only 200mm wafers can be processed.

Need for simulation model:

Computer simulation refers to methods used to imitate a system's operations or characteristics, often over time. A computerized model is needed to understand the behavior of a system for a given set of conditions (74). The purpose of the simulation model is to replicate the scenario of a semiconductor plant and schedule in order to get approximate labor requirement. Running a simulation model helps to understand the flow of the product. It also identifies bottlenecks, critical areas and optimal utilization of resources (equipment and labor both).

Simulation model was run for two different schedules:

- First in first out
- Minimum completion time

Minimum completion time type of scheduling is carried out in most of the semiconductor fabs to achieve higher yields. An attribute was assigned in Arena (simulation software) after every step of a process. This attribute value was increased after every step, which defines the entry to its next step, in turn achieving minimum completion time for the wafer. Many simulation trials were run to acquire an optimum direct labor workforce without sacrificing production. Table 33 below shows number of operators needed to run the plant efficiently. Table 34 gives the annual wages to the operators.

The simulation is a replica for the CMOS manufacturing process and follows the same steps, timings and machines as listed in table 4 and table 8. Simulation is set-up for a production capacity of 11,000wafers/week.

Figure 12 below shows the output of a simulation run (simulation ran in Arena, simulation software) by First In First Out (FIFO) schedule. The extreme left column on figure 12 shows activity areas. This area shows different statistics for all our resources in the system. The adjacent column titled Category Overview gives statistics for different parameters. The major parameters are Entity (Product statistics), Queue (product and

resource statistics combined) and Resource (machine and labor statistics). It shows the number of entities that came in the system (Number of cassettes) as 22,812 and number out as 20,198. So the system processed 22,812 cassettes while 20,198 were finished and 2,614 are in WIP (Work In Process).

Figure 13 shows an Entity statistics for WIP for FIFO schedule run (Work in process). It shows that on an average the process has 1596.74 cassettes (i.e. 39,918 wafers) in inventory. It also shows minimum (242 cassettes) and maximum (2861 cassettes) as inventory for the system.

Figure 14 shows a Queue statistics for number of cassettes waiting for a certain resource for FIFO schedule run. It shows that Deposition mcop1.queue (machine and operator queue) at an average of 16.3336 cassettes with a minimum of 0 cassettes and maximum of 62 cassettes. It means that on an average there are 16 cassettes waiting for a machine and operator.

Figure 15 shows a resource utilization statistics for FIFO schedule run. It shows the average utilization of machines and operators. Ex. Diffusion operator1 is utilized for 0.7495 (i.e. for 74.95% of the time, the operator is busy with loading/unloading or collecting data on the machine).

Figure 16 shows the statistics for minimum completion time (i.e. if the wafer is loaded in the system, the oldest wafer will get the first priority on the machines). The semiconductor industry does that to achieve higher yield. Annual production of the simulation model with minimum completion time schedule is at 19,782 cassettes.

Figure 17 shows entity statistics for minimum completion time. It shows the number of entities that came in the system (Number of cassettes) as 22,812 and number out as 19,782. So the system processed 22,812 cassettes while 19,782 were finished and 3,030 are in WIP (Work In Process).

Figure 18 shows queue statistics for minimum completion time. It shows that Centrifugal washer dryer3.queue (machine queue) at an average of 0.03102 cassettes with a minimum of 0 cassettes and maximum of 3 cassettes. It means that on an average there are 0.03 cassettes waiting for a machine.

Figure 19 shows a resource utilization statistics for minimum completion time. It shows the average utilization for machines and operators. Ex. Diffusion operator1 is utilized for 0.75 (i.e. for 75% of the time the operator is busy with loading/unloading or collecting data on the machine).

When comparing both methods, FIFO and minimum completion time, we find that FIFO has more number of cassettes (416 cassettes, i.e. 10,400 wafers) out compared to minimum completion time.

Table 33: Total number of operator required to run the fab from simulation trials

Process	# of m/cs	Mc/opr	Operator/shift	3 shifts
Cleaning	10	5	2	6
Oxidation	5	2	3	9
Deposition	5	3	2	6
Photolithography	49	13	4	12
Etching	29	10	3	9
Ion Implantation	15	8	2	6
Resist Strip	19	5	4	12
Diffusion	5	5	1	3
Deposition	15	2	8	24
Polarity - CMP	15	8	2	6
Wafer sort - probe	4	1	4	12
Wafer Dicing saw	3	1	3	9
Die bonders	7	1	7	21
Wire bonding	22	3	8	24
Packaging	7	1	7	21
Total				180

Table 34: Approximate annual operator wages to run a fab

	Pay with benefits	# of people	Salary paid
Operators	$120,000	180	$21,600,000

3.12 Chemicals and Material costs

Chemicals and other material costs (MC) are a very small part of the semiconductor industry. They contribute to approximately 10% of the total costs (52) (excluding water & energy costs). Material costs consist of layer materials, chemicals, gases and packaging materials and other indirect materials costs (masks, cleaning chemicals, combustion chamber gases, etc). These costs form a relatively small amount of the total costs.

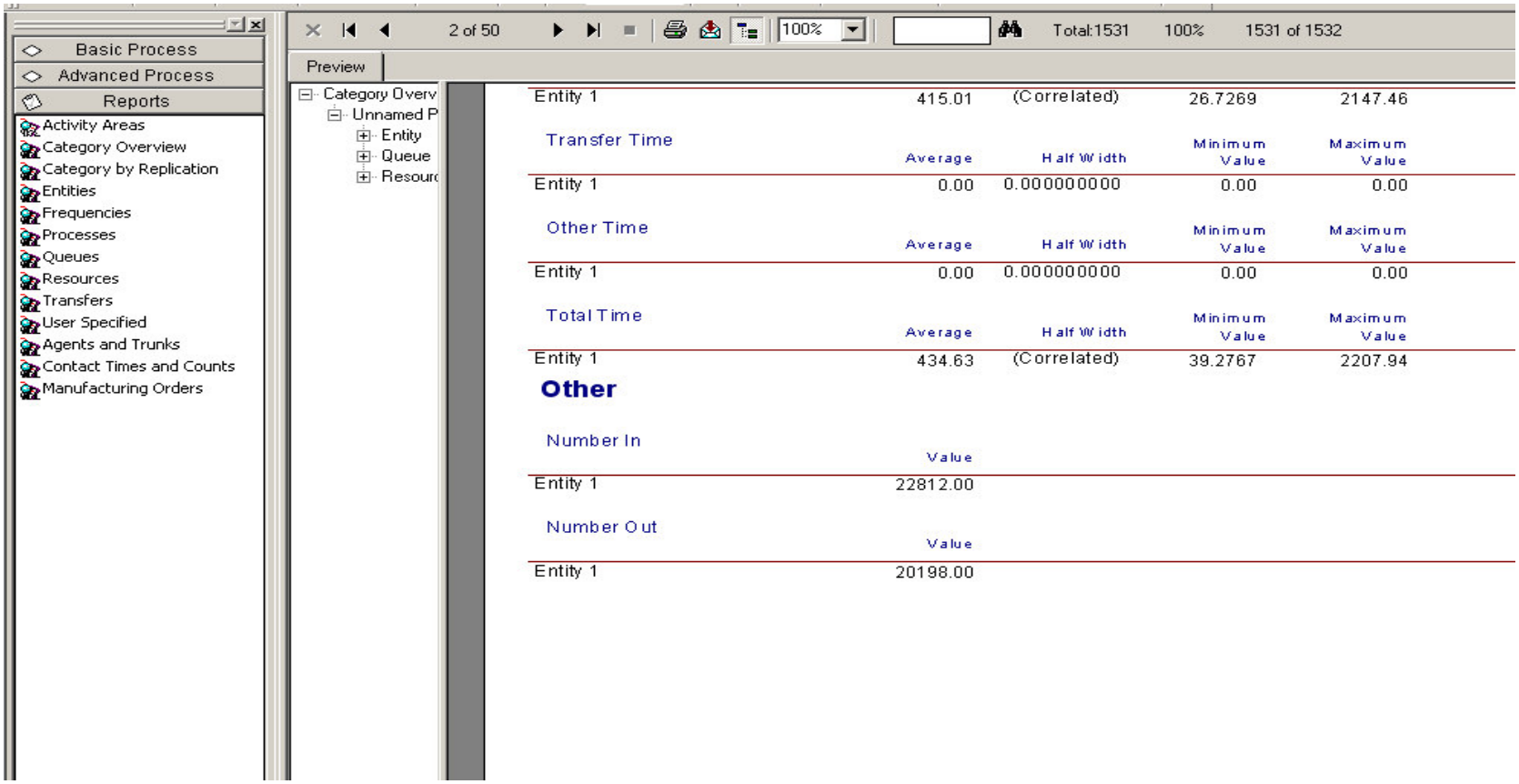


Figure 12: Number of cassettes entered and exited in the system for FIFO (First In First Out) schedule

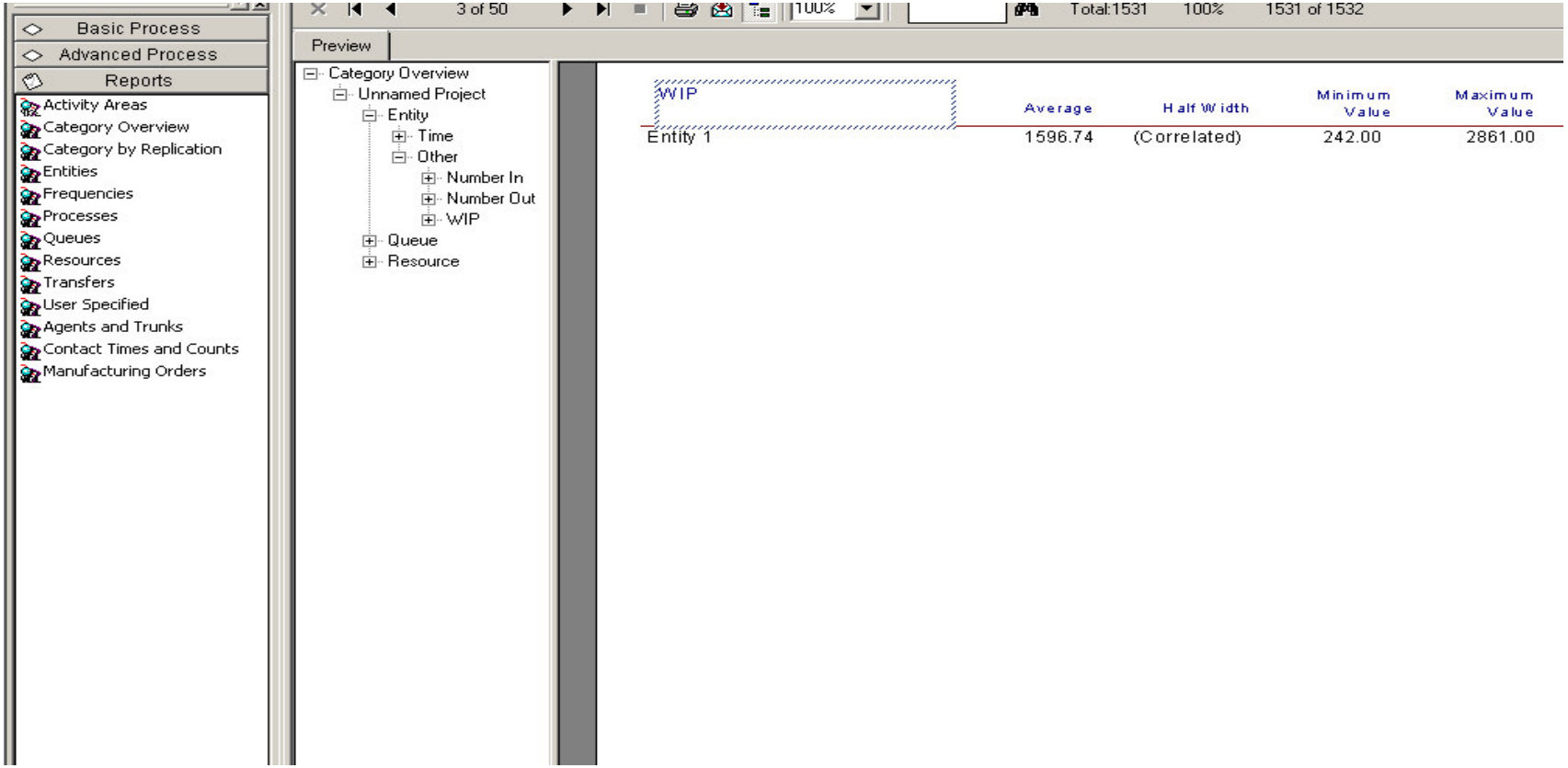
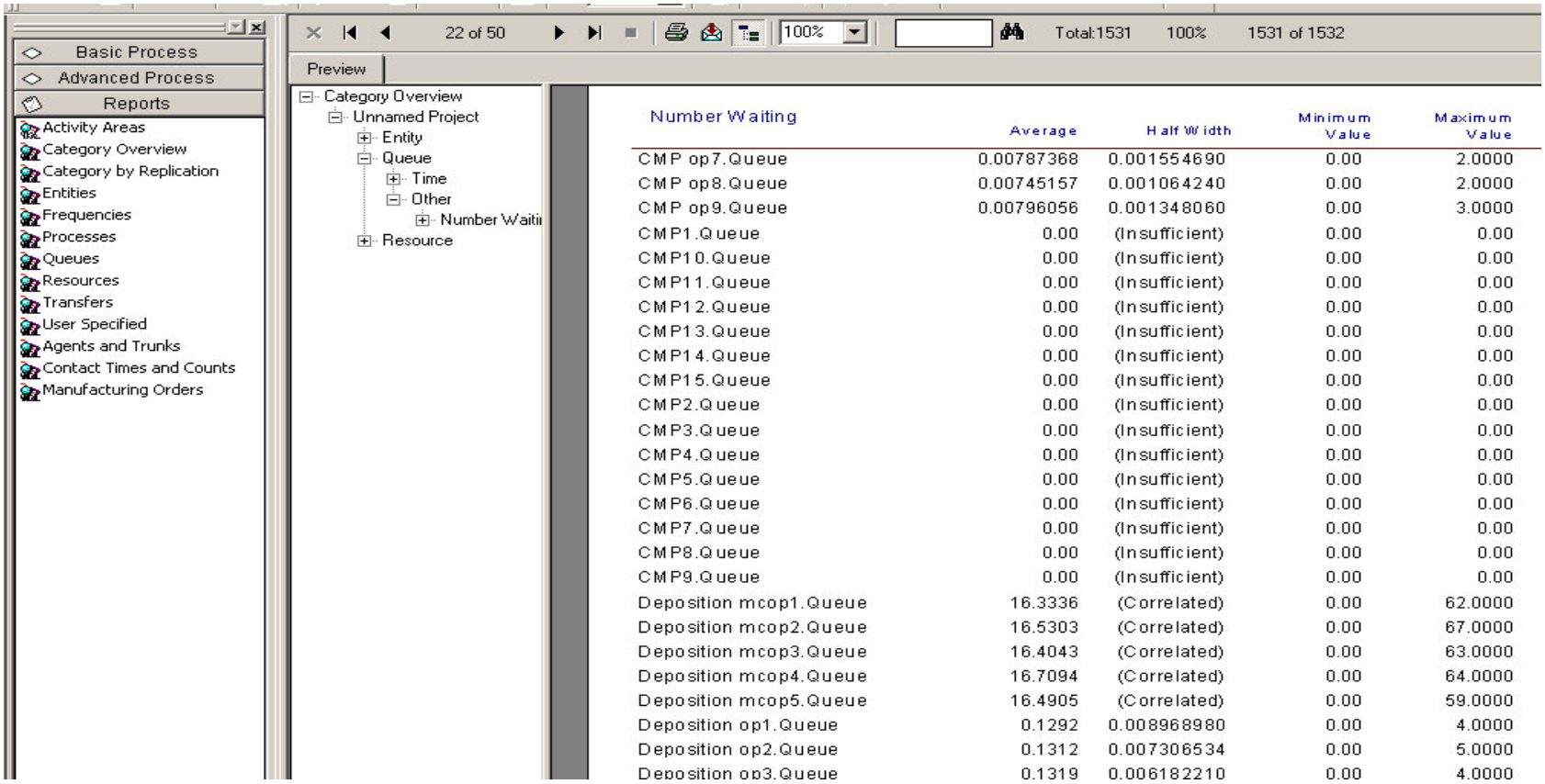


Figure 13: Average inventory in the system by FIFO



Number Waiting

	Average	Half Width	Minimum Value	Maximum Value
CMP op7.Queue	0.00787368	0.001554690	0.00	2.0000
CMP op8.Queue	0.00745157	0.001064240	0.00	2.0000
CMP op9.Queue	0.00796056	0.001348060	0.00	3.0000
CMP1.Queue	0.00	(Insufficient)	0.00	0.00
CMP10.Queue	0.00	(Insufficient)	0.00	0.00
CMP11.Queue	0.00	(Insufficient)	0.00	0.00
CMP12.Queue	0.00	(Insufficient)	0.00	0.00
CMP13.Queue	0.00	(Insufficient)	0.00	0.00
CMP14.Queue	0.00	(Insufficient)	0.00	0.00
CMP15.Queue	0.00	(Insufficient)	0.00	0.00
CMP2.Queue	0.00	(Insufficient)	0.00	0.00
CMP3.Queue	0.00	(Insufficient)	0.00	0.00
CMP4.Queue	0.00	(Insufficient)	0.00	0.00
CMP5.Queue	0.00	(Insufficient)	0.00	0.00
CMP6.Queue	0.00	(Insufficient)	0.00	0.00
CMP7.Queue	0.00	(Insufficient)	0.00	0.00
CMP8.Queue	0.00	(Insufficient)	0.00	0.00
CMP9.Queue	0.00	(Insufficient)	0.00	0.00
Deposition mcop1.Queue	16.3336	(Correlated)	0.00	62.0000
Deposition mcop2.Queue	16.5303	(Correlated)	0.00	67.0000
Deposition mcop3.Queue	16.4043	(Correlated)	0.00	63.0000
Deposition mcop4.Queue	16.7094	(Correlated)	0.00	64.0000
Deposition mcop5.Queue	16.4905	(Correlated)	0.00	59.0000
Deposition op1.Queue	0.1292	0.008968980	0.00	4.0000
Deposition op2.Queue	0.1312	0.007306534	0.00	5.0000
Deposition op3.Queue	0.1319	0.006182210	0.00	4.0000

Figure 14: Wait time for a resource in FIFO (machine and operator)

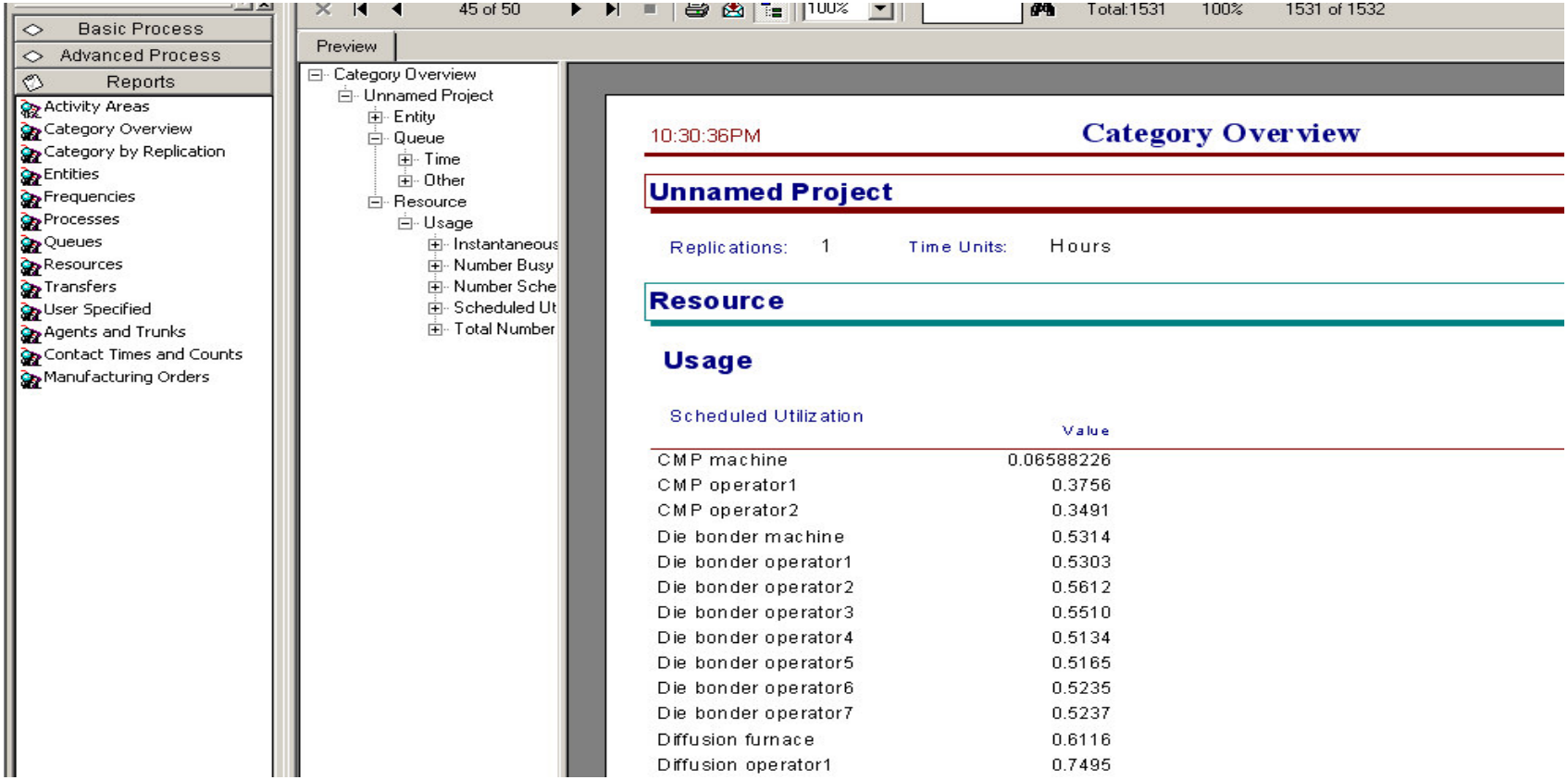


Figure 15: Utilization of machine and operator in FIFO

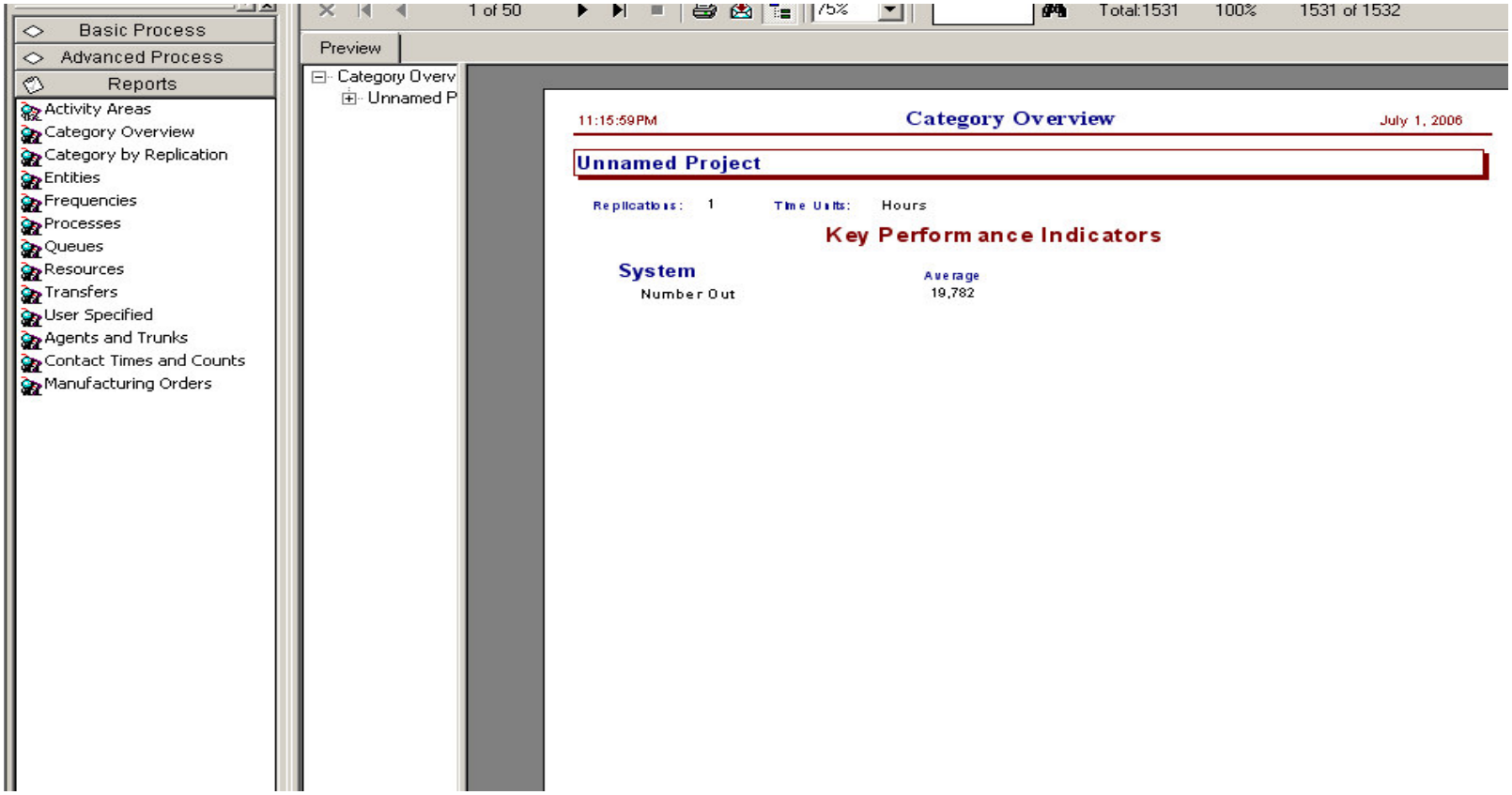


Figure 16: Number of cassettes exited in the system for minimum completion time schedule

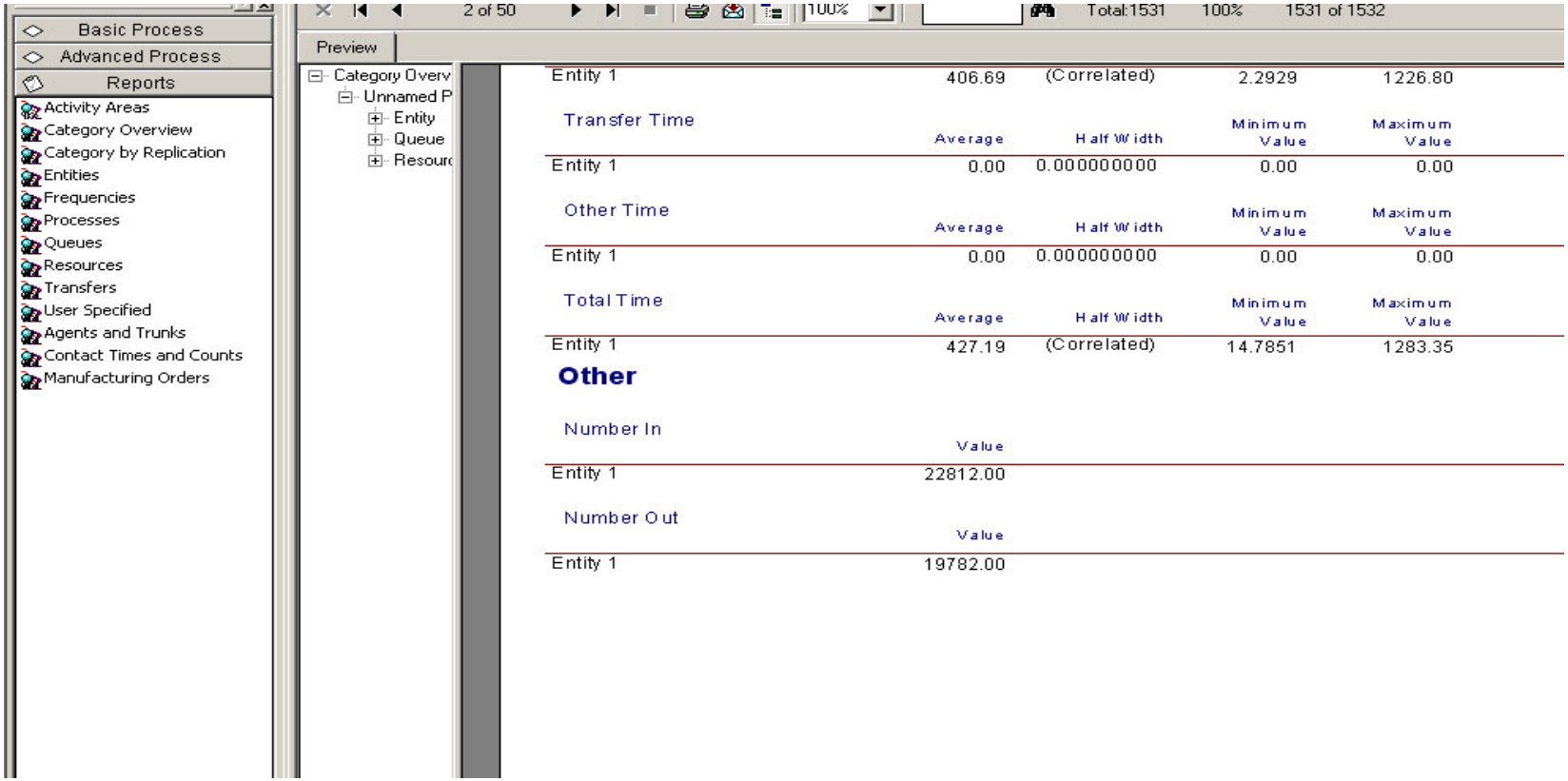


Figure 17: Number of cassettes entered and exited in the system for minimum completion time schedule

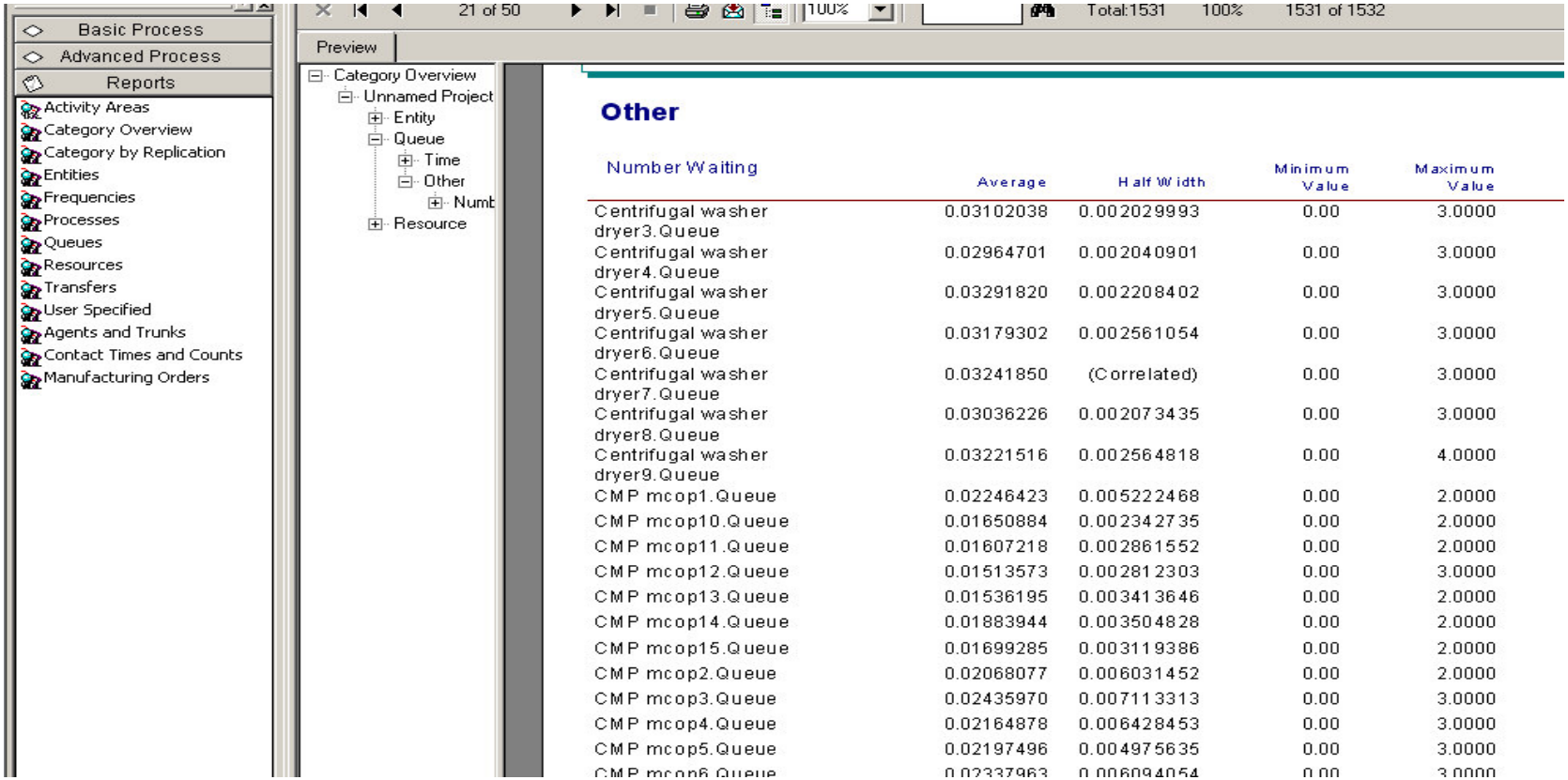


Figure 18: Wait time for a resource in minimum completion time (machine and operator)

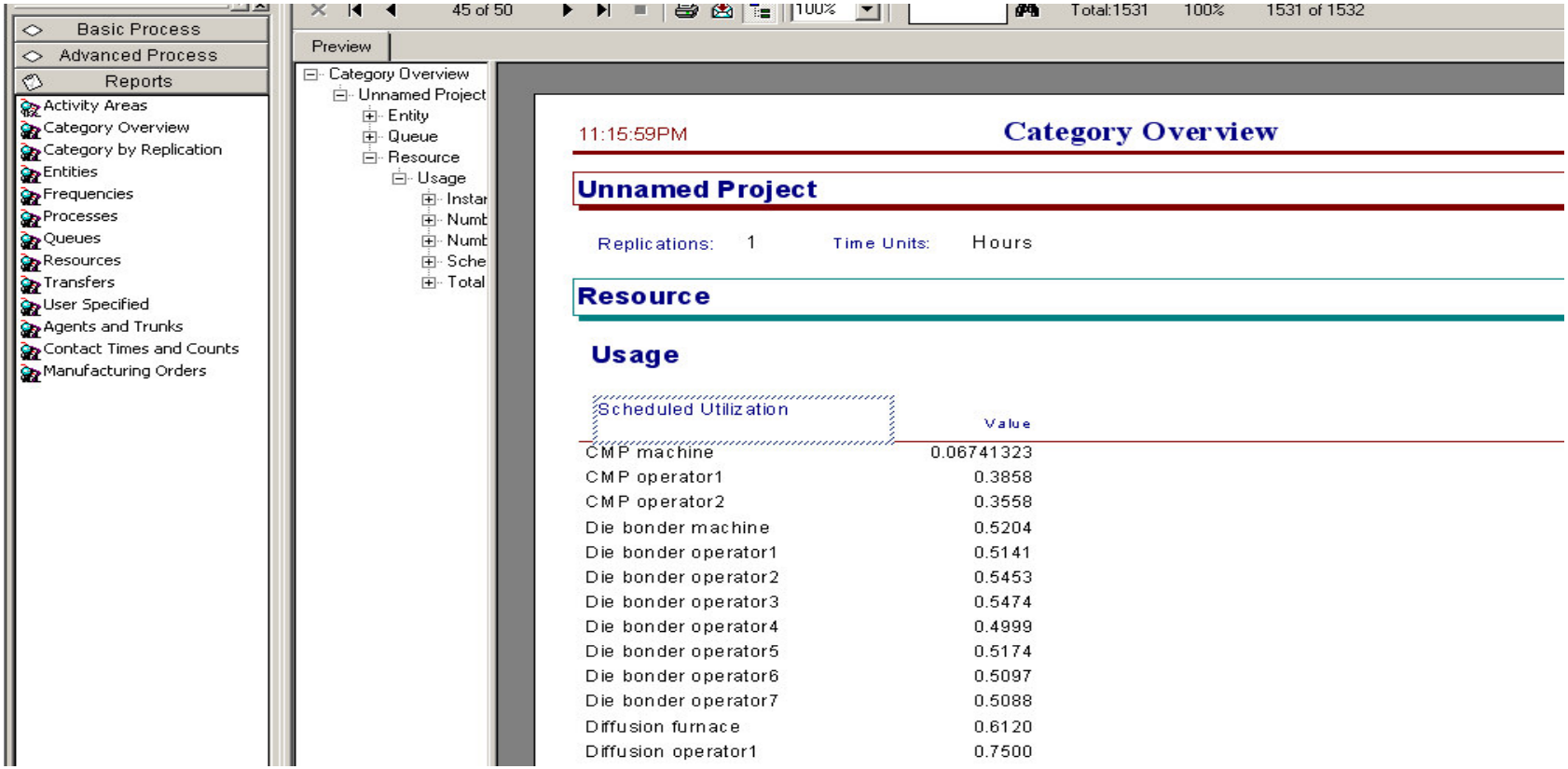


Figure 19: Utilization of machine and operator in minimum completion time

3.13 Calculation and Validation for Cost of Microchip

Table 35 shows the total cost of microchip (It takes in to account all the costs calculated above).

Table 35: Cost of a chip

SL	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Total cost	$339,643,278	$393,189,667	$393,189,667	$393,189,667	$393,189,667	$352,459,667
Cost/chip	$0.67	$0.77	$0.77	$0.77	$0.77	$0.69
MACRS	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6
Total cost	$386,781,472	$453,446,620	$398,543,880	$364,699,962	$362,290,481	$336,625,582
Cost/chip	$0.76	$0.89	$0.78	$0.72	$0.71	$0.66
Average cost/chip		$0.75				

Cost/chip = (ED + FD + OB + OPD + CC + SWC + CRM + MC + IC + WC + EC + ILC + DLC + MC)/ (TNC * AW)

Where,

TC = Total Cost ($393,189,667)

ED = Equipment Depreciation ($48,534,000)

FD = Fab Depreciation ($21,750,000)

OB = Office Building Depreciation ($1,319,000)

OPD = Other Process Depreciation ($24,780,000)

CC = Cassettes Cost ($500,000)

SWC = Starting Wafer Cost ($82,500,000)

CRM = Clean Room Maintenance Cost ($2,000,000)

MC = Maintenance Cost ($29,118,400)

IC = Insurance Cost ($72,796,000)

WC = Water Cost ($13,384,800)

EC = Energy Cost ($11,088,000)

ILC = Indirect Labor Cost ($24,500,000)

DLC = Direct Labor Cost ($21,600,000)

MC = Material Cost (39,318,967)

TNC = Total number of chips (1,184)

AW = Annual number of Wafers (550,000)

TNC = (Number of chips per wafer)/ Yield (925)

A square CMOS chip (4mm x 4mm) made from a 200mm wafer (from bulk wafer to packaged chip) costs 44 cents at 92% yield. The above process was for a two metal layer microchip which are used for simple applications like digital watches, digital display etc. These days complex microchips of about 8-15 metal layers are made for high end devices like multi utility cell phone, high speed computers, defense and space systems, etc. Hardware is then coupled with software to integrate and control the IC functions in electronic products.

The cost of a CMOS chip of size 4.8 x 4.8 mm is published at $1.65 as compared to $0.75 at 78.2% yield by the above calculation and cost formulations (65).

4.0 Conclusion and Future Work

4.1 Conclusion

Semiconductor industries have good productivity due to their technological ability to increase the component count on a chip. It relies on better technologies for being able to reduce the size of the minimum feature dimension on a chip. Semiconductor industry will eventually reach a minimum feature dimension and will need some other methods to achieve productivity and cost reductions. Analyzing costs and calculating cost per component could be considered as the first step to focus on possible cost reductions.

A meaningful manufacturing cost facilitates managerial decisions to enter into a new product line or discontinue the existing product line (if losses are incurred). The key intention of any business is to sell manufactured products and make profits. The above analysis and approach can help semiconductor industries calculate cost for microchips and earn a desired profit. A simulation model of an ideal semiconductor fab will help to accurately calculate and optimize labor & machines needed for production. Cost analysis helps the industry to focus on resource drains and try to control or reduce it. A proper costing technique helps industries sustain competition and gain market share.

Knowing cost of product is a good tool to benchmark the semiconductor fab with competitors. It can help a semiconductor fab catch up with or increase its market share for the specific product line.

4.2 Future work

The above is one of the few steps that have been taken to understand and analyze costs in the semiconductor industry. The industry can exploit many industrial engineering applications to achieve cost reduction. Single wafer production is one of the possible futures for the semiconductor industry. More complicated designs cost analysis, new scheduling techniques, efficient layout and shop floor utilization; lean manufacturing could possibly be other steps that will help achieve higher productivity.

Simulation for multiple product lines in same fab would be an interesting scenario and will replicate actual semiconductor fab operation. As seen from figure 12 to figure 19, better scheduling methods could be developed to optimize the resources and work in process. Having an efficient layout for the plant can play a big role in affecting running costs in a semiconductor industry. Lean manufacturing techniques can be applied to reduce WIP and decrease cycle time.

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Acronyms

CMOS – Complimentary Metal Oxide Semiconductor

MOS – Metal Oxide Semiconductor

Fab - Fabrication

IC – Integrated Circuits

PCB – Printed Circuit Boards

SIA – Semiconductor Industry Association

NIST – National Institute of Semiconductor Technology

VLSI – Very Large Scale Integrated Circuits

ULSI – Ultra Large Scale Integrated Circuits

LOCOS – LOCal Oxidation of Silicon

CMP – Chemical Mechanical Polishing

CVD – Chemical Vapor Deposition

LPCVD – Low Pressure Chemical Vapor Deposition

PECVD – Plasma Enhanced Chemical Vapor Deposition

FIFO – First In First Out