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Measuring Dynamic Capabilities: Practices and Performance in Semiconductor Manufacturing

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Research on dynamic capabilities emphasizes the importance and role of organizational routines in explaining interfirm differences in performance. While performance differences are well documented, few empirical analyses explore the processes inside organizations that lead to dynamic capabilities or attempt to define and measure their performance effects. This paper examines one type of dynamic capability – the development and introduction of new process technologies in semiconductor manufacturing. This dynamic capability is an important source of competitiveness in the semiconductor industry, given the short product lifecycles, rapid price declines, and rapid technological advances that define the industry. Because much of the knowledge that underpins semiconductor manufacturing is idiosyncratic, firm-level R&D organization and information technology practices that facilitate problem solving and learning-based improvement provide important and enduring advantages. We derive models of the rate of improvement in manufacturing yield (i.e. the quality of production) and cycle time (i.e. the speed of production) following the development and introduction of new process technologies in manufacturing facilities, and test the empirical specifications of these models. The ways in which semiconductor manufacturers accumulate experience and articulate and codify knowledge within the manufacturing environment build new process development and introduction dynamic capabilities that improve performance.

Introduction

An extensive literature considers the role of dynamic capabilities in firm strategy and performance (Helfat *et al.*, 2007). Teece, Pisano and Shuen (1997) argue that dynamic capabilities enable organizations to renew competencies and to strategically manage the internal and external organizational skills, routines and resources required to maintain performance in the face of changing business conditions. Similar definitions are provided by Eisenhardt and Martin (2000) and Winter (2003). Significant conceptual and theoretical progress has been made in the field of dynamic capabilities in understanding the bases for sustained competitiveness within fast-moving business landscapes. Nonetheless, few empirical analyses have explored the processes inside organizations that lead to dynamic capabilities or attempted to define and measure their performance effects.

This paper provides an empirical analysis of one type of dynamic capability – the speed and

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effectiveness with which firms develop and introduce new process technologies into semiconductor manufacturing. The semiconductor industry represents an ideal setting to examine dynamic capabilities, given the rapid technological advancement, short product lifecycles and fast price declines that define it. Because new semiconductor products normally require new manufacturing processes, the development and introduction of new process technologies is paramount for sustained competitive performance.

Our theoretical approach draws mainly on Zollo and Winter (2002), who underscore the importance of deliberate learning mechanisms, such as organizational routines related to experience accumulation, knowledge articulation and knowledge codification, in the development of dynamic capabilities. The nature of our data allows us not only to measure the learning mechanisms inside manufacturing facilities that build new process development and introduction dynamic capabilities, but also to determine the performance effects of dynamic capabilities.

We make several contributions to the literature. Our empirical analysis develops and tests the performance consequences of firm-specific routines in new process development and introduction, an important class of the dynamic capabilities highlighted by Teece, Pisano and Shuen (1997) and Zollo and Winter (2002). We provide evidence that dynamic capabilities develop and build from organizational routines that support experience accumulation, knowledge articulation and knowledge codification. We also demonstrate that organizational routines have static and dynamic effects on performance, and their implementation may involve tradeoffs between these classes of performance benefit. We find that the enduring nature of inter-organizational differences in the extent and use of these organizational routines suggests that competitive advantage created from dynamic capabilities is enduring and inimitable. Overall, our paper is distinguished by its focus on dynamic capabilities and serves as an example of how to examine empirically the dynamic capabilities concept.

We also contribute to the literature on the management of new product and process development. Although new product development has been extensively examined in the management of innovation literature (Clark and Fujimoto, 1991), new process development has received far less attention but nevertheless represents an important dimension of performance in many high-technology industries. Our empirical approach draws on Hatch and Mowery (1998) and Macher and Mowery (2003), who show that manufacturing performance improvements are driven in part by practices that improve the analysis of production volume, and complements research that examines the sources of 'learning before doing' and 'learning by doing' (Pisano, 1996). We underscore the contributions of R&D organization and information technology (IT) practices to problem solving in new process development and introduction (Iansiti, 1995; West and Iansiti, 2003). Finally, we add to the small number of empirical studies that examine the performance implications of IT implementation at the process (as opposed to the firm) level (Ashworth, Mukhopadhyah and Argote, 2004; Mukhopadhyah, Rajiv and Srinivasan, 1997).

The next section surveys the theoretical and empirical research in the dynamic capabilities literature. Then hypotheses are developed around the influence of deliberate routines on new process development and introduction dynamic capabilities in semiconductor manufacturing. An empirical model of problem solving, learning and performance in semiconductor manufacturing is then developed. This section also describes the data sources and characteristics, the variable construction, and the estimation methodology used in the empirical analysis. In the penultimate section the empirical results are presented and discussed, and the final section concludes.

Theory

Dynamic capabilities research is rooted in the resource-based view (RBV) of the firm. This perspective conceptualizes organizations as collections of difficult-to-imitate resources that create competitive advantage and contribute to sustained interfirm performance differences (Hoopes, Madsen and Walter, 2003). The RBV was developed by Barney (1986, 1991), Peteraf (1993) and Wernerfelt (1984), and further extended by Helfat and Peteraf (2003) and Mahoney and Pandian (1992), among others. Dynamic capabilities extend the RBV by examining the sources of competitive advantage in rapidly changing markets, and refer to firms' abilities to

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'integrate, build, and reconfigure internal and external competencies to address rapidly changing environments' (Teece, Pisano and Shuen, 1997, p. 516). Dynamic capabilities include strategic and organizational processes (Nelson and Winter, 1982), such as product development, alliance formation and strategic decision making, that are deeply embedded in firms (Eisenhardt and Martin, 2000). The RBV and dynamic capabilities approaches are seen largely as overlapping, as opposed to separable, frameworks (Helfat and Peteraf, 2003).

Dynamic capabilities have been the focus of a large theoretical and conceptual literature, but few empirical analyses have explored the processes inside organizations that lead to dynamic capabilities or have attempted to define and measure their performance effects. A related research stream that examines the emergence, development and performance implications of firm capabilities has seen increased empirical support (Helfat, 2000; Hoopes, Madsen and Walter, 2003). Early empirical studies within this research stream document significant and persistent differences among firms in new product development (Leonard-Barton, 1992) and R&D productivity (Henderson and Cockburn, 1994) performance, but proved less successful in explaining the sources of these differences. More recent empirical research examines the importance of initial interfirm differences (Cockburn, Henderson and Stern, 2000), deliberate learning mechanisms (Zollo and Singh, 2004), managerial cognition and inertia (Tripsas and Gavetti, 2000), managerial human and social capital (Adner and Helfat, 2003), human capital selection, training and deployment (Hatch and Dyer, 2004) and customer and project management investment (Ethiraj *et al.*, 2005) in determining firm capabilities and performance. Related empirical research in product development (Clark and Fujimoto, 1991), process development (Iansiti, 1995; Pisano, 1994, 1996) and operations strategy (Hayes, Pisano and Upton, 1996; Hayes, Wheelwright and Clark, 1988) does not adopt a capability-based approach *per se*, but does analyse the influence of firms' managerial and organizational practices on firm capabilities and performance. Our study builds on these research streams by constructing disaggregated and context-specific measures, linking these measures to organizational routines that build dynamic capabilities, and testing the effects of these measures on firm performance.

Although the dynamic capabilities literature argues that they are rooted in organizational practices, the nature of these 'foundational' routines has received less attention. Zollo and Winter (2002) suggest that dynamic capabilities are 'learned and stable pattern[s] of collective activity through which the organization systematically generates and modifies its operating routines in pursuit of improved effectiveness' (Zollo and Winter, 2002, p. 340). Dynamic capabilities build through organizational processes of experience accumulation, knowledge articulation and knowledge codification. Operating routines develop through the accumulation of experience as a result of the repeated execution of similar tasks (Argote, 1999). Knowledge articulation is the process by which organizations determine what works (and what does not) in the execution of organizational tasks (Levinthal and March, 1993) and communicate this implicit information throughout the organization. Knowledge codification documents understanding of the performance implications of operational routines (i.e. through manuals, blueprints, IT etc.), facilitates the diffusion of existing knowledge, and improves the coordination and implementation of complex activities (Nonaka, 1994; Winter, 1987; Zander and Kogut, 1995). Organizational performance improves as causal linkages between actions and performance are established, become better understood, and eventually are embedded within the organization. The extent of knowledge articulation and knowledge codification within an organization thus reflects managerial decisions and strategies, rather than being solely determined by the knowledge environment.

Hypotheses

Knowledge articulation in process development

Knowledge articulation is the process by which organizations determine the effectiveness of particular organizational approaches and communicate this information throughout the organization (Levinthal and March, 1993; Zollo and Winter, 2002). We argue that two approaches facilitate the articulation of knowledge within the organization: (1) the use of functionally diverse teams (work groups); and (2) the co-location of development and manufacturing personnel.

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Performance in knowledge-intensive activities improves as the causal links between performance and individual or group actions are established and practices based on recognition of these links are embedded within the organization (Zollo and Winter, 2002). One means to achieve this goal is through the use of functionally diverse teams. A substantial literature on the contributions of team diversity to performance reaches varied conclusions (Williams and O'Reilly, 1998), partly due to definitional differences. When defined in terms of functional composition, team diversity is generally found to increase the information available. This additional information is especially advantageous when new approaches or multiple perspectives are important in problem solving. Higher levels of functional diversity within teams also provide additional knowledge, skill sets and potentially important contacts that enhance problem-solving efforts (Ancona and Caldwell, 1992; Bantel and Jackson, 1989). Both the amount and the richness of information available to organizations increase through more functionally diverse teams. In complex R&D environments, where gaining understanding of (tacit) information is critical, functionally diverse teams provide problem-solving advantages.

Greater functional diversity within a team can increase intra-team conflict (Jehn, Northcraft and Neale, 1999; Pelled, Eisenhardt and Xin, 1999) and lead to coordination difficulties, but the increased knowledge accessible both within (Glick, Miller and Huber, 1993) and outside of (Ancona and Caldwell, 1992) the team from greater functional diversity provides more salient advantages. Functional diversity has been shown to increase administrative innovation in banking (Bantel and Jackson, 1989), increase firm growth in the semiconductor industry (Eisenhardt and Schoonhoven, 1990) and improve organizational responsiveness to environmental shifts (Keck and Tushman, 1993). Studies in new product development similarly find that cross-functional teams improve the coordination and dissemination of organizational learning (Ancona, 1990; Nonaka, 1991; Tushman, 1977) and accelerate process development (Denison, Hart and Kahn, 1996).

In the context of process technology development and introduction in semiconductor manufacturing, functionally diverse teams are especially important for problem solving. The development and introduction of new process technologies involves both the exploitation and intrafirm transfer of tacit knowledge. For example, a common problem is the transfer of new process technologies from development (pilot) facilities to the full-volume commercial production facilities. Manufacturing problems arise only after new process technologies have been transferred, not only because of differences in equipment, production volumes and worker skills, but also because of tacit know-how. To partially address the challenges of intrafirm tacit knowledge transfer, Intel utilizes a 'copy exactly' approach, whereby everything (e.g. methodologies, process flows, equipment sets, suppliers, clean rooms) in the development facility is exactly duplicated in the commercial production facility. Cross-functional teams of operators, technicians and engineers that span product design, process development and manufacturing are another R&D organization practice that helps address these knowledge transfer challenges by improving communication, increasing information availability and facilitating integration. These organizational approaches support the earlier identification of problems and the faster implementation of corrective solutions. Greater functional diversity within teams is therefore a primary mechanism for knowledge articulation within manufacturing facilities, which motivates our first hypothesis.

> *H1a:* Greater functional diversity within teams employed in problem-solving activities improves learning and problem-solving performance.

Closely related to functional diversity within particular teams (e.g. intra-team diversity) is diversity in the types of teams (e.g. inter-team diversity) operating throughout the organization. Some teams are able to address complex tasks and problems that span functional boundaries (Ancona and Caldwell, 1992), while other teams are better suited to more narrowly defined tasks or problem solving within a particular functional area. We argue that diversity of the types of teams assigned to particular tasks aids organizations in developing effective new process development and introduction dynamic capabilities. Inter-team diversity increases variance and builds experience in the types of problems that organizations face and eventually solve, both within and across several functional areas (Bailey, 1998). The problem-solving practices developed in one functional area can be refined and

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applied to the practices in other functional areas. Inter-team diversity thus provides problem-solving benefits via economies of specialization and economies of scope. Greater diversity in the types of problems encountered by teams spread across functional areas also produces additional information. If this information is exchanged between and among teams, organizations accumulate experience more quickly and are able to move down the problem-solving 'learning curve' faster.

Semiconductor firms must make decisions regarding not only the number of teams operating within the manufacturing facility, but also the assignment of individual team tasks. We argue that a more important factor than the number of teams is how functional responsibilities are assigned. Semiconductor manufacturers that have the 'right' number of teams examining the 'right' number of functional areas can more effectively articulate knowledge important for problem solving related to new process development and introduction. Several different kinds of teams are utilized in semiconductor manufacturing facilities, including total quality management teams, quality improvement teams, cycle time reduction teams, process improvement teams, *ad hoc* 'special project' teams, self-directed work groups, among others. Teams organized to examine specific functional areas build problem-solving competence and develop useful information within these areas, which can then be disseminated to other functional areas. Organizations that are more diverse in the tasks, roles and assignments of teams across specific functional areas can solve more problems more quickly. This R&D organization practice develops new process development and introduction dynamic capabilities, which results in superior overall manufacturing performance. We therefore examine the following hypothesis.

> *H1b*: Greater functional diversity across team types employed in problem-solving activities improves learning and problem-solving performance.

A second common R&D organization practice important to firms' new process development and introduction dynamic capabilities is the co-location of development and manufacturing personnel. Co-location improves coordination between design and manufacturing through techniques such as employee rotations and temporary personnel transfers (Clark and Fujimoto, 1991). For instance, development engineers move with a new manufacturing process from the development facility, helping to install and 'debug' it in the full-volume commercial production facility, while manufacturing engineers participate in new process technology development.

Co-location facilitates the articulation of knowledge related to problem solving by reducing communication barriers in the organization (van den Bulte and Moenaert, 1998). The co-location of development and manufacturing personnel also simplifies intrafirm knowledge transfer (Hayes, Pisano and Upton, 1996; Iansiti, 1995), especially for tacit information that is difficult to transfer without face-to-face communication, and saves time by supporting accurate and timely identification of design and manufacturability problems (Cordero, 1991; Smith and Reinertsen, 1991; Zirger and Hartely, 1996). Finally, co-location achieves greater coordination and integration between product planning, process design and manufacturing that facilitates both the requirements of new products and processes and the interrelationships and inherent tradeoffs among these requirements (Ettlie, 1995). Co-location is thus one way that organizations can facilitate the articulation of (especially tacit) knowledge between development and manufacturing, thereby accelerating problem solving.

In semiconductor manufacturing, co-location improves communication between development and manufacturing personnel in new process technology development and introduction (Macher and Mowery, 2003). Development personnel gain complete and timely information on the unique requirements of the full-volume production facility while manufacturing personnel are less likely to repeat the same mistakes, not least because of the advantages of face-to-face communication of otherwise tacit information. The expected benefits of co-location for problem-solving performance results in the following hypothesis.

> *H2*: The co-location of a greater number of development and manufacturing personnel improves learning and problem-solving performance.

Knowledge codification in process development

Knowledge codification is the process by which organizations document understanding of the effectiveness of specific practices. Codification

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facilitates the identification of causal connections between practices and performance, and supports the diffusion of this information within the organization (Zollo and Winter, 2002). The extensive use of IT for data collection and performance monitoring is one mechanism for knowledge codification related to problem solving important to new process development and introduction.

Support for these arguments comes mainly from research that examines the returns to investments in and business value of IT. We follow Ashworth, Mukhopadhyah and Argote (2004) in analysing the contributions of IT deployment to improved performance in the key business processes most important for performance in new process development and introduction (i.e. a 'process-level' analysis of the effects of IT). The limited research on IT business process implementation highlights its contribution to performance through improved problem solving, work coordination, administration and management, and knowledge sharing. Mukhopadhyah, Rajiv and Srinivasan (1997) find that IT implementation improves both the quality and output of mail sorting, in comparison to mechanical technologies. Mukhopadhyah and Kekre (2002) find similar benefits from the adoption of electronic data interchange for order-processing cycles by suppliers and customers. Related research examines the effects of technology on organizations' abilities to learn through experience-based productivity improvement (Adler, 1990; Huber, 1991). Although IT facilitates the capture, retrieval and sharing of knowledge and information (Argote, Beckman and Epple, 1990), it also must enhance problem solving if it is to improve productivity (Boone and Ganeshan, 2001; Williams and Kotnour, 1993). IT investment may also yield performance benefits through its contributions to the codification and capture of knowledge accumulated through historical production experience (Ashworth, Mukhopadhyah and Argote, 2004).

The increasing complexity of semiconductor manufacturing has made investment in and implementation of IT requirements for effective new process development and introduction. One central IT application is in the automated 'handling' of information within the manufacturing facility. Higher levels of information handling automation facilitate the codification of knowledge. More systematic and reliable collection of manufacturing performance data enables faster identification and diagnosis of processing problems. Automated downloads of process 'recipes' into manufacturing equipment and computerized 'sanity checks' (verifying that processing steps are correct for a specific lot) remove important sources of operator error. Higher levels of information handling automation also accelerate organizational learning because information is more readily captured, retrieved and shared throughout the manufacturing facility. Advanced information handling applications collect computerized records of wafer lots in integrated databases as they progress through the production facility. Statistical analyses of these databases enable engineers to more accurately set process parameter windows and identify areas on which to focus problem-solving efforts aimed at improving yield and/or cycle time. We therefore examine the following hypothesis.

H3: More extensive deployment of IT improves learning and problem-solving performance.

Empirical model

Performance and learning in semiconductor manufacturing

A semiconductor is any microelectronic device fabricated on 'semiconducting' material (usually silicon), but is normally a set of interconnected electronic components (i.e. integrated circuit) that perform a particular function. New semiconductor products usually require significant changes in underlying manufacturing processes. Manufacturing a semiconductor consists of constructing layers of conducting and insulating materials on silicon 'wafers' in intricate patterns that give the integrated circuit its function. Wafer fabrication is characterized by a series of complex process steps, where each 'ingredient' in the process 'recipe' must be applied within a certain range to produce the desired effect.[1]

[1]A 'recipe' is a codified description of the ingredients, process steps, and machine and equipment operations involved in making a semiconductor product. Many process steps are too complex to identify the optimal ranges for all the ingredients through physics and engineering. Unexpected interactions between and among any of the process steps, ingredients or machine operations also can destroy the functionality of the die.

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New process development and introduction is important to competitive performance in the industry for several reasons. First, because new technological generations are frequent in occurrence, experiential advantages in working with a given production technology become rapidly obsolete (Cabral and Leiblein, 2001). Semiconductor firms must invest continuously in new process development and introduction to maintain competitive parity. Second, the ability to increase the production output of new semiconductor products rapidly, before imitators enter, is crucial to profitability. Semiconductors are characterized by price declines of 25%–30% per year (Smith and Reinertsen, 1991) and product lifecycles measured in months. Third, the high fixed costs associated with semiconductor manufacturing – new manufacturing facilities cost between \$2 and \$3 billion and are considered 'state-of-the-art' for no more than three years (ICE, 2001) – mean that poorly managed manufacturing environments increase costs and reduce profitability.

Yield is an important component of semiconductor manufacturing performance (Appleyard and Brown, 2001; Hatch and Mowery, 1998) and is generally expressed in terms of line yield (the proportion of wafers entering the production process that are not scrapped) and die yield (the proportion of dies on a successfully processed wafer that pass functionality tests). Common causes of line yield losses include broken or damaged wafers and skipped production process steps that render all of the integrated circuits on a wafer non-functional. Die yield losses are due either to random particles or to parametric processing problems. Semiconductor manufacturing facilities use extensive air filtration systems and protective enclosures for equipment and wafers to reduce airborne particles and create ultra-clean environments. A more pervasive source of die yield losses is parametric problems that result from insufficient control of the production process or incomplete understanding of the process technology parameters, due to inferior materials, equipment failures or processing errors.

Cycle time is an equally important component of manufacturing performance (Macher and Mowery, 2003). We measure cycle time from the 'start' of a wafer through the manufacturing facility to the emergence of a completed integrated circuit. Shorter cycle times enable semiconductor manufacturers to increase output quickly and to respond rapidly to customer and market demand changes. Cycle time problems result from poorly designed process recipes or from process changes that are not optimized or produce unanticipated consequences.

Because many process steps are neither well understood nor easily replicated on different equipment sets or in different production facilities, improving manufacturing performance depends on knowledge that is accumulated through experimentation and experience. Knowledge gained from these activities yields tighter process specification limits and parameters. The widespread application of such knowledge, especially in different manufacturing facilities, often requires its articulation and codification throughout the firm. Specific R&D organization and IT practices within the manufacturing facility can improve new process development and introduction capability. These practices bring more information to bear on problem-solving activities, improving identification of the sources of yield losses or cycle time excursions and supporting faster implementation of corrective solutions.

Learning and problem solving in semiconductor manufacturing

The speed and quality of problem solving are fundamental drivers of new process development and introduction performance within semiconductor manufacturing (Appleyard, Brown and Sattler, 2006). Our approach draws on Hatch and Mowery (1998) and Macher and Mowery (2003), who show that improvements in manufacturing performance are driven in part by practices that improve engineers' analysis of production problems. We extend and differentiate our approach from these other papers in several ways. We utilize two measures of manufacturing performance in our empirical analysis. The first is the rate of improvement in yield (i.e. the *quality* of production processes) following the introduction of a new process technology into a production facility. The second is the rate of improvement in cycle time (i.e. the *speed* of production) for this new process technology following its introduction. We also develop and test the influence on manufacturing performance of a broader set of measures of firms' R&D organization and IT practices, using a principal components analysis approach. We provide useful and more detailed

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insights as to how these practices translate into improved performance.

The traditional model for learning by doing is embodied in the following equation:

$$C_N = C_1 N^{-\lambda} \tag{1}$$

where C_N is the cost of the Nth unit produced, N is the cumulative amount produced, and C_1 is the cost of the first unit produced. This formulation models learning as a function of cumulative volume, but a variety of other measures of 'experience' have been used in other studies. Surprisingly, however, the influence on learning of deliberate actions aimed at overcoming sources of productivity bottlenecks has received more limited attention (Adler and Clark, 1991; Argote, 1999). Firms acquire process-specific knowledge through engineering analysis of manufacturing output to identify and eliminate sources of yield loss or cycle time excursions. Cumulative learning thus is affected by cumulative volume, measured in terms of wafers manufactured for a particular process. Denoting cumulative volume at time t as CV_t, the 'learning index' for a manufacturing process is defined as

$$L_t = \beta_1 \mathrm{CV}_t + L_0 \tag{2}$$

where L_0 is the level of knowledge in the initial period. In order to link learning to specific manufacturing performance measures, we assume that the learning curves for defect density and cycle time, respectively, are additively separable into static and dynamic (learning by doing) components:

$$P_t = h_1(L_t) + h_2(\cdot) \tag{3}$$

where P_t represents either defect density or cycle time and L_t is the unobservable 'learning index' defined in equation (2). The second term in equation (3) includes the influence of variables that do not directly affect the rate of learning but index the underlying technological 'difficulty' of the manufacturing process and the associated learning-based improvements in it. Among these static variables are the linewidth of the manufacturing process (LW), the wafer size (WS), the clean room grade (CR) and the number of mask layers (ML), which we detail below.

Neither economics nor engineering provide insights into the appropriate functional forms for our dynamic and static components of learning (Yelle, 1979). We therefore specify functional forms for the $h_2(\cdot)$ and $h_1(L_t)$ components of learning as follows:

$$h_1(L_t) = \gamma + \psi \mathrm{e}^{-\delta L_t} \tag{4}$$

$$h_2(\cdot) = \beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML} \tag{5}$$

Note that $h_1(L_t)$ allows for both shifts in rate of learning through γ and scalability in the rate of learning through δ, while $h_2(\cdot)$ assumes that the static factors that do not directly affect the learning rate are additively separable. Inserting equations (4) and (5) into equation (3) gives

$$P_t = \gamma + \psi \mathrm{e}^{-\delta L_t} + \beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML} \tag{6}$$

Because the learning index (L_t) is not observed directly, it is necessary to solve for L_0 in terms of P_0 (which is observable) and substitute in the result. In the initial period (i.e. when $t = 0$), the manufacturing performance parameter is

$$P_0 = \gamma + \psi \mathrm{e}^{-\delta L_0} + \beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML} \tag{7}$$

Solving for L_0 in terms of P_0 gives

$$L_0 = \frac{-\ln\left[\dfrac{P_0 - \gamma - (\beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML})}{\psi}\right]}{\delta} \tag{8}$$

Substituting equation (8) into equation (2) and then into equation (6) provides a learning curve with an observable initial period parameter:

$$\begin{aligned} P_t = {} & \gamma + \mathrm{e}^{-[\beta_1 \mathrm{CV}_t]} \cdot [P_0 - \gamma - (\beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} \\ & + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML})] + \beta_2 \mathrm{LW} + \beta_3 \mathrm{WS} \\ & + \beta_4 \mathrm{CR} + \beta_5 \mathrm{ML} \end{aligned} \tag{9}$$

where γ and β are redefined accordingly ($\gamma = \delta\gamma$, $\beta_i = \delta\beta_i \ \forall i$). Equation (9) represents a generic learning-based performance model. In order to capture the influence of R&D organization and IT practices on problem solving and learning performance, we redefine the learning index as $L_t' = L_t + \mathrm{OP} + \mathrm{ITP}$, where OP and ITP represent the knowledge gained by implementing particular R&D organization and IT practices, respectively, in the manufacturing facility. These practices influence learning not only directly via their implementation, but also indirectly by enhancing the productivity of the sources of learning highlighted in equation (2). The 'indirect effects' of these organizational routines are

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captured through terms testing for the influence of interactions between the particular R&D organization and IT practice variables and the cumulative volume (CV_t) variable. Including OP and ITP in equation (2) and solving the model as described above results in the following:

$$P_t = \gamma + e^{-[\beta_1 CV_t + OP(\alpha_1 + \alpha_2 CV_t) + ITP(\alpha_3 + \alpha_4 CV_t)]} \times [P_0 - \gamma - (\beta_2 LW + \beta_3 WS + \beta_4 CR + \beta_5 ML)] + \beta_2 LW + \beta_3 WS + \beta_4 CR + \beta_5 ML \tag{10}$$

Equation (10) provides the basis for our tests of the influence on manufacturing performance improvement of the R&D organization and IT practices discussed above.

Data

Data were collected as part of a global semiconductor manufacturing research project.[2] Semiconductor firms were targeted for participation to achieve a representative sample across product types, process technologies and geography. Manufacturing facilities were selected in consultation with participating semiconductor firms under the criteria of (1) possessing advanced technologies, products and processes; and (2) having sufficiently long production histories for longitudinal analysis. Surveys designed to collect facility- and process-specific information were mailed to semiconductor firms that agreed to participate. Responses to the surveys were verified and elaborated by field visits to each production site.

The surveys and field visits collected data on manufacturing performance (e.g. yield, cycle time, equipment efficiency) for individual semiconductor manufacturing processes, as well as data within each manufacturing facility related to the human resource, organizational, technological and managerial practices implemented. Each manufacturing process in our data set represents a unique semiconductor product. Most manufacturing facilities provided historical data that enabled the construction of time series on the performance of a manufacturing process during its development, introduction, ramp-up and full-scale operation. Usable data were collected from 93 manufacturing processes in 36 different manufacturing facilities representing 32 different semiconductor firms from 1989 to 2001, although the empirical analysis restricts the sample from 1995 to 2001. The manufacturing facilities of US, European, Japanese, Korean and Taiwanese semiconductor firms operating both domestically and offshore are included in the sample.

Dependent variables

Our analysis employs two measures of new process development and introduction performance. The first is die yield (DY). Because die yield is affected by particulate contamination on the silicon wafer surface, reported die yield is sensitive to average die size. To control for die size differences, die yield is translated into an equivalent ‘defect density’ measure (i.e. number of fatal defects per square centimetre) using the Murphy model.[3] The relationship between die yield and the average number of fatal defects per square centimetre is given by

$$DY = \left[\frac{1 - e^{-A DD}}{A DD}\right]^2 \tag{11}$$

where A is the die area and DD is the defect density parameter.

Figure 1 presents data on initial defect density and early-stage rates of improvement in defect density for a subsample of manufacturing processes that make similar memory products. As distinct processes are used to manufacture particular products, some manufacturing facilities are represented by more than one product-specific time series in Figure 1. Superior defect density performance is revealed in low initial defect densities and steady improvement rates. Semiconductor manufacturers with superior yield management performance have lower initial defect densities and steeper

[2] This multi-year research project is the Competitive Semiconductor Manufacturing Program conducted at the University of California at Berkeley. The project was sponsored by the Alfred P. Sloan Foundation, with the cooperation of semiconductor producers from Asia, Europe and the USA.

[3] The list of commonly used models includes the Poisson model, the Murphy model and the negative binomial model. The Murphy model extends the Poisson model to account for the observed clustering of defects on wafers. In particular, this model assumes a triangular approximation of the Gaussian distribution. See Stapper (1989) for an overview.

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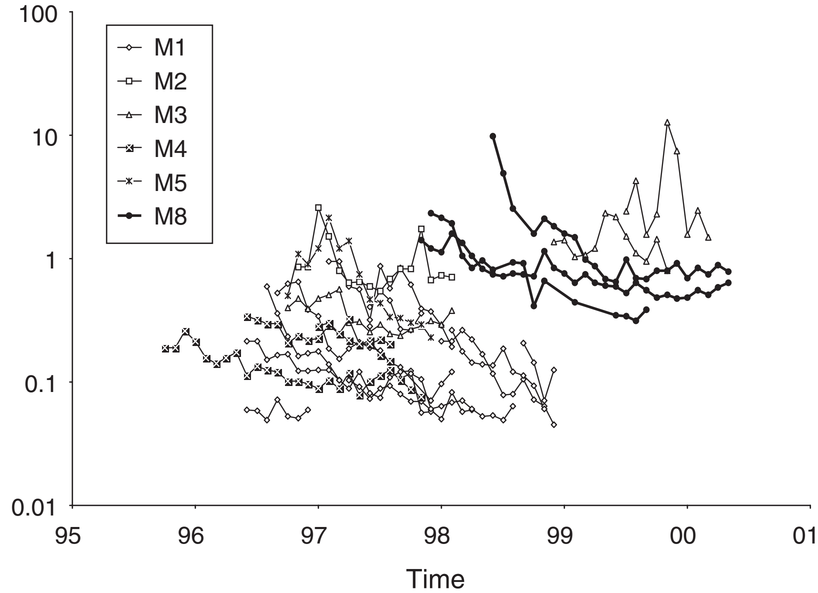

Figure 1. Memory defect density (0.33–0.40 micron processes)

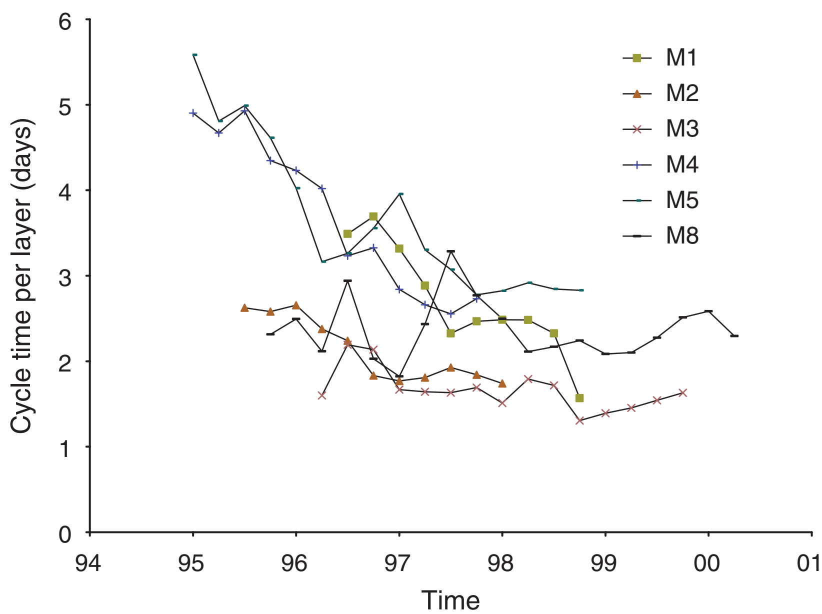

Figure 2. Cycle time per layer

slopes. There is significant variance among the manufacturing processes included in Figure 1, as the worst performing processes have initial defect densities roughly five times those of the best performing facilities. Moreover, these differences appear to persist over time (i.e. the slopes of the 'learning curves' vary substantially).

Our second performance measure is cycle time, or the length of time required to manufacture a semiconductor product. Because semiconductor firms produce products that require different numbers of circuitry layers, we normalize cycle time by the number of 'mask' layers (CTPL) necessary for each semiconductor product in the sample. The second dependent variable therefore takes the form

$$\mathrm{CTPL} = \frac{\mathrm{CT}}{\mathrm{ML}} \tag{12}$$

where CT represents cycle time and ML is the number of mask layers for the product. Figure 2 presents initial cycle time and early-stage rates of improvement in cycle time for the same set of manufacturing facilities depicted in Figure 1. Cycle time performance is shown as a weighted average (based on volume) of cycle times for all manufacturing processes within a particular manufacturing facility. Superior performance is again associated with low initial cycle times and steep slopes. Figure 2 similarly reveals considerable variation in both the initial starting point and the improvement rate among the manufacturing facilities presented.

Discussions of dynamic capabilities emphasize the organizational embeddedness of firm-specific routines and processes. This embeddedness characteristic should be reflected in the relative magnitudes of interfirm and intrafirm performance variation that we examine – performance differences among firms should be both more substantial and more enduring than performance differences within firms. A descriptive comparison of the coefficients of variation – sample standard deviation divided by sample mean – for yield and cycle time within and among manufacturing facilities confirms this characterization. The average within-firm yield coefficient of variation is 1.44, while the between-firm coefficient of variation is 4.42. Similarly, the average within-firm cycle time coefficient of variation is 0.66, while the between-firm coefficient of variation is 2.14. Our performance metrics thus appear to capture firm-specific differences that are both substantial and enduring, consistent with the arguments of other researchers who examine interfirm differences in learning rates (Adler and Clark, 1991; Argote and Epple, 1990).

Independent variables

We measure 'extent of use' both quantitatively and qualitatively for several of the R&D organization and IT practices that we investigate. Quantitative estimates are based upon questionnaire responses from participating semiconductor manufacturers. Qualitative estimates are based upon field visits and extensive interviews conducted with managers, engineers, operators and technicians in the participating manufacturing facilities. From this two-pronged approach, we construct measures of the extent of use for each practice within each manufacturing facility using a three-point scale (e.g. low usage = 0, medium usage = 1 and high usage = 2), where we deemed this construction to be both sensible and relative to the practices of other manufacturing facilities in the sample. We favour this measurement approach over alternative measurement approaches (e.g. the construction of percentage measures of the extent of use), because of minor differences in question interpretation across the manufacturing facilities in our sample.

Three variables capture deliberate learning mechanisms related to knowledge articulation, based on measures of particular organizational practices implemented within manufacturing facilities. *Intra-team diversity* measures two dimensions of functional diversity within teams: (1) the extent of involvement of both direct (i.e. operators and technicians) and indirect (i.e. engineers and supervisors) personnel in problem-solving activities; and (2) the degree to which the different functional areas (i.e. product design, process development, manufacturing etc.) are included. This variable tests Hypothesis H1a that greater diversity in team composition improves problem solving in new process development and introduction. *Inter-team diversity* captures the extent that functionally distinct team types operate in the manufacturing facility, and tests Hypothesis H1b that more diversity in the types of teams engaged in problem solving results in faster implementation of corrective solutions. More diverse teams represent deliberate organizational approaches that foster collective learning, improve communication and facilitate information availability that are directed at determining causal links critical to new process development and introduction.

Four variables measure the extent of co-location within the manufacturing facility. *Co-location* is defined as the number of manufacturing engineers who transfer to development and their transfer duration, and the number of development engineers who transfer to manufacturing and their transfer duration. Similar to the extent and use of teams, this organizational practice represents a deliberate learning mechanism targeted at improving understanding of the causal mechanisms that underlie new process development and introduction. We use principal components analysis to combine these four measures into a single 'co-location' variable (see discussion below).

Five variables capture deliberate learning mechanisms related to knowledge codification,

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Table 1. Variable description

Variable	Unit	Range	Description
Defect density	Defects/cm^2		Number of fatal defects per centimetre squared
Cycle time	Days/ml		Time (in days) to manufacture single mask layer
Cumulative volume	1 K wafer starts		Thousands of wafer starts
R&D organization practices			
Teams			
Intra-team diversity	Same/in between/ different	0..2	Diversity within problem-solving teams operating in the manufacturing facility
Inter-team diversity	Few/several/many	0..2	Diversity between problem-solving teams operating in the manufacturing facility
Co-location			
DE co-location	#		Number of development engineers co-located in commercial-volume facility
PE co-location	#		Number of process engineers co-located in development facility
DE time	#		Length of time development engineers spent in commercial-volume facility
PE time	#		Length of time process engineers spent in development facility
Information technology practices			Extent of information technology in manufacturing facility
Information handling automation			
Auto download	L/M/H	0..2	Extent of automatic process recipe downloaded by CAM system
Auto capture	L/M/H	0..2	Extent of automatic process metrology and equipment data capture by CAM system
Auto track	L/M/H	0..2	Extent of automatic track-in and track-out (time) of wafer lots by CAM system
Database analysis			
DB capability	L/M/H	0..2	Extent that data captured are readily available in an integrated relational database
Production scheduling			
Shopfloor control	L/M/H	0..2	Sophistication of automatic scheduling system of wafer lots and/or machines
Linewidth	[0, . . ., 1]		Normalized linewidth of individual process to technological frontier
Wafer size	#		Normalized size of wafer manufactured (100 mm as base)
Clean room grade	#		Maximum clean room grade (particles/ft^3)
Mask layers	#		Number of mask layers for device

based on measures of IT practices utilized within manufacturing facilities. Each manufacturing facility included in our study is categorized according to its level of adoption of these IT practices, relative to other manufacturing facilities. The automation of *Information handling* is constructed from measures of the extent of adoption of three types: (1) automated download of process 'recipes' into semiconductor processing equipment; (2) automated capture of process and equipment performance data; and (3) automated wafer lot tracking. The extent of *Database analysis* is constructed according to whether applications exist that can track production lots, collect integrated data, and link these data directly to statistical tools for data analysis. Finally, the extent of advanced *Production scheduling* systems is constructed on the ratings of shopfloor production (i.e. product and equipment scheduling) systems. We argue that IT practices such as these represent effective methods for codifying information important to the replication and diffusion of a particular set of activities within the manufacturing facilities.

Several static variables are included as controls in the empirical analysis. *Linewidth* is the dimension of the smallest circuit feature manufactured, and represents the technological sophistication of a semiconductor product (smaller linewidths are more difficult to produce, *ceteris paribus*). The 'technological frontier' defined by the most advanced linewidth has shifted during the time period of our study. We therefore convert linewidth for a given manufacturing process according to its 'distance' from the technological frontier, which we define and update on the basis of industry analyses that document where the 'leading-edge' in linewidth is over time. *Linewidth* therefore ranges

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Table 2. Summary statistics and correlations

	Defect density	Cycle time per layer	Cumulative volume	Intra-team diversity	Inter-team diversity	DE co-location	PE co-location	DE time	PE time	Auto download	Auto capture	Auto track	DB capability	Shop-floor control	Line-width	Wafer size	Clean room	Mask layers
Mean	1.001	2.801	61.877	4.156	1.157	2.550	4.854	18.211	42.809	0.869	0.396	1.212	1.385	0.784	0.848	1.629	1327.794	15.986
SD	1.520	0.984	88.882	2.328	0.697	2.097	5.389	23.576	95.093	0.796	0.677	0.915	0.858	0.724	0.409	0.264	2864.062	4.622
Min	0.050	0.580	0.004	1.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.250	1.250	10.000	5.000
Max	27.580	9.000	758.400	7.000	2.000	12.000	30.000	96.000	648.000	2.000	2.000	2.000	2.000	2.000	1.000	2.000	10000.000	28.000
Correlations																		
Defect density	1.000																	
Cycle time per layer	−0.124	1.000																
Cumulative volume	−0.228	−0.057	1.000															
Intra-team diversity	−0.332	−0.405	0.154	1.000														
Inter-team diversity	−0.074	0.054	−0.115	0.156	1.000													
DE co-location	−0.014	0.216	−0.007	−0.392	−0.113	1.000												
PE co-location	−0.003	0.062	−0.057	−0.166	0.107	0.278	1.000											
DE time	0.083	−0.006	−0.024	−0.614	−0.014	0.744	0.362	1.000										
PE time	0.000	−0.062	−0.080	−0.089	0.119	−0.085	0.846	0.087	1.000									
Auto download	−0.257	0.079	0.136	0.269	0.148	0.122	0.027	0.011	0.139	1.000								
Auto capture	−0.256	−0.164	−0.075	0.210	0.163	0.045	−0.033	0.004	0.043	0.496	1.000							
Auto track	−0.141	0.133	−0.082	0.142	0.687	0.012	−0.026	−0.157	−0.016	0.072	0.275	1.000						
DB capability	−0.072	−0.362	−0.217	0.010	−0.158	0.069	0.320	0.144	0.230	−0.103	0.274	−0.132	1.000					
Shopfloor control	−0.159	0.186	−0.023	0.201	0.866	0.093	0.005	−0.002	−0.051	0.291	0.032	0.686	−0.202	1.000				
Linewidth	0.078	0.159	0.192	−0.293	0.059	−0.100	0.096	−0.021	0.141	−0.318	−0.657	0.001	−0.479	0.145	1.000			
Wafer size	−0.228	−0.230	−0.184	0.459	0.107	0.072	−0.218	−0.078	−0.222	0.463	0.709	0.170	0.409	0.095	−0.880	1.000		
Clean room grade	−0.050	−0.078	0.077	−0.135	−0.369	0.371	0.181	0.100	0.004	−0.257	−0.200	0.199	0.329	−0.084	0.138	−0.179	1.000	
Mask layers	0.021	−0.043	−0.158	0.297	−0.046	0.063	0.089	−0.011	0.095	0.391	0.466	0.063	0.261	−0.168	−0.735	0.671	−0.116	1.000

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from near zero (lagging process technologies) to one (leading process technologies). *Clean room grade* is a measure of the maximum number of particles per cubic foot in the facility. *Wafer size* is a measure of the diameter of wafers manufactured normalized to the industry standard (which during the period covered by these data was 200 cm). *Clean room grade* and *Wafer size* both capture the technological complexity of a given manufacturing process, as well as the magnitude of investments in steps to accommodate this complexity. *Mask layers* is the number of conducting and insulating material layers used to fabricate the semiconductor component, and represents a proxy of the total number of process steps. More mask layers extend cycle time and increase the probability of a fatal defect on the die, *ceteris paribus*. Finally, *Cumulative volume* is constructed as the sum of wafer starts (scaled in 1000 unit increments) from the initial period since data collection commenced to the current period, using data from both new and established manufacturing processes.

Empirical analysis

Empirical results

Table 1 describes the variables used in our analysis. Table 2 provides summary and correlation statistics. Semiconductor manufacturing facilities in our sample have roughly one defect per square centimetre and take roughly three days per mask layer for a representative product, but significant heterogeneity exists in the sample for both performance measures. Table 2 also indicates modestly wide ranges in most of the independent variables.

Our econometric approach utilizes principal components analysis to construct measures of several of the knowledge articulation and codification processes that contribute to problem solving in new process development and introduction. In particular, we extract the principal components that maximize the interfirm variance of the four co-location variables and five IT variables described above. We retain only those factors with eigenvalues greater than one, as suggested by Kaiser (1960). This procedure results in one principal component for the co-location variables and two principal components for the IT variables.

Table 3 displays the cycle time results using four separate models of the specification in equation (10); the same models in Table 4 use yield as their dependent variable. All models are estimated using a non-linear maximum likelihood estimator with a first-order (AR1) serial correlation correction. Each model provides the estimation results with and without manufacturing facility fixed effects, but the fixed effect coefficients are not reported because of space constraints. The coefficient signs with and without fixed effects within each model are broadly consistent, although the magnitudes are generally smaller in fixed effects models. Reported log likelihoods indicate that each successive model in its respective table is a statistically significant improvement over the initial model.

Model 1 in Table 3 represents a baseline model that employs only *Cumulative volume* and the control variables measuring characteristics of the manufacturing process and facility. Cycle time performance improves with cumulative volume, a finding consistent with generic learning-curve models.[4] Cumulative volume is an important determinant of learning because it provides information about cycle time excursions that can be corrected through engineering analysis (Adler and Clark, 1991). But performance improvement does not arise solely from repetition; it can be enhanced by the deliberate problem-solving activities within the manufacturing facility (Bohn, 1995; Hatch and Mowery, 1998).

Models 2–4 test for the influence of R&D organization and IT practices on firms' performance in process development and introduction. Model 2 incorporates measures of the extent of teams (diversity in type and in composition) and co-location of personnel into Model 1. The sign and value of the first coefficient for each practice capture its direct effect on the level of cycle time – i.e. the magnitude of any upward or downward shift in the learning curve. The sign and value of the second coefficient for each practice represent the interaction of the R&D organization variables with *Cumulative volume* and capture the indirect effect of each of these practices on the cycle time slope – i.e. the steepening or flattening

[4]We rescale all variables so that the same sign has the same interpretation for both the learning index (i.e. $h_1(L_t)$) and static variables (i.e. $h_2(\cdot)$). The functional form used in the empirical estimation indicates that a positive (negative) coefficient improves (worsens) manufacturing performance.

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Table 3. Cycle time results

	Model 1		Model 2		Model 3		Model 4	
	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)
Constant	5.191***	4.140*	– 32.948***	– 41.514***	9.654***	23.067*	8.078***	9.215**
	(1.437)	(2.472)	(10.209)	(15.900)	(2.232)	(12.512)	(2.398)	(3.697)
Cumulative volume	1.182E-03***	8.897E-04***	2.461E-04***	2.020E-04***	1.321E-03***	3.522E-04**	2.375E-04***	2.010E-04**
	(1.086E-04)	(1.212E-04)	(6.203E-05)	(6.948E-05)	(1.152E-04)	(1.505E-04)	(7.333E-05)	(8.039E-05)
Intra-team diversity			– 8.595E-03***	– 7.130E-03***			– 9.116E-03***	– 7.391E-03***
			(2.130E-03)	(2.440E-03)			(2.687E-03)	(2.771E-03)
Inter-team diversity			1.575E-02***	1.414E-02***			1.183E-02***	1.053E-02**
			(4.155E-03)	(5.033E-03)			(3.754E-03)	(4.376E-03)
Co-location			– 1.002E-03**	– 7.330E-04*			– 2.036E-03***	– 1.717E-03**
			(4.119E-04)	(4.420E-04)			(7.346E-04)	(7.687E-04)
Intra-team diversity × CV			0.916E-05***	8.298E-05***			6.861E-05***	7.174E-05**
			(2.668E-05)	(2.996E-05)			(2.638E-05)	(3.494E-05)
Inter-team diversity × CV			– 7.703E-06	– 8.052E-06			– 2.605E-05*	– 3.596E-05
			(5.521E-06)	(6.266E-06)			(1.494E-05)	(2.238E-05)
Co-location × CV			4.408E-05***	3.919E-05**			4.562E-05	3.454E-04
			(1.293E-05)	(1.549E-05)			(4.676E-04)	(5.585E-04)
IT 1					– 3.870E-03*	– 3.264E-03	– 1.556E-04	– 1.629E-04
					(2.232E-03)	(2.725E-03)	(4.249E-04)	(1.005E-03)
IT 2					– 1.011E-02***	– 1.523E-02**	– 9.398E-03***	– 7.969E-03***
					(2.211E-03)	(6.769E-03)	(2.735E-03)	(3.007E-03)
IT 1 × CV					2.388E-05	5.153E-05**	5.365E-05***	2.892E-05**
					(2.398E-05)	(2.331E-05)	(1.549E-05)	(1.171E-05)
IT 2 × CV					3.429E-05**	4.921E-05***	3.759E-05***	3.490E-05**
					(1.769E-05)	(1.906E-05)	(1.234E-05)	(1.511E-05)
Linewidth	1.811***	2.147***	6.625***	7.761**	3.941***	10.997**	27.218***	32.881**
	(0.402)	(0.682)	(2.009)	(3.103)	(0.589)	(4.791)	(8.448)	(12.867)
Wafer size	3.898***	4.245***	20.087***	25.807**	9.084***	25.213**	79.708***	97.386**
	(0.822)	(1.435)	(5.601)	(10.808)	(1.425)	(12.400)	(24.387)	(39.172)
Clean room grade	0.000	0.000	0.004***	0.004**	0.000	0.000	0.001**	0.000
	(0.000)	(0.000)	(0.001)	(0.002)	(0.000)	(0.000)	(0.000)	(0.001)
ρ	– 0.952***	– 0.987***	– 0.972***	– 0.934***	– 0.980***	– 0.964***	– 0.948***	– 0.917***
	(0.030)	(0.033)	(0.018)	(0.021)	(0.030)	(0.034)	(0.019)	(0.021)
N	1305	1305	1305	1305	1305	1305	1305	1305
Log likelihood	5598.2	6068.8	6102.4	6274.6	6084.7	6272.6	6538.8	6609.6
Firm fixed effects	No	Yes	No	Yes	No	Yes	No	Yes

*p<0.10; **p<0.05; ***p<0.01.

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Table 4. Yield results

	Model 1		Model 2		Model 3		Model 4	
	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)	Est. (SE)
Constant	4.040*	6.251**	9.478***	11.230***	2.164***	7.125***	10.345***	7.821***
	(2.428)	(2.988)	(1.876)	(1.877)	(0.119)	(2.605)	(1.313)	(1.517)
Cumulative volume	1.724E-03***	1.435E-03***	3.595E-03***	4.682E-03***	3.397E-03***	5.360E-04**	4.492E-03***	6.515E-04***
	(1.786E-04)	(2.031E-04)	(5.716E-04)	(8.246E-04)	(1.721E-04)	(2.253E-04)	(7.101E-04)	(1.073E-04)
Intra-team diversity			– 1.739E-02***	– 1.376E-02**			– 4.386E-02***	– 4.725E-02***
			(3.869E-03)	(6.838E-03)			(6.061E-03)	(7.892E-03)
Inter-team diversity			2.187E-01***	1.798E-01***			2.658E-01***	2.601E-01***
			(2.286E-02)	(2.961E-02)			(2.151E-02)	(2.778E-02)
Co-location			– 6.424E-02***	– 8.471E-02***			– 8.881E-02***	– 6.838E-02***
			(1.624E-02)	(2.143E-02)			(1.298E-02)	(1.491E-02)
Intra-team diversity × CV			1.894E-04***	1.911E-04*			4.802E-04***	8.649E-04***
			(5.500E-05)	(1.023E-04)			(1.671E-04)	(2.626E-04)
Inter-team diversity × CV			2.575E-04	– 4.375E-04			– 3.665E-04	– 9.916E-04
			(3.220E-04)	(5.289E-04)			(5.820E-04)	(7.018E-04)
Co-location × CV			7.966E-04**	1.514E-03***			5.287E-05***	4.219E-05**
			(3.806E-04)	(4.146E-04)			(1.695E-05)	(1.682E-05)
IT 1					– 3.380E-02***	– 1.671E-02**	– 2.734E-02**	– 5.550E-02***
					(4.404E-03)	(7.797E-03)	(1.165E-02)	(1.401E-02)
IT 2					– 4.328E-02***	– 8.325E-03**	– 1.403E-01***	– 1.747E-01***
					(4.422E-03)	(3.592E-03)	(2.321E-02)	(2.855E-02)
IT 1 × CV					1.938E-03***	1.967E-04**	7.522E-04**	4.531E-04
					(1.098E-04)	(9.003E-05)	(3.174E-04)	(4.128E-04)
IT 2 × CV					4.013E-04***	1.963E-04***	1.046E-03***	1.913E-03***
					(4.830E-05)	(7.642E-05)	(4.056E-04)	(6.042E-04)
Linewidth	0.936	1.227	– 1.391**	– 1.850***	– 4.331***	– 11.336***	– 0.558	– 0.757
	(0.740)	(0.943)	(0.685)	(0.655)	(0.223)	(3.781)	(0.531)	(0.597)
Wafer size	2.213**	3.136***	3.578***	3.704***	9.503***	34.616**	3.200***	2.522***
	(0.903)	(1.137)	(0.773)	(0.777)	(0.541)	(13.633)	(0.531)	(0.651)
Clean room grade	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
	(0.000)	(0.000)	(0.000)	(0.000)	(0.000)	(0.000)	(0.000)	(0.000)
Mask layers	0.031	0.130*	0.162***	0.187***	0.309***	1.313**	0.189***	0.135***
	(0.057)	(0.069)	(0.029)	(0.036)	(0.028)	(0.570)	(0.029)	(0.031)
ρ	– 0.993***	– 0.997***	– 0.963***	– 0.989***	– 0.953***	– 0.908***	– 0.960***	– 0.989***
	(0.024)	(0.026)	(0.024)	(0.023)	(0.023)	(0.025)	(0.023)	(0.023)
N	1235	1235	1235	1235	1235	1235	1235	1235
Log likelihood	2144.2	2252.4	2827.0	3052.4	2284.9	2502.1	2903.3	3216.5
Firm fixed effects	No	Yes	No	Yes	No	Yes	No	Yes

*p<0.10; **p<0.05; ***p<0.01.

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of the learning curve as cumulative volume increases. *Intra-team diversity* initially shifts the learning curve up, suggesting that it worsens initial cycle time, but increases the cycle time improvement rate as volume expands, indicated by the positive coefficient for the interaction of *Intra-team diversity* with cumulative production. By contrast, *Inter-team diversity* shifts the learning curve down, improving initial cycle time performance, but has no statistically significant effect on the cycle time slope. The results provide partial support for Hypotheses H1a and H1b. The more extensive co-location of personnel impedes problem solving and learning at low product volumes, but significantly improves the rate of learning as cumulative production volume expands, consistent with Hypothesis H2.

Model 3 replaces the R&D organization measures with the IT measures. The IT practice measures have similar and statistically significant effects on both the level and slope of the cycle time learning curve. Both IT measures initially shift the learning curve up, worsening cycle time performance at low levels of output. The rate of improvement in cycle time increases, however, with more production volume. IT practices that enhance knowledge codification thus significantly improve cycle time performance as output expands, consistent with Hypothesis H3. Model 4 in Table 3 analyses the combined effects of R&D organization and IT deployment on cycle time performance. The results are broadly consistent with those obtained in Models 2 and 3, although the indirect effect of greater co-location loses statistical significance.

Model 1 in Table 4 presents the baseline model results with yield (defect density) replacing cycle time as the dependent variable. The results are broadly consistent with Model 1 in Table 3 – yield performance improves as cumulative volume increases. Model 2 incorporates the R&D organization variables into Model 1. The greater extent of different types of teams initially shifts the yield learning curve down, but has no effect on the slope. By contrast, greater functional diversity within teams initially shifts the learning curve up but steepens the slope as cumulative production increases. These R&D organization practices thus have similar effects on cycle time and yield performance. The greater extent of co-location initially shifts the performance curve up, but does steepen the learning curve slope with more cumulative production volume. While the direct effects from the extent of co-location are similar for cycle time and yield performance,[5] only the indirect effects from the extent of co-location are positive and significant for yield performance. This finding suggests that co-location enhances manufacturing facilities' abilities to learn and solve problems only at high volumes of production. Model 3 examines the influence of the IT practices on yield performance. Both IT practice measures initially shift the yield curve up, but steepen the slope with greater cumulative production. This finding not only supports Hypothesis H3, but also demonstrates similar performance effects for both cycle time and defect density. Model 4 incorporates the combined influence of the R&D organization and IT practice variables on yield improvement. The signs and magnitudes of the coefficients in Model 4 are broadly consistent with those for Models 2 and 3, although one indirect IT practice loses statistical significance. Nevertheless, intra- and inter-team diversity, co-location and IT implementation remain effective mechanisms for problem solving in yield improvement.

Discussion

The results indicate that these R&D organization and IT practices have similar and different effects on yield and cycle time performance. These practices have mixed effects on manufacturing performance at low production volumes, but generally increase the rate of performance improvement as production volumes expand (one exception is the effect of inter-team diversity on the rate of performance improvement). Given the cost and complexity of these practices, their different direct effects raise important questions as to whether they are economically justified. In particular, there appears to be some minimum production volume threshold that semiconductor manufacturing facilities must achieve in order for the benefits of steeper learning curves (the indirect effects) to outweigh the penalties of poorer starting points (the direct effects). At production volumes below this threshold, the

[5]In addition, the empirical results are similar for both yield and cycle time performance when examining the effects of unidirectional co-location (e.g. development personnel to manufacturing) versus bidirectional co-location.

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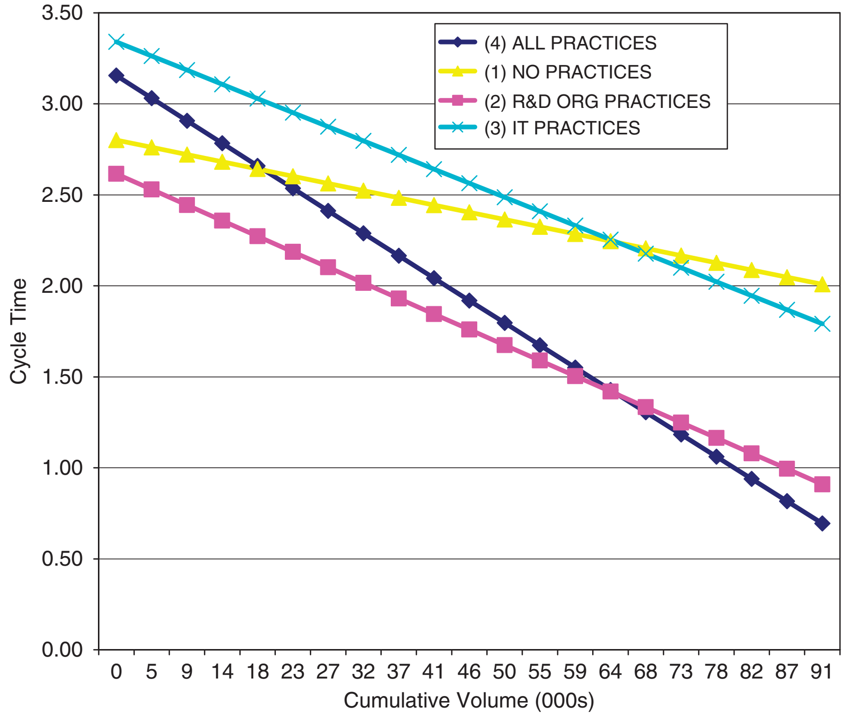

Figure 3. Cycle time performance

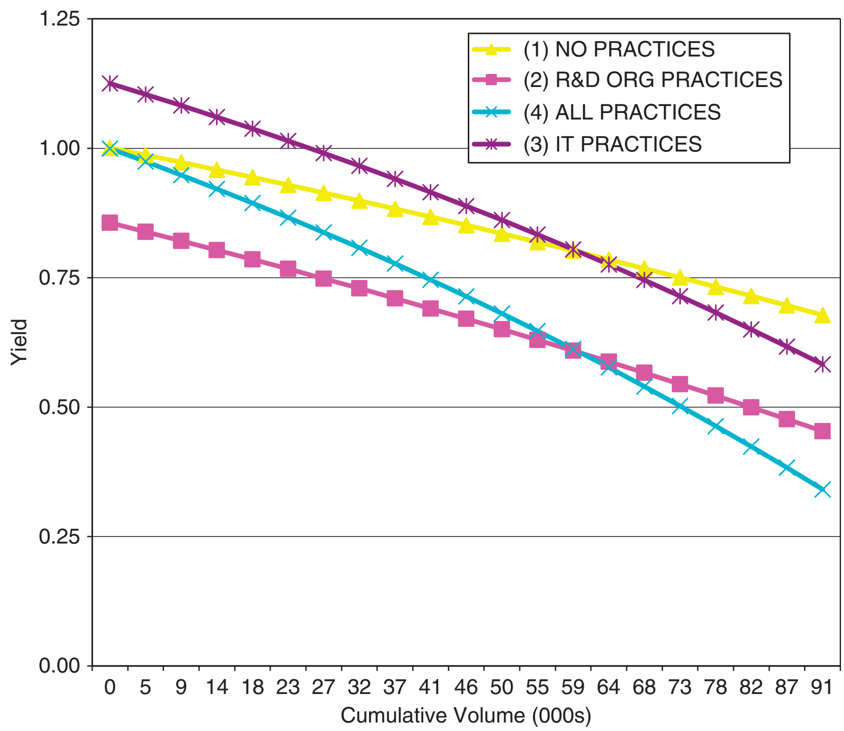

Figure 4. Defect density performance

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implementation of these practices will worsen performance relative to semiconductor manufacturers that do not use them.

Figures 3 and 4 depict the 'volume dependence' of these negative and positive effects on performance for cycle time and defect density, respectively. Both figures use the coefficient estimates from their respective Model 4 fixed effect estimations and hold initial performance and all of the independent variables (including monthly production volumes) at their means. Figure 3 compares cycle time performance for semiconductor manufacturers implementing (1) neither practice; (2) R&D organization practices; (3) IT practices; and (4) both R&D organization and IT practices. By comparison with the 'no practice' baseline, Figure 3 indicates that the implementation of the R&D organization practices immediately improves cycle time performance and this performance margin increases with greater production volume. For IT practices a clear 'volume threshold' exists, as the effects of the initial upward shift in the cycle time learning curve are eventually offset by more rapid learning.[6] The joint effect of both R&D organization and IT practices on cycle time performance indicates an initial starting point between scenarios (2) and (3). Performance associated with both R&D organization and IT practices implemented surpasses the 'no practice' baseline at roughly 25,000 cumulative wafers (five equivalent production months) and the R&D organization practices scenario at roughly 65,000 cumulative wafer starts (13 equivalent production months).

Figure 4 presents a similar comparison for yield performance. Against the 'no practice' baseline, the implementation of R&D organization practices immediately improves yield and increases this performance margin with greater production volume. IT practices shift the yield learning curve up initially, but also steepen the yield learning curve slope and eventually surpass (at roughly 60,000 cumulative wafer starts) what would be achieved without the implementation of these practices. The joint effect of both R&D organization and IT practices on cycle time performance lies in between the independent effects of these practices, but eventually results in the best yield performance at roughly 65,000 cumulative wafer starts. Interestingly, the joint initial effect of both R&D organization and IT practices is equal to the 'no practice' baseline, but has a markedly steeper improvement rate.

Larger semiconductor manufacturers possess performance advantages in cycle time and yield, since their larger monthly production volumes enable them to benefit from the interaction between cumulative volume and the R&D organization and IT practices implemented. Higher production volumes enable larger semiconductor manufacturers that employ these practices to achieve superior performance against the 'no practice' threshold in a shorter time period. For instance, a one standard deviation increase in monthly production volume for a manufacturing process from its mean reduces the crossover time period from lower to superior performance (assuming that both the R&D organization and IT practices are in place) to just under three months for cycle time and just under two months for yield. Interestingly, these findings are consistent with trends in the global semiconductor industry. Data from the late 1990s (the period covered by our study) indicate that manufacturing facilities with at least 20,000 wafer starts per month achieve performance advantages by comparison with smaller-volume facilities (Benavides, Duley and Johnson, 1999). Our results are consistent with these estimates of minimum efficient scale.

Semiconductor manufacturers that utilize a larger number of different types of functionally diverse problem-solving teams and co-location practices that strengthen links between development and manufacturing appear to learn more quickly, especially at higher production volumes. Inter-team diversity appears to provide immediate problem-solving benefits through greater focus in specific areas while intra-firm diversity provides problem-solving benefits from additional information. These effects are consistent for both yield and cycle time performance, and may derive from improvements in the articulation of tacit knowledge that otherwise is 'locked up' within the organization. Our results also suggest that semiconductor firms that more extensively deploy IT applications reap significant benefits at the level of organizational processes, enabling them to improve both yield and cycle time more quickly. IT practices support the codification of otherwise tacit knowledge, facilitating its internal dissemination and accel-

[6]After about 70,000 wafers produced, or 15 months for the average manufacturing process in the sample.

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erating problem solving and learning. In summary, R&D organization practices help articulate information and IT practices help codify information into forms more suitable for analysis. Both types of practices represent deliberate learning mechanisms that shape firms' new process development and introduction capabilities and subsequent manufacturing performance.

Importantly, these practices do not affect all dimensions of performance equally. Co-location improves yield performance but has little effect on cycle time improvement, perhaps because yield improvement relies to a greater extent on the articulation of tacit information that benefits from face-to-face communication. Co-location is also more probably geared toward articulating knowledge related to process technology transfer from development to production (which is an important driver of yield improvement), as opposed to articulating knowledge related to production scheduling (which is an important driver of cycle time improvement). The extent and use of teams within the manufacturing facility, on the other hand, accelerates cycle time improvement but has a more modest effect on yield improvement. This finding is consistent with the hypothesis that different problem-solving efforts are required in new process development and introduction when manufacturing performance is multidimensional. Despite these performance differences, the results clearly indicate that R&D organization and IT practices build problem solving and shape semiconductor manufacturers' new process development and introduction capabilities.

The firms in our sample that have adopted elements of the key R&D organization and IT practices that we identify have superior manufacturing performance. Nevertheless, further analyses of longitudinal data to establish whether these capabilities contribute to sustained competitive advantage in this industry are needed. Moreover, additional empirical examinations of the processes that build and develop dynamic capabilities and relate these capabilities back to performance inside other organizations and in other industries are also warranted.

Conclusion

The literature on dynamic capabilities consists largely of conceptual and theoretical discussions, rather than direct empirical tests of hypotheses. Moreover, few empirical analyses that examine processes inside organizations that lead to dynamic capabilities or the performance effects of firms' dynamic capabilities exist. In this paper we utilize data from a large sample of semiconductor manufacturing facilities to develop measures of firm-specific R&D organization and IT practices that facilitate problem solving and subsequently influence performance in the development and introduction of new process technologies, a key dynamic capability in the semiconductor industry.

The R&D organization and IT practices that we identify as central to firms' problem-solving efforts in new process development and introduction are rooted in the empirical literatures on product and process development, organizational behaviour and IT. These practices are the foundation for organizational learning via improved knowledge articulation and knowledge codification. Our empirical analysis focuses on the deliberate learning mechanisms used by semiconductor manufacturers to capture information from production experience and then to articulate and codify this information throughout the organization. R&D organization practices facilitate knowledge articulation through improved intrafirm communication and understanding. IT practices improve the codification of tacit knowledge. Both practices improve problem solving important to manufacturing performance improvement by improving organizations' abilities to utilize production-based information and to learn. Once new production processes are introduced into manufacturing, these practices accelerate the speed of problem identification, characterization and resolution.

Our empirical results provide strong support for the arguments of Teece, Pisano and Shuen (1997), Eisenhardt and Martin (2000), Zollo and Winter (2002), Winter (2003) and Helfat *et al* (2007) that, in rapidly changing (often high-technology) industries, firm-specific performance differences may reflect differences in their capabilities in managing novelty (in our case, the development and introduction of new process technologies). Our empirical analysis relates differences in new process development and introduction performance to firm-level organizational routines employed in the management of process innovation. Our empirical analysis also highlights the importance of deliberate, rather than passive, learning for the development of dynamic capabilities.

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