1. Part I-A: System Design



1. Intended operation

* Write a set of data to an SRAM array

The control signal tells SRAM to work on write mode. For each cycle, data in write registers and address given by user, address decoder with row decoder and column decoder decodes the address, then the data is read from write register and written to the respective row and columns decoded by the decoder.

* Read data sequentially from the array

The control signal tells SRAM to work on read mode. For each cycle, the address decoder decodes the address, then data is read from respective SRAM cells and write to READ registers. Address is increased by one after each cycle.

* Driven through a long-interconnect and add them sequentially for n cycle

The data in read registers of SRAM is read by the long-interconnect and it drives the data to the input registers of the adder system. Then the data is added to the already computed partial sum.

b. How to implement the sequential sum

* The sequential sum can be implemented by 3 8-bit registers as follow



* Adder gets one input from a 8-bit register whose data is the new data fetched from SRAM via the long-interconnect, and another input from the partial sum register. Then addition is executed and the output is written to the sum register output. In the he next cycle, the partial sum register is updated the newly calculated partial sum from the sum register. Then the adder get inputs from the 8-bit input register and partial sum register and repeat the same process.

c. Brief description of the system functionality

* We utilized pipeline speed up the system



* High-level functionality
* Write the entire array in the initialize cycles
* Perform 3 cycle of read, driven and partial sum updated, and addition operation (pipelined)

+ One cycle is read data from SRAM

+ The second cycle is driven data from SRAM’s read register to adder’s input register. At the same time, the value of the partial sum register is updated from the sum register.

+ Add data in the third cycle