

# Technical Note

## DDR3 Point-to-Point Design Support

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### Introduction

Point-to-point design layouts have unique memory requirements, and selecting the right memory design methodology can be critical to a project's success. While DDR3 SDRAM was targeted for use on modules, it can easily be adapted for point-to-point applications.

DDR3 is an evolutionary transition from DDR2. DDR3 point-to-point systems are similar to DDR2 point-to-point systems; both require similar design principles. But given that DDR3 signaling is more critical, DDR3 point-to-point systems require an emphasis on improving the data bus signaling.

Before reviewing this technical note, a basic understanding of DDR2 point-to-point design methodologies and DDR3 operation is recommended. Micron's DDR3 data sheet, along with the following technical notes, are available for reference on [micron.com](http://micron.com):

- TN-00-20: Understanding the Value of Signal Integrity Testing
- TN-41-02: DDR3 ZQ Calibration
- TN-41-04: Dynamic On-Die Termination
- TN-46-02: Decoupling Capacitor Calculation for a DDR Memory Channel
- TN-46-06: Termination for Point-to-Point Systems
- TN-46-11: DDR SDRAM Point-to-Point Simulation Process
- TN-46-14: Hardware Tips for Point-to-Point System Design: Termination, Layout, and Routing
- TN-47-19: DDR2 (Point-to-Point) Features and Functionality
- TN-47-20: DDR2 (Point-to-Pont) Package Sizes and Layout Basics

## DDR2 to DDR3 SDRAM Comparison

When designing point-to-point memory systems, the major differences between DDR2 and DDR3 include:

- An increase in bandwidth from 800 MT/s to 1600 MT/s, with optional 1866 MT/s and 2133 MT/s.
- An increase in the minimum clock frequency from 125 MHz to 300 MHz.
- Narrower DDR3 output drive ranges that can be recalibrated to adjust for voltage and temperature variations.
- Adjustable on-die termination (ODT) with dynamic control that provides ODT support during writes without having to wire the ODT signal.
- Small FBGA package sizes that enable high-density devices in extremely compact footprints for improved power delivery.

See the DDR3 Point-to-Point Advantages table below for a more detailed comparison.

**Table 1: DDR3 Point-to-Point Advantages**

Feature/Option	DDR2	DDR3	DDR3 Advantage
Voltage (core, I/O)	1.8V	1.5V	Lower power
Low power (core, I/O)	NA	1.35V	Lower power
V <sub>REF</sub> input	1 – all inputs	2 – DQs and CMD/ADDR	Improved power delivery
Data rate	800 MT/s	1600 MT/s	2X data rate
t <sub>CK</sub> DLL enabled	125–400 MHz	300–800 MHz	2X clock rate
t <sub>CK</sub> DLL disabled	Undefined	128–125 MHz	Slow clock debug
Prefetch	4 bits (4n)	8 bits (8n)	–
Burst length (selectable)	BL4, BL8	BC4, BL8	–
Burst type	Fixed	Fixed, on-the-fly (OTF)	–
Additive latency (selectable)	0, 1, 2, 3, 4	1, CL - 1, CL - 2	–
Data bus ODT – nominal	Yes	Yes	–
ODT nominal standby	50Ω, 75Ω, 150Ω	20Ω, 30Ω, 40Ω, 60Ω, 120Ω	–
ODT nominal writes	50Ω, 75Ω, 150Ω	40Ω, 60Ω, 120Ω	Improved signaling
Data bus ODT – dynamic	No	Yes	ODT without ODT pin control
ODT dynamic writes	NA	60Ω, 120Ω	Improved signaling
Data Bus ODT – variation	±20%	±10%	–
Driver impedance (full)	18Ω (12.9–32.5Ω)	34Ω (30.5–38.1Ω)	Improved signaling
Driver variation (full)	–37–59%	±10%	Improved signaling
Driver impedance (reduced)	40Ω (21.6–81.3Ω)	40Ω (36–44Ω)	Improved signaling
Driver variation (reduced)	–44–111%	±10%	Improved signaling
Driver/ODT calibration	None	Via external R	Improved signaling
Multipurpose register (MPR)	None	Outputs predefined pattern	–
Write leveling	None	DQS captures clock	De-skews if fly-by used
Reset	None	Dedicated input	–
Automatic self refresh (ASR)	None	Optional	Self refresh if T <sub>C</sub> > 85°C
FBGA package	60/84-ball	78/96-ball	Improved power busing

## DDR3 Overview

DDR3 functions much like DDR2 in that a source-synchronous data strobe is used, and data is transferred on both the leading and trailing strobe edges. However, DDR3 has an  $8n$ -prefetch architecture where the internal data cycle time is one-eighth the external data rate, and the internal data bus width is eight times the size of the external data bus width.

For example, a x16 DDR3 SDRAM device has a 128-bit-wide internal data bus, so for each single access to or from the internal array, eight data transfers of 16 bits each will be provided externally. Because of the  $8n$  prefetch, burst lengths are limited ( $BL = 8$ ). In addition to  $8n$  prefetch, both the DDR3 core and the I/O operate from a 1.5V power source (DDR3L is 1.35V). With the advanced process technology, lower operating voltage, and input voltage swings, DDR3 and DDR3L provide significant reduction in overall power consumption.

DDR3L (1.35V) will work well in point-to-point designs alongside DDR3 (1.5V). While DDR3L has the same timings as DDR3, DDR3L does not have as much voltage margin. However, the reduced voltage margin is not typically an issue with a well-terminated point-to-point system.

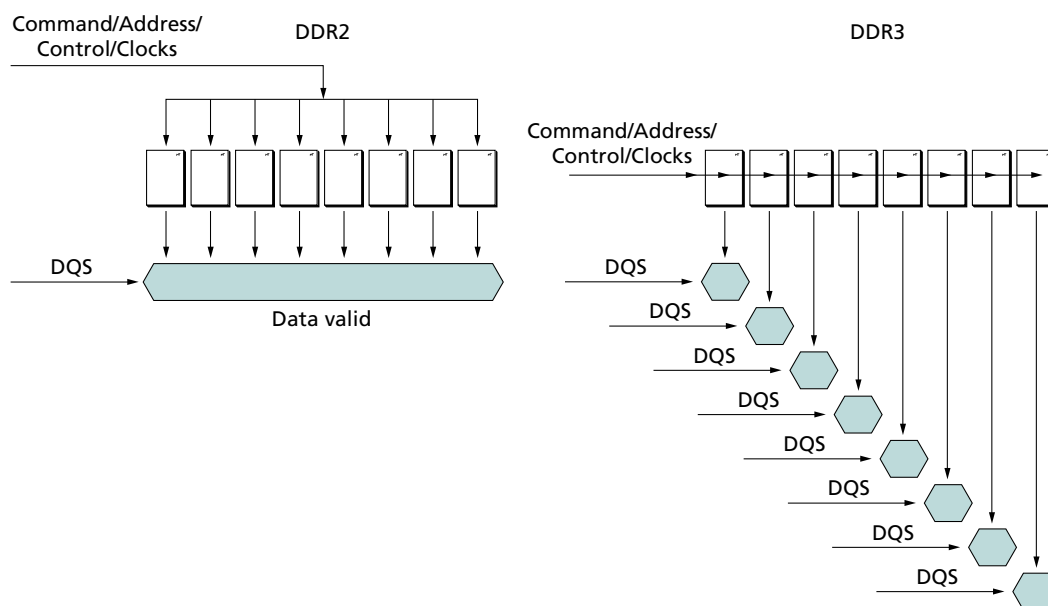
## Memory Architecture

SDRAM, DDR, and DDR2 memory system architectures assume a symmetrical tree layout coupled with minimal clock skews between command/address/control buses and the data bus. DDR3 memory system architectures assume a daisy-chain, or fly-by, layout. When developing systems that support JEDEC DDR3 modules, fly-by architecture must be supported.

DDR3 point-to-point designs, on the other hand, do not have to be implemented using a fly-by architecture. A DDR3 point-to-point design can employ either the DDR2 tree architecture (minimal timing skew concerns; command/address/control buses that likely do not require termination) or the DDR3 fly-by architecture (significant timing skew between clock and data buses; command/address/control buses that require termination).

Write leveling was added to DDR3 to remove the skew (induced by the fly-by architecture) between the command/address/control/clocks buses and each of the DRAM data buses, as shown in the figure below. Even if fly-by architecture is used in a point-to-point system, it is generally better to hard code the skews rather than use the write-leveling feature.

**Figure 1: DDR2 Tree vs. DDR3 Fly-By Architecture**



## On-Die Termination (ODT)

Like DDR2 ODT, DDR3 ODT reduces layout constraints by eliminating the need for discrete termination to  $V_{TT}$  and the need for  $V_{TT}$  generation for the data bus. ODT improvement is one of the more significant additions to DDR3. ODT has been improved in the following ways:

- Value reduction – Closer impedance matching for point-to-point systems, providing improved signal quality
- Calibration control – Neutralizing voltage and temperature shifts, providing improved signal quality
- Tighter ranges – Less variation, providing tighter control and improved signal quality
- Dynamic ODT – Desired termination opportunistically applied during writes

A summary of the DDR3 ODT resistors is shown in the ODT Settings – MR1 and ODT Settings – MR2 tables below. For most point-to-point designs,  $R_{TT\_NOM}$  for non-write cases are not applicable and are not used. These settings are intended to be used in dual-rank systems coupled with dynamic ODT use. In most cases, only  $R_{TT\_NOM}$  for writes or  $R_{TT\_WR}$  (that is, dynamic ODT) are used in point-to-point designs.

**Table 2: ODT Settings – MR1**

M9 M6 M2	R <sub>TT_NOM</sub> (ODT) Non-Writes	R <sub>TT_NOM</sub> (ODT) Writes
0 0 0	R <sub>TT_NOM</sub> disabled	R <sub>TT_NOM</sub> disabled
0 0 1	RZQ/4 (60Ω [NOM])	RZQ/4 (60Ω [NOM])
0 1 0	RZQ/2 (120Ω [NOM])	RZQ/2 (120Ω [NOM])
0 1 1	RZQ/6 (40Ω [NOM])	RZQ/6 (40Ω [NOM])
1 0 0	RZQ/12 (20Ω [NOM])	NA
1 0 1	RZQ/8 (30Ω [NOM])	NA
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

**Table 3: ODT Settings – MR2**

M10 M9	R <sub>TT_WR</sub> (ODT) Dynamic ODT
0 0	R <sub>TT_WR</sub> disabled
0 1	RZQ/4 (60Ω)
1 0	RZQ/2 (120Ω)
1 1	Reserved

## Reducing Values

DDR3's smaller signal swing coupled with reduced loading requirements allows for drivers with reduced current drive (that is, higher impedance drivers). The output drivers are the building blocks of ODT resistors. Thus, the ODT resistors can be derived at values that support point-to-point architectures well. The closer that the impedances match the transmission line, the better the signal quality.

## Calibration Control

DDR2 does not offer driver/resistor calibration; thus, the ODT resistors change with a voltage and/or temperature change. Also, parts from the manufacturer require a wider range of specification limits because of manufacturing distributions. DDR3 adds the ability to perform calibration when needed. Upon initialization, the drivers are calibrated to a known value to support tight tolerances. Calibration may also be performed at other times, as needed, to neutralize the effects of voltage and temperature shifts. Keeping tight driver and ODT resistor impedance tolerances helps improve signal quality.

## Tighter Ranges

As shown in the table below, the allowed DDR2 ODT variation is twice that of the DDR3 ODT (referenced at midpoint). The closer that the impedances match the transmission line, the better the signal quality.

**Table 4: ODT Variation**

Feature/Option	DDR2	DDR3	DDR3 Point-to-Point Advantage
Data bus ODT – variation	±20%	±10%	Improved signaling
Driver/ODT calibration	None	Via external R	Improved signaling

## Dynamic ODT

The intent of dynamic ODT is to allow the desired ODT value (larger R) to be opportunistically applied during writes, while also allowing a different ODT value (smaller R) to be applied to the same memory when in standby and when a different rank is being written to in multirank systems. This requires the DRAM device to have its  $R_{TT\_NOM}$  bits set in mode register 1 (MR1) and the  $R_{TT\_WR}$  bits set in mode register 2 (MR2). After the MR1 and MR2 ODT bits are set or enabled, toggling the ODT pin on and off is required in order to have a different  $R_{TT}$  value when the DRAM is in standby versus during writes.

$R_{TT\_NOM}$  for non-write cases is not applicable and would not be used in a point-to-point system. This setting is intended for use in dual-rank systems coupled with dynamic ODT.

Either  $R_{TT\_NOM}$  for writes or  $R_{TT\_WR}$  (that is, dynamic ODT) may be used for termination of the data bus during writes in point-to-point systems. Using  $R_{TT\_NOM}$  requires the ODT pin to toggle and turn on and off  $R_{TT}$  termination during writes. Using  $R_{TT\_WR}$  allows the ODT pin to be tied active (no routing of signal), and the  $R_{TT}$  termination to be automatically applied during writes as needed. Thus, dynamic ODT offers a clear benefit for point-to-point systems: no routing of ODT, yet automatic ODT control on the DRAM device.

## Output Drive Levels

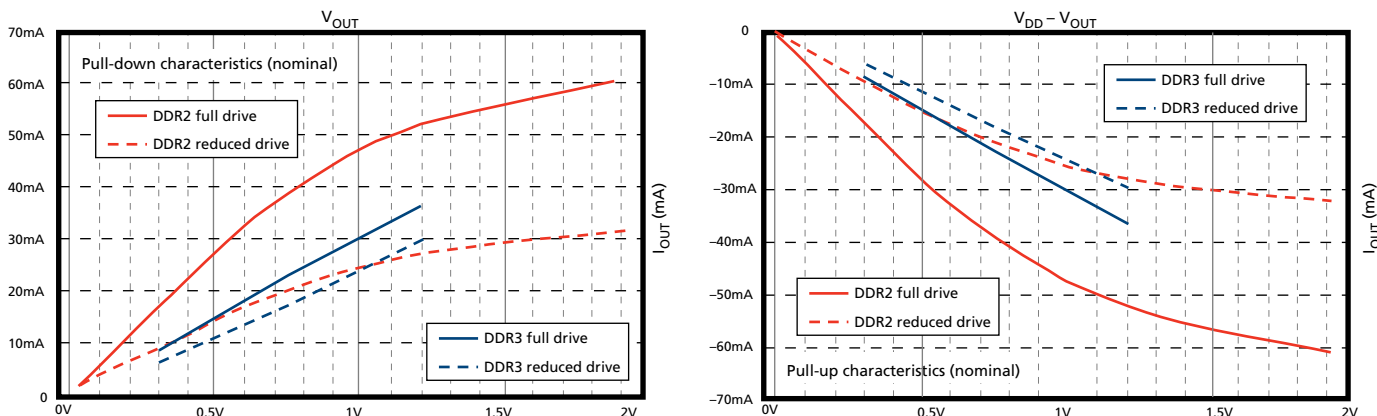
In point-to-point designs, the memory's position is typically quite close to the controller, which results in short data bus trace lengths. This makes a driver with a low-impedance output undesirable. DDR2 all but requires the DDR2 reduced drive mode to be used since the DDR2 full-drive output buffer impedance was fairly low (that is, 18Ω). Unfortunately, the DDR2 reduced output driver has a wide range that is rather difficult to design to. DDR3, on the other hand, provides two higher-impedance drives with tight tolerances that make them well-suited to support point-to-point designs, as shown in Table 1.

**Table 5: DDR3 Point-to-Point Advantages**

Feature/Option	DDR2	DDR3	DDR3 Advantage
Driver impedance (full)	18Ω (12.9–32.5Ω)	34Ω (30.5–38.1Ω)	Improved signaling
Driver variation (full)	–37–59%	± 10%	Improved signaling
Driver impedance (reduced)	40Ω (21.6–81.3Ω)	40Ω (36–44Ω)	Improved signaling
Driver variation (reduced)	–44–111%	± 10%	Improved signaling
Driver/ODT calibration	None	Via external R	Improved signaling

The figure below compares DDR2 and DDR3 full and reduced drive. The DDR3 values are both good options for point-to-point designs since they have a higher impedance and are more linear than DDR2 levels.

**Figure 2: Comparison of Full and Reduced Drive I/O**



## DDR3 Layout and Design Considerations

Layout is one of the key elements of a successfully designed application. The following sections provide guidance on the most important factors of layout so that if trade-offs need to be considered, they may be implemented appropriately.

### Decoupling

Micron DRAM has on-die capacitance for the core as well as the I/O. There is not a total reliance on external capacitance. It is not necessary to allocate a capacitor for every pin pair ( $V_{DD}:V_{SS}$ ,  $V_{DDQ}:V_{SSQ}$ ).

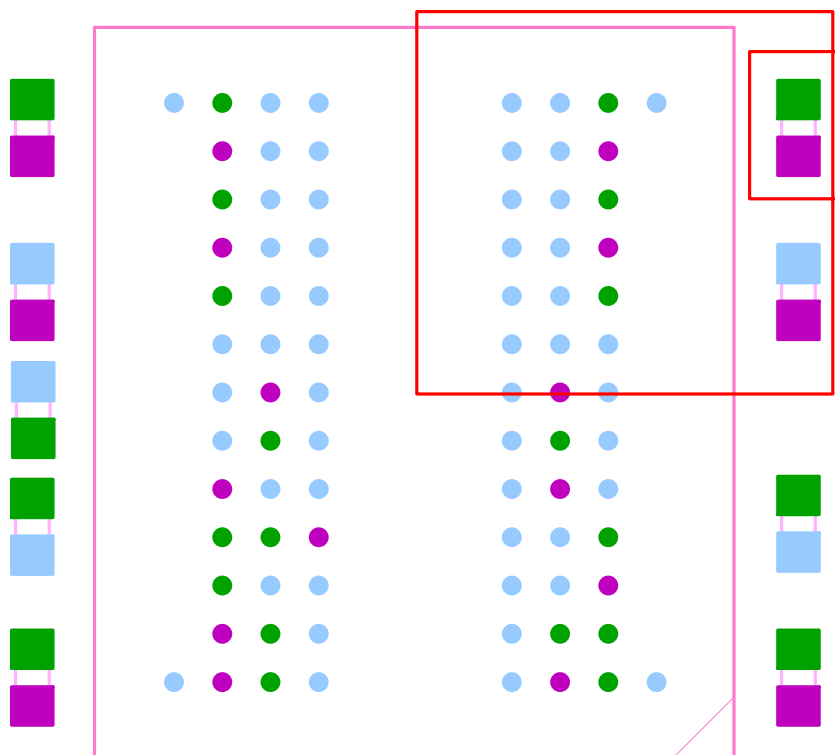
Decoupling prevents the voltage supply from dropping when the DRAM core requires current, as with a refresh, read, or write. It also provides current during reads for the output drivers. The core requirements tend to be lower frequency. The output drivers tend to have higher frequency demands. This means that the DRAM core requires the decoupling to have larger values, and the output drivers want low inductance in the decoupling path but not a significant amount of capacitance.

One recommendation is to place enough capacitance around the DRAM device to supply the core and to place capacitance near the output drivers for the I/O. This is accomplished by placing four capacitors around the device on each side of the package. Place one of the capacitors centered in the upper quarter of the ball grid and one in the lower quarter of the ball grid (see the Decoupling Placement Recommendations figure). Place these capacitors as close to the device as practical with the vias located to the device side of the capacitor. For these applications, the capacitors placed on both sides of the card in the I/O area may be optimized for specific purposes. The larger value primarily supports the DRAM core, and a smaller value with lower inductance primarily supports I/O. The smaller value should be sized to provide maximum benefit near the maximum data frequency.



Decide between two values—0.1 $\mu$ F and 1.0 $\mu$ F—for the core. Intermediate values tend to cost the same as 1.0 $\mu$ F capacitors, which is based on demand and may change over time. Consider 0.1 $\mu$ F for designs that have significant capacitance away from the DRAM and a power supply on the same PCB. For designs that are complex or have an isolated power supply (for example, on another board), use 1.0 $\mu$ F. For the I/O, where inductance is the basic concern, having a short path with sufficient vias is the main requirement.

**Figure 3: Decoupling Placement Recommendations**



## Power Vias and Sharing

A DRAM device has four supply pin types:  $V_{DD}$  and  $V_{SS}$  power the core, and  $V_{DDQ}$  and  $V_{SSQ}$  are present only for the output drivers. However, there are exceptions. The substrate for the device typically maintains isolation from the package balls all the way to the die where isolation is also maintained. This isolation is intended to keep I/O noise off of the core supply and core noise off of the I/O drivers. It is good practice, but not an absolute requirement, to use separate vias for  $V_{SS}$  and  $V_{SSQ}$  as well as for  $V_{DD}$  and  $V_{DDQ}$ .

There is a compromise position. Where a via connects to a  $V_{SS}$  ball on one side of the card and a  $V_{SSQ}$  ball on the other side of the card, the actual path being shared is minimized.

The path from the planes to the DRAM balls is important. Providing good, low inductance paths provides the best margin. Therefore, separate vias where possible and provide as wide of a trace from the via to the DRAM ball as the design permits.

Where there is concern and sufficient room, multiple vias are a possibility. This is generally applied at the decoupling cap to make a low impedance connection to the planes.

## Return Path

If anything is overlooked, it will be the current return path. This is most important for terminated signals (parallel termination) since the current flowing through the termination and back to the source involves higher currents. No board-level (2D) simulators take this into account. They assume perfect return paths. Most simulators interpret that an adjacent layer described as a plane is the perfect return path whether it is related to the signal or not. Some board simulators take into account plane boundaries and gaps in the plane to a degree. A 3D simulator is required to take into account the correct return path. These are generally not appropriate for most applications.

Most of the issues with the return path are discovered with visual inspection. The current return path is the path of least resistance. This may vary with frequency, so resistance alone may be a good indicator.

## Trace Length Matching

Prior to designing the card, it is useful to decide how much of the timing budget to allocate to routing mismatch. This can be determined by thinking in terms of time or as a percentage of the clock period. For example, 1% ( $\pm 0.5\%$ ) at 800 MHz clock is 6.25ps (1250ps/200). Typical flight times for FR4 PCB are near 6.5 ps/mm. So matching to  $\pm 1$ mm ( $\pm 0.040$  inch) allocates 1% of the clock period to route matching. Selecting 1mm is completely arbitrary. If the design is not likely to push the design limits, a larger number can be allocated.

When the design has unknowns, it is important to select a tighter matching approach. Using this approach is not difficult and allows as much margin as is conveniently available to allocate to the unknowns.

## Address

For the address, the design will likely use a tree topology with branching. Making the branches uneven causes some signal integrity issues. For this reason, make all related branches match to within 1mm within each net. Different nets may have different branch lengths as long as they are matched within a branch. This is somewhat arbitrary, but there are many cases to consider, and 1mm should be adequate for all cases. There may be some exceptions.

## Data Bus

For DQ, the topology is point-to-point or point-to-two-points where the two points are close together. For the data bus, the bit rate is the period on interest. That is 625ps for an 800 MHz clock. Because 1% of this interval is 6.25ps, if the matching is held to a range of 1% ( $\pm 0.5\%$ ), then  $\pm 0.5$ mm is the limit. Again, this is arbitrary.

Other factors to account for are vias, differences in propagation time for routing on inner layers versus outer layers, and load differences.

## Propagation Delay

Propagation delay for inner layers and outer layers is different because the effective dielectric constant is different. The dielectric constant for the inner layer is defined by the glass and resin of the PCB. Outer layers have a mix of materials with different dielectric constants. Generally the materials are the glass and resin of the PCB, the solder mask that is on the surface, and the air that is above the solder mask. This defines the effective

tive dielectric for the outer layers and usually amounts to a 10% decrease in propagation delay for traces on the outer layers. For the design of JEDEC UDIMMs, a 10% difference accounts for the differences in propagation of the inner layers versus the outer layers. If all traces that need to match are routed with the same percentage on the outer layers versus the inner layers, this difference may be ignored for the purpose of matching timing. Otherwise, this difference should be accounted for in any delay or matching calculations.

For inner layer propagation, velocity is about 6.5 ps/mm. To match all traces within 10ps, traces must be held within a range of 1.5mm, 60 mils. In most cases, this can be easily achieved. Most designs tolerate a much greater variation and still have significant margin. The engineer must decide how much of the timing budget is allocated to trace matching.

## Vias

In most cases, the number of vias in matched lines should be the same. If this is not the case, the degree of mismatch should be held to a minimum. Vias represent additional length in the Z direction. The actual length of a via depends on the starting and ending layers of the current flow. Because all vias are not the same, one value of delay for all vias is not possible. Inductance and capacitance cause additional delay beyond the delay associated with the length of the via. The inductance and capacitance vary depending on the starting and ending layers. This is either complex or labor-intensive and is the reason for trying to match the number of vias across all matched lines. Vias can be ignored if they are all the same. A maximum value for delay through a via to consider is 20ps. This number includes a delay based on the Z axis and time allocated to the LC delay. Use a more refined number if available; this generally requires a 3D solver.

## Timing Budgets

The table below lists parameters typically included in an address bus timing budget. The address A[15:0], bank address B[2:0], command (RAS#, CAS#, WE#), and control (CS#, ODT, CKE) signals are referred to as the CA bus. Separate tables for each group are acceptable. Simulation provides an eye. The simulation should include the clock and the CA bus, which allows a direct measurement of the setup and hold time for the simulation case. For most simulations, assume that the clock and CA bus are aligned at the source. If this is not the case, address the offset separately.

**Table 6: Address Timing Budget Example**

Ref	Parameter	Setup	Hold
A	Open address window from simulations	476ps	651ps
B	DRAM setup and hold requirements from the data sheet	45ps	120ps
C	Slew rate (V/ns)	2.3ps	2.8ps
D	Timing offset with respect to $V_{REFCA}$ (simulations placed $V_{REF}$ ideally) (this applies to setup)	13ps	–
E	Timing offset with respect to $V_{REFCA}$ (simulations placed $V_{REF}$ ideally) (this applies to hold)	–	11ps
F	DRAM derating	88ps	50ps
G	Crosstalk	47ps	42ps

**Table 6: Address Timing Budget Example (Continued)**

Ref	Parameter	Setup	Hold
H	Controller error (includes skew and all other errors attributed to the controller)	200ps	200ps
I	Clock error (this can be jitter [from all sources including cross-talk] or placement error if not included elsewhere)	30ps	30ps
J	Routing error	10ps	10ps
K	Margin	41ps	185ps

**Notes:**

1. Open address window (A) comes directly from simulations. For setup, the slow corner is simulated. This is typically at  $V_{DD}$  (min) and high temperature with slow silicon. These cases are in the spice and IBIS models. The fast corner, which is  $V_{DD}$  (max) and minimum temperature with fast silicon, applies to the hold case. It is generally not acceptable to only run the typical case. For DDR3, different thresholds are used for different speeds and voltages. Attention must be paid to using the correct thresholds when extracting the setup and hold margins from the simulations.
2. DRAM setup and hold values (B) come directly from the DRAM data sheet. Be sure to use the correct speed and voltage numbers.
3. Slew rate (C) is not used directly but is used to calculate derating values. See the DRAM data sheet for the slew rate definitions.
4. Timing offset with respect to  $V_{REFCA}$  (D and E) is to address the fact that the simulations use a single value for the threshold.  $V_{REFCA}$  has a tolerance of 1%,  $0.49 \times V_{DD}$  to  $0.51 \times V_{DD}$ . In addition, any noise that is on  $V_{REFCA}$  is added to this parameter. Micron uses 30mV as a typical error for  $V_{REFCA}$ . This includes both AC and DC contributors. To get to a value for the table, multiply the slew rate for the setup waveform by 30mV. The resulting value is added to the table.
5. DRAM derating (F) uses the slew rate to adjust the actual setup and hold time required by the device. See the DRAM data sheet for the derating procedure.
6. Crosstalk (G) can be handled several ways. If the simulation is performed with coupling turned on, it is included in the setup and hold values from the simulation waveform (A). Another method is to run a separate simulation on fewer signals, and then determine which is likely the worst-case signal. This can be done by simulation or visual inspection using the result in the timing budget.
7. Controller error (H) can generally be found in the data sheet for the controller.
8. Clock error (I) assumes that this is a separate parameter from skew attributed to the controller. If included in the controller, it can be ignored.
9. Routing error (J) assumes that only one trace was simulated. Add any differences in routing length between the simulated trace and the fastest and slowest traces here. Usually, either all traces are simulated, or just the fastest and slowest traces are simulated, resulting in a value of zero.
10. Margin (K) is simply the open address window (A) parameter minus all other parameters. If the result is positive, there is margin. If there is a large difference between the setup and hold margin, it may be appropriate to skew the clock to get a more even margin.

There is nothing in this budget to allocate toward  $V_{DD}$  noise. Since the DRAM specification includes noise in the test fixture, some noise is included. Because the environment for the test fixture and the application are different, additional  $V_{DD}$  noise is not account-

ted for. If the other guidelines in this document are followed, this should be small enough to ignore.

## Write Leveling and Training

Write leveling is a new feature for DDR3, intended for applications that use the daisy-chain topology for the clock. For an application where memory is only placed on the main board, write leveling is only useful if four or more DRAM devices are placed on the same side of the PCB using a daisy-chain topology for the clock.

With the daisy-chain topology and four devices, the clock at each device is offset 150ps to 200ps from the adjacent devices. The first device has a clock offset 450ps to 600ps from the clock at the last device. The major implication is that the DQ bus needs to be skewed per byte lane (per 16 bits for x16 devices) to meet  $t_{DQSCk}$  for writes. The controller must provide the skew.

The following three options are available to address this skew requirement:

1. Use a series of reads and writes to fine-tune the skew (preferred).
2. Predict or measure the skew one time, and apply it universally to the design.
3. Use the write leveling feature to determine the skew for each PCB.

Write leveling does not provide a very tight definition of the clock skew. The setup and hold requirements provide a good indication of the uncertainty, which varies with the maximum speed of the DRAM device.

## Drive Strength and Calibration

DDR3 has two drive strengths: 40Ω and 34Ω. DRAM devices from some manufacturers may support 48Ω. DDR3 is designed to match the driver to the transmission line. With a 40Ω driver, the intended transmission line is 40Ω. The advantage of matching the driver to the transmission line is that it eliminates the reflections that return to the driver. The result is cleaner edges and a more open eye.

To achieve a driver near 40Ω, calibration is necessary. To maintain tight calibration, recalibrate periodically. There are commands to initiate calibration. For smaller systems where tight tolerance is not necessary, the initial calibration may be all that is required. However, this allows the driver impedance to vary with voltage and temperature.

See Micron technical note, TN-41-02: DDR3 ZQ Calibration, for a better understanding of calibration.

See the Terminating Point-to-Point Systems section to learn the effects of mismatching a driver to the transmission line.

## ODT Values/Calibration

The termination resistances 120Ω, 60Ω, 40Ω, 30Ω, and 20Ω are calibrated at the same time as the output drivers. DDR3 has different termination resistances that provide a better match compared to DDR2. Because these values are also adjusted through ZQ calibration, it is important to perform periodic calibration to keep the ODT termination resistances within the data sheet values.

The models that Micron provides assume that calibrations are done periodically. The slow corner uses a maximum ODT tolerance, and the fast corner uses a minimum ODT tolerance. If periodic calibration will not be performed, contact Micron for additional information.

## Data Bus Topologies

The DDR3 DQ bus is similar to DDR2 in terms of the actual routing. However, DDR3 uses wider traces in general (lower impedance) and has more separation in practice. The improvements are in the controllers and the DRAM devices themselves. The DDR3 features may lead to different trade-offs. For DDR3, the DQ bus is 25mm to 75mm (1 inch to 3 inches). Generally, DQ buses in the range of 40Ω with drive strengths of 34Ω or 40Ω provide the greatest margin.

The improvements in the controller are reduced skew, improved setup and hold, improved package parasitic, improved calibration, and added adjustment and training features. Not all controllers have these features.

Improvements in the DRAM device are reduced skew, reduced setup and hold, improved package parasitic, improved calibration, and improved support for training.

The terminations are on-die, either in the controller or the DRAM device, with a termination resistance near the transmission line impedance.

## Terminating Point-to-Point Systems

DDR3 point-to-point systems require terminating techniques similar to DDR2, with additional attention paid to the small details because of faster data rates. It is imperative that simulations be performed to verify the termination assumptions chosen.

For point-to-point applications, a 34Ω driver with a 40Ω transmission line and a 60Ω termination provides the best, or near-best, solution. There is some mismatch, but with the DRAM and controller packages included, it provides the best solution. The four cases in the table below all provide good results. There is no crosstalk in these four cases, which must be considered as well. The more mismatch in the termination, the more crosstalk.

**Table 7: ODT Termination Table for Simple Configurations (40Ω Transmission Line)**

Case	Operation	Controller	DRAM	Comments
1	READ	Term 60	Driving 34Ω	–
2	WRITE	Driving 34Ω	Term 40Ω	–
3	WRITE	Driving 34Ω	Term 60Ω	–
4	WRITE	Driving 34Ω	Term 120Ω	Allows more crosstalk

If an application has enough margin, a higher bus impedance may be considered: 45Ω, 50Ω, or 60Ω. For all of these cases, the driver should be 40Ω and the termination should be 60Ω. The reference plane may be  $V_{SSQ}$  or  $V_{DDQ}$ . Choose one or the other for each DRAM device. The DRAM package operates equally for either choice. If the controller has a preference, it can drive the decision. What is convenient to measure may also drive the decision.

DQS timing may be a special consideration. If the controller has the capability of skewing DQS relative to DQ, the DQS length can match the DQ lengths loosely. If the controller does not have this capability, the routing length is more critical. A differential signal routed with the same width trace as the DQ signals has an impedance that is a little less than twice the single-ended impedance. This results in a difference in the rise time that



creates an offset. Simulations are the only practical method of determining the offset. If the differential traces are thinner than the single-ended DQ traces such that the differential impedance is twice the single-ended impedance, the rise times should be the same and there should not be an offset. For the outer layers, the difference in flight time is about 10% with the inner layers being slower. This needs to be accounted for if the signals are routed on an outer layer. Because simulations must account for the differences in rise time, use them to provide the flight time differences as well. For the simulations to be accurate, the PCB stackup must be correct.

The following ADDR/CMD/CNTL buses and data bus discussions have examples showing termination techniques simulated for a DDR3-1333 point-to-point system. Topology, layout, and device parasitics each play a significant role in obtaining good signal quality. Thus, these simulations are intended for comparison purposes, and the termination values are not a recommendation for any specific point-to-point design.

## Bus Termination Overview

Terminating point-to-point buses is generally straightforward: match the impedance of the driver to the line impedance of the transmission line. As a general rule, it is acceptable to use a slightly lower series R for a stronger drive. For single-direction buses, like address and command buses, it is optimal to place a series resistor near the driver. Adequate results may be seen even with the resistor placed near the middle of the bus. Data buses are a bit trickier because the transmission line is bidirectional; therein lies the beauty of ODT.

Prior to implementing, it is imperative to simulate a chosen termination scheme. Varying driver strengths with trace characteristics can help find an optional combination.

## ADDR/CMD/CNTL Bus Termination

When terminating ADDR/CMD/CNTL buses in point-to-point systems, there are a variety of options:

- Tree with  $V_{TT}$  R (Figure 3)
- Tree with series R (Figure 4)
- Tree without series R (Figure 5)
- Fly-by (Figure 6)

Although the tree with  $V_{TT}$  R option provides the best signal, it is generally overkill in a point-to-point system. The tree with series R provides acceptable signal quality without having to provide  $V_{TT}$  power when there is a mismatch between the driver and transmission line. The tree without series R option generally provides acceptable signal quality without having to provide  $V_{TT}$  power when there is a minimal mismatch between the driver and transmission line. The fly-by option also has acceptable signal quality, providing ease of layout at the expense of  $V_{TT}$  power and termination; it also induces a skew between the clock and the data bus.

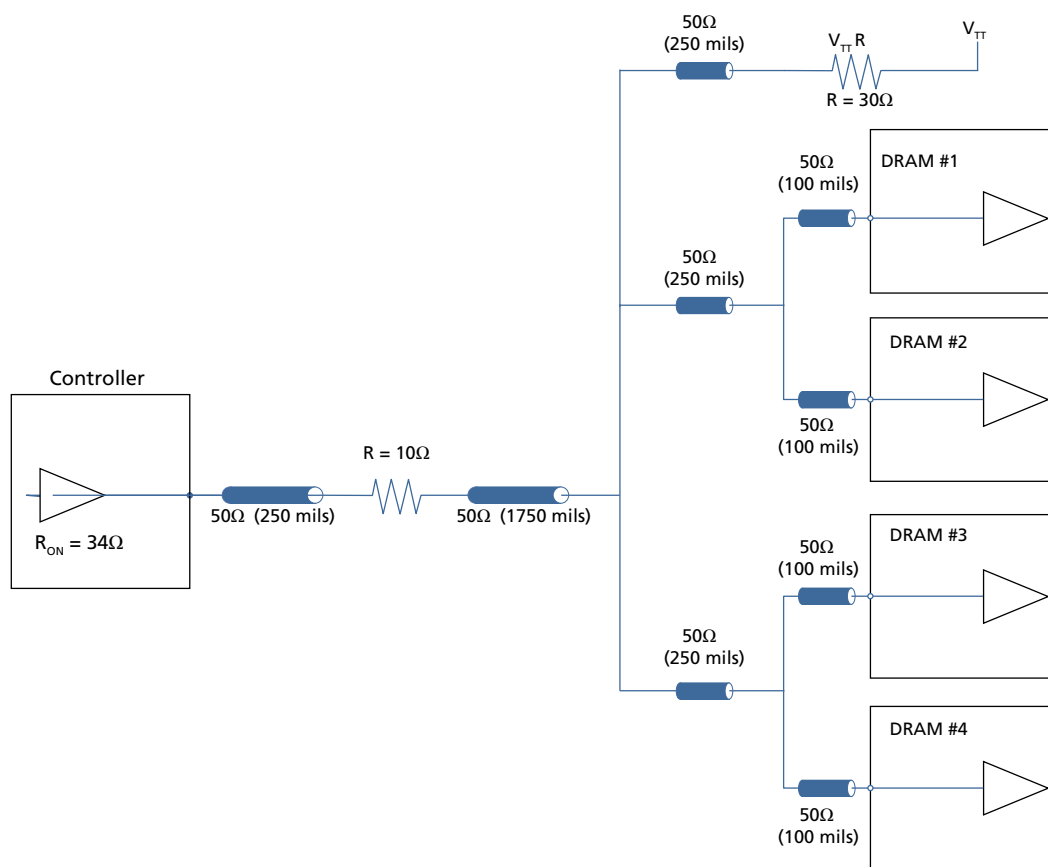
Each tactic has its advantages and disadvantages. The best termination technique to use depends on the design requirements.

When using the tree approach, the driver impedance and the series R should be slightly less than the trace impedance. If using the fly-by approach, terminate the last device to  $V_{TT}$ . Assuming a simple point-to-point system, each of the above termination schemes were simulated, and the results are shown in Figure 6 and the values are summarized in the table below.

**Table 8: CMD/ADDR/CNTL Bus Termination**

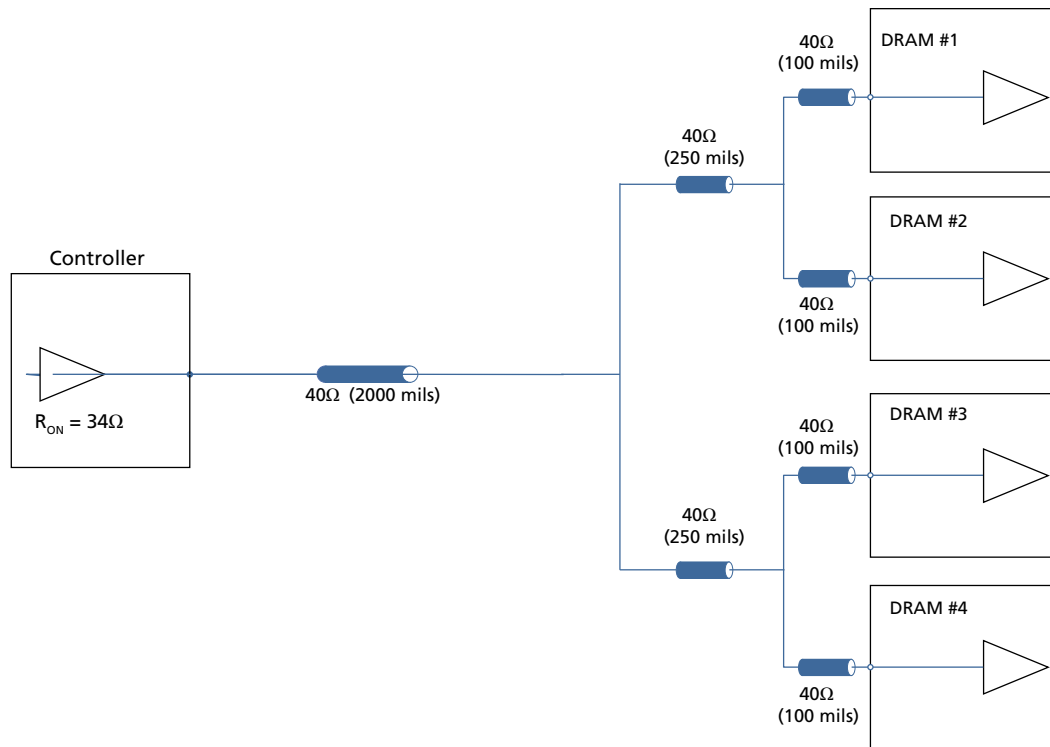
Termination	Jitter	Aperture	Slew	Voltage Margin
Tree – $V_{TT} R$	5ps	1.32ns	1.5 V/ns	140mV
Tree – No R	28ps	1.39ns	1.7 V/ns	510mV
Tree – $10\Omega R$	33ps	1.34ns	2.2 V/ns	560mV
Fly-by	5ps	1.37ns	2.2 V/ns	100mV

**Figure 4: Tree Architecture with CMD/ADDR/CNTL Buses –  $V_{TT} R$  with Series R**

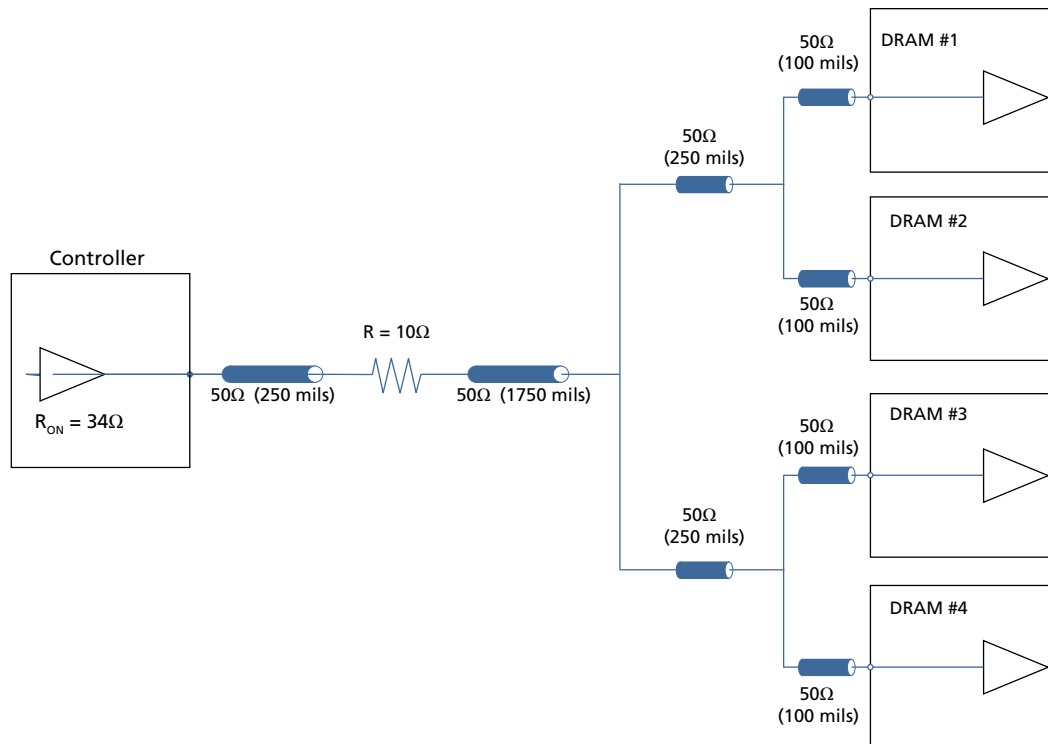




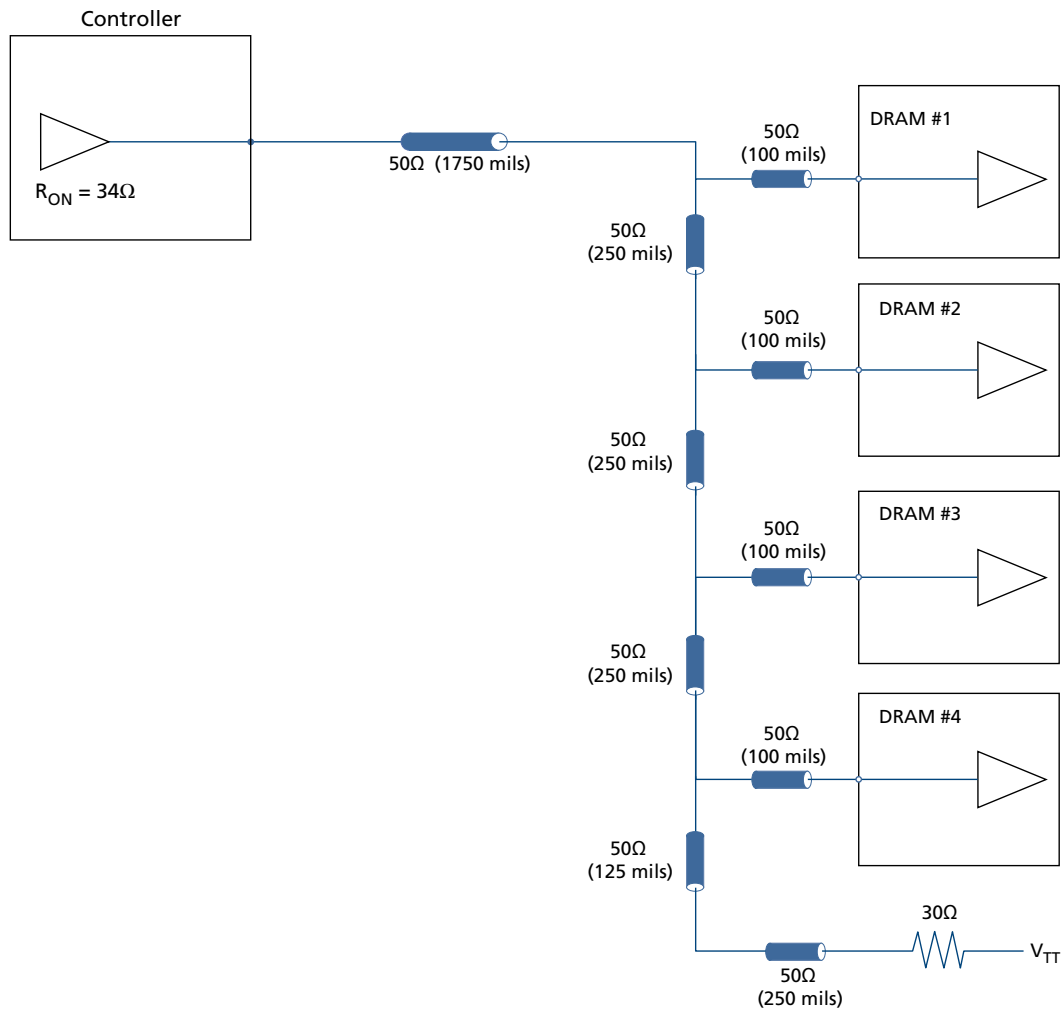
**Figure 5: Tree Architecture with CMD/ADDR/CNTL Buses – Without Series R**



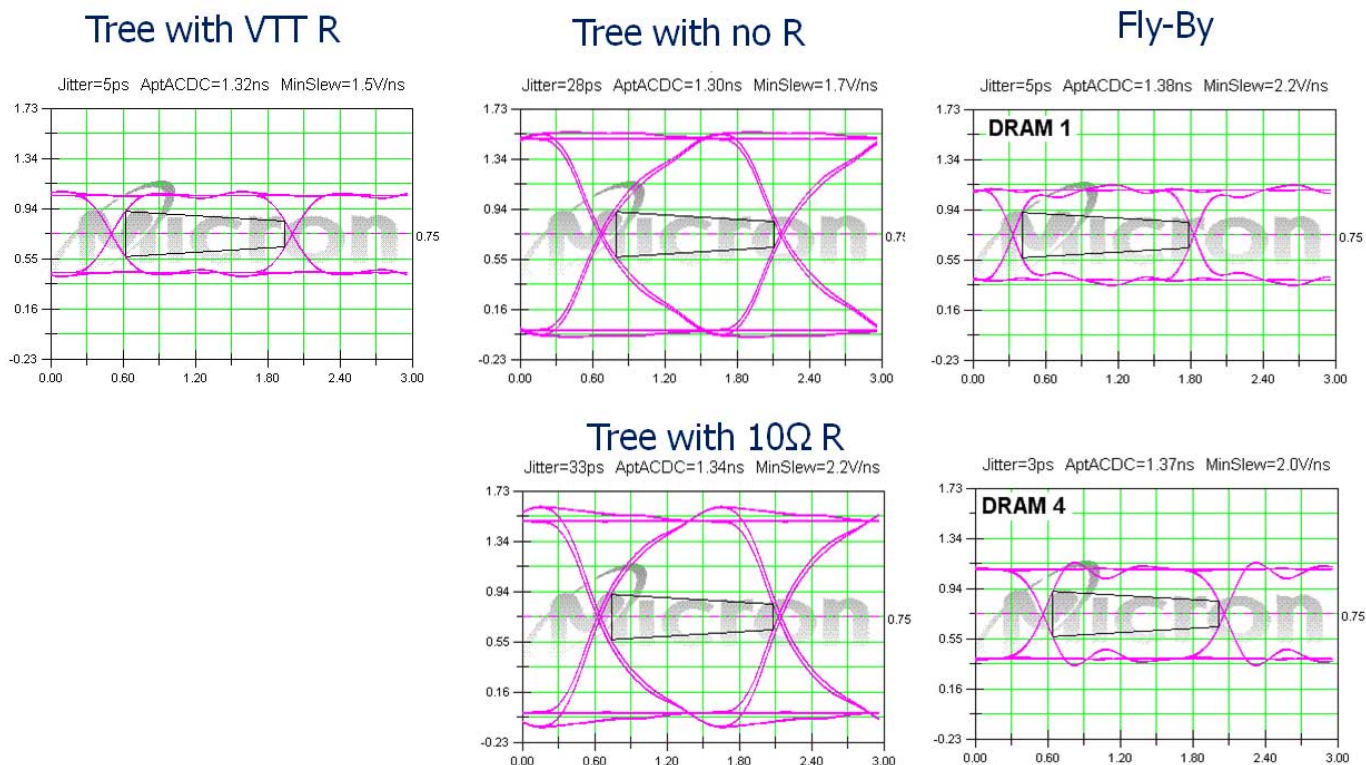
**Figure 6: Tree Architecture with CMD/ADDR/CNTL Buses – With Series R**



**Figure 7: Fly-By Architecture with CMD/ADDR/CNTL Buses**



**Figure 8: Tree vs. Fly-By Termination on CMD/ADDR/CNTL Buses Simulations at DDR3-1333**



## Data Bus Termination

When terminating the data bus in point-to-point systems, there are essentially two options:

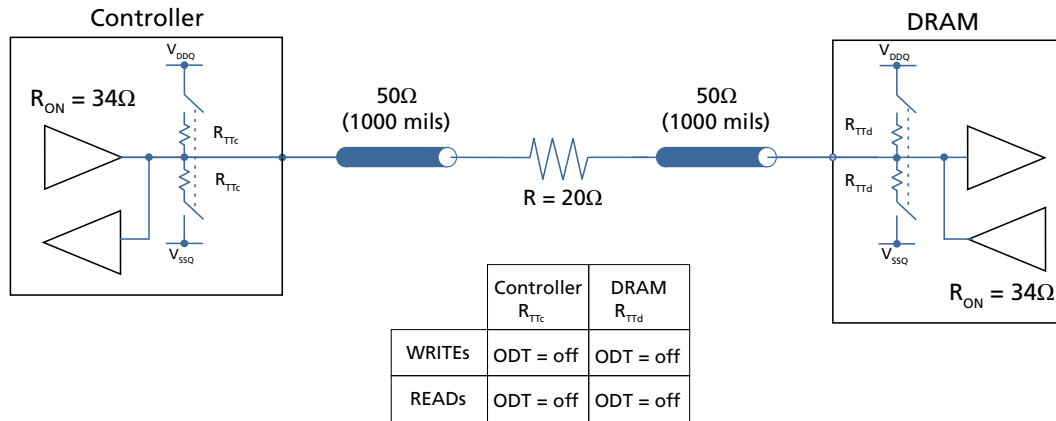
- Series R (Figure 8)
- Direct connect using ODT (Figure 9)

Additionally, DDR3 supports two output drive impedance settings—34Ω and 40Ω—to obtain better impedance matching to the transmission line during DRAM reads.

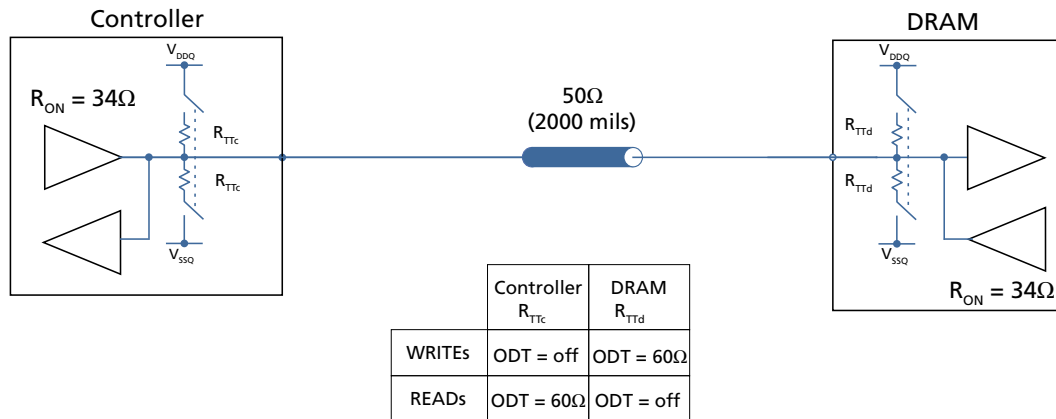
Series R generally provides acceptable signal quality without having to provide ODT power through the DRAM device and controller for power savings. Series R should be placed in the center of the transmission line between the controller and the DRAM device. The series R termination scheme becomes increasingly more difficult when the data bus exceeds 2in.

The direct connect with ODT provides better signal quality and lower cost compared to series R. For ODT during writes, 40Ω, 60Ω, or 120Ω can be used with  $R_{TT\_NOM}$  versus 60Ω or 120Ω with  $R_{TT\_WR}$ . In most cases, 60Ω provides the best signaling. If two loads per DQ bit are designed in, and using  $R_{TT\_NOM}$  or  $R_{TT\_WR}$  alone does not provide an adequate data eye, toggling  $R_{TT\_NOM}$  (low R) with  $R_{TT\_WR}$  (large R) between the two ranks may improve the data eye. See Micron's DDR3-1333 UDIMM Design Guide.

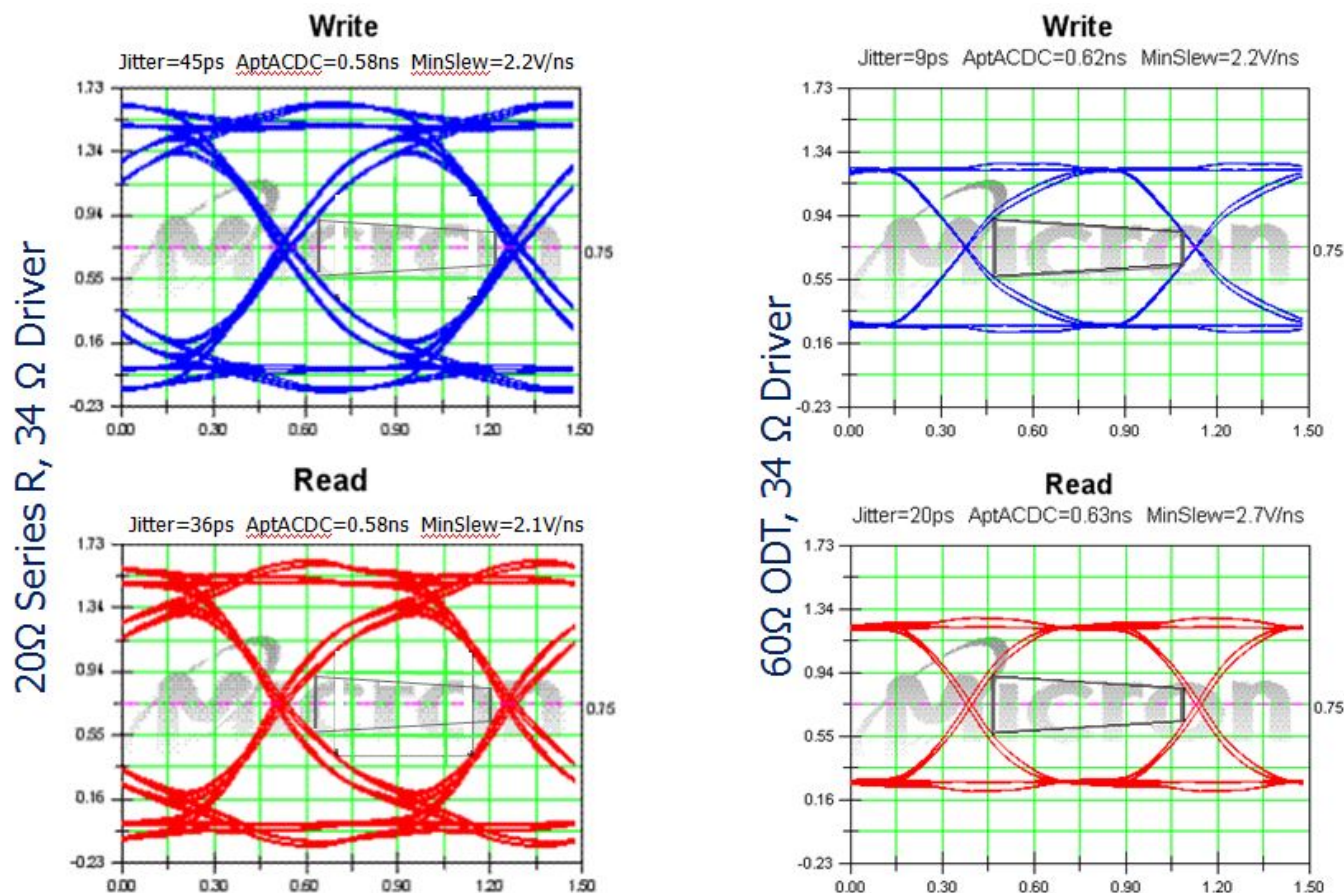
**Figure 9: Data Bus Termination with Series R**



**Figure 10: Data Bus Termination with Direct Connect Using ODT**



**Figure 11: Series R vs. ODT Termination on Data Bus Simulations for DDR3-1333**



**Table 9: Data Bus Terminations**

Termination	DRAM Access	Jitter	Aperture	Slew	Voltage Margin
Series R	Writes	45ps	580ps	2.2 V/ns	380mV
ODT	Writes	9ps	620ps	2.2 V/ns	250mV
Series R	Reads	36ps	580ps	2.1 V/ns	310mV
ODT	Reads	20ps	630ps	2.7 V/ns	270mV

## Other DDR3 Point-to-Point System Considerations

### Bandwidth

Micron's DDR3 devices define input clock rate targets of 400 MHz (DDR3-800), 533 MHz (DDR3-1066), 667 MHz (DDR3-1333), 800 MHz (DDR3-1600), 933 MHz (DDR3-1866), and 1067 MHz (DDR3-2133). DDR3L is only JEDEC-defined up to 800 MHz (DDR3-1600). These rates translate to high bandwidth for the data bus with up to

1600 MT/s/pin or 12.8 GB/s for a 64-bit bus. Regardless of the upper speed limit, all DDR3 devices operate down to 300 MHz with the DLL enabled. The slower clock helps with the initial design bring-up or debug process, and it assists the system's test engineer throughout the life of the product. Additionally, the slower operating frequency can greatly reduce overall power consumption.

## High-Temperature Operation

Many point-to-point systems operate in adverse system environments where the operating conditions are extreme. DDR3 supports an upper temperature limit of 95°C (<sup>t</sup>CASE) compared to 85°C (<sup>t</sup>CASE) for DDR2. When the temperature operation exceeds 85°C, the device requires a higher refresh rate. The standard periodic refresh interval (<sup>t</sup>REFI) is 7.8  $\mu$ s (that is, 64 ms for the full array) for all DDR3 densities. However, when operating DDR2 devices above a <sup>t</sup>CASE of 85°C, the periodic refresh interval (<sup>t</sup>REFI) changes from 7.8  $\mu$ s to 3.9  $\mu$ s (that is, 32 ms for the full array). To ensure that the self refresh also performs at the increased refresh rate, configure the device at its initialization sequence to enable either auto self refresh (ASR) or self refresh temperature (SRT).

## Addressing

The majority of point-to-point designs do not utilize high-density memory, but after the layout is complete and released to production, the product life spans several DDR3 density crossovers. Throughout these transitions, it may be more cost-effective to change to a higher-density part. DDR3 addressing makes this transition easy because the page size for all components is either 1KB (x4, x8) or 2KB (x16). As long as the controller is initially set up to handle no-connects or unused pins correctly, migrating to the next density is fairly easy. See Figure 11 for address mapping.

In addition to addressing changes, the refresh period must be accounted for. As the densities increase, the refresh period (<sup>t</sup>RFC) increases as shown in the following table:

**Table 10: DDR3 Refresh Rates**

Parameter	512Mb	1Gb	2Gb	4Gb	8Gb
<sup>t</sup> RFC	90 ns	110 ns	160 ns	300 ns	350 ns



**Figure 12: DDR3 Addressing for Compatibility**

Configuration	Addresses	Used / Not used
512Mb (x4)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 BA0 BA1 BA2
512Mb (x4)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) BA0 BA1 BA2
1Gb (x4)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 BA0 BA1 BA2
1Gb (x4)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 BA0 BA1 BA2
2Gb (x4)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 BA0 BA1 BA2
2Gb (x4)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 BA0 BA1 BA2
4Gb (x4)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2
4Gb (x4)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 A15 BA0 BA1 BA2
8Gb (x4)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2
8Gb (x4)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 A15 BA0 BA1 BA2

512Mb (x8)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 BA0 BA1 BA2
512Mb (x8)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) BA0 BA1 BA2
1Gb (x8)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 BA0 BA1 BA2
1Gb (x8)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 BA0 BA1 BA2
2Gb (x8)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 BA0 BA1 BA2
2Gb (x8)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 BA0 BA1 BA2
4Gb (x8)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2
4Gb (x8)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 A15 BA0 BA1 BA2
8Gb (x8)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2
8Gb (x8)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 A15 BA0 BA1 BA2

512Mb (x16)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 BA0 BA1 BA2
512Mb (x16)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) BA0 BA1 BA2
1Gb (x16)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 BA0 BA1 BA2
1Gb (x16)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) BA0 BA1 BA2
2Gb (x16)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 BA0 BA1 BA2
2Gb (x16)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 BA0 BA1 BA2
4Gb (x16)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 BA0 BA1 BA2
4Gb (x16)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 BA0 BA1 BA2
8Gb (x16)	ROW	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 BA0 BA1 BA2
8Gb (x16)	COL	A0 A2 A3 A3 A4 A5 A6 A7 A8 A9 (AP) A11 (BC) A13 A14 A15 BA0 BA1 BA2



## Conclusion

DDR3 SDRAM design requirements are similar to DDR2 except DDR3 supports operation at twice the clock and data rate. DDR3 provides significant improvement in output drive and ODT characteristics to help achieve faster data rates. Point-to-point systems benefit from the larger driver impedance options as well as the tighter ranges. The dynamic ODT offering makes ODT support very easy. It seems that dynamic ODT was added to DDR3 just for point to-point design support—it is that helpful.

When implementing termination, point-to-point designs have some flexibility. Depending on the system constraints, the best option can usually be chosen. The experienced DDR2 point-to-point designer should find designing DDR3 point-to-point systems rather easy.

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