Bài 1:

1 block = 256 byte = 2^8 byte

Cache = 4MB = 16384 block = 2^14 block

Các trường có thứ tự lần lượt là Tag - index - offset

(a) Direct Mapped

- 8bit byte-offset
- 14bit index
- 10bit tag

(b) 4-way set associative

- 1 set có 4 block
- =>8bit byte-offset
- 12bit index
- 12bit tag

(c)Fully

- chỉ có 1 set trong cache và có 16384 block
- => 8bit byte-offset
- 0bit index (vì chỉ có 1 set)
- 24bit tag

Bài 2:

1 block 64 words = 128 half word = 2^7 half-word

cache = 256KB = 1024 blocks = 2^10 blocks

(a)

- 7bit half-word offset
- 10bit index
- 11bit tag

(b)

- 1 set có 4block :
- 7bit half-word offset
- 8bit index
- 13bit tag

(c)

- duy nhất 1 set có 2^11 blocks
- 7bit half-word offset
- 0bit index
- 21bit tag

Bài 3:

(a) 1 block = 4 words

Cache = 256byte = 16block = 16 set = 2^4 => 4 bit Index

Number	Tag	Index	Miss/Hit
0	0	0	Miss
4	0	1	Miss
1	0	0	Hit
5	0	1	Hit
65	1	0	Miss
1	0	0	Miss
67	1	0	Miss
46	0	11	Miss
1	0	0	Miss
70	1	1	Miss
2	0	0	Hit
0	0	0	Hit

Hit = 4, Miss = 8

(b)1 set có 2 block => 1 set = 8 word;

Index = 256/8*4 = 8 = 2^3 => 3 bit Index

Number	Tag	Index	Miss/Hit
0	0	0	Miss
4	0	1	Miss
1	0	0	Hit
5	0	1	Hit
65	2	0	Miss
1	0	0	Hit
67	2	0	Hit
46	1	3	Miss
1	0	0	Hit
70	2	1	Miss
2	0	0	Hit
0	0	0	Hit

Hit = 7, Miss = 5

(c) Duy nhất 1 set 16 blocks => 0 bit Index

Number	Tag	Index	Miss/Hit
0	0	0	Miss
4	1	0	Miss
1	0	0	Hit
5	1	0	Hit
65	16	0	Miss
1	0	0	Hit
67	16	0	Hit
46	11	0	Miss
1	0	0	Hit
70	17	0	Miss
2	0	0	Hit
0	0	0	Hit

Hit = 7, Miss = 5

Bài 4:

AMAT = Hit time + Miss rate*Miss penalty

Clock rate = 2GHz => T_{CR} = 0.5 (ns)

Hit time = 5 T_{CR} = 2.5 (ns)

Miss penalty = 10 (ns)

+ Direct Mapped: AMAT = 2.5 + 8/12 * 10 = 9.166667 (ns)

+ 2-way set associative: AMAT = 2.5 + 5/12*10 = 6.66667 (ns)

+ Fully associative: AMAT = 2.5 + 5/12*10 = 6.66667 (ns)

Bài 5:

L1 Hit time = 10 T_{CR} , L2 Hit time = 15 T_{CR}

L1 Miss rate = 20%, L2 Miss rate = 10%

L2 penalty = RAM access time = 100 T_{CR}

L1 penalty = L2 AMAT

L2 AMAT = 15 T_{CR} + 10% * 100 T_{CR} = 25 T_{CR}

System AMAT = L1 AMAT = 10 T_{CR} + 20% * 25 T_{CR} = 15 T_{CR}

Bài 6:

Số chu kỳ miss/1 IC:

I-cache = 0.05*100 = 5 cycles

D-cache = 0.1*0.1*100 = 1 cycle

=> Tổng cycles cho I và D cache trong 1 IC = 6 cycles

CPI theo đề : 1004/1000 = 1.004

=> CPI trung bình = 1.004+6 = 7.004