ECGR 4146 Introduction to VHDL
Lab 2
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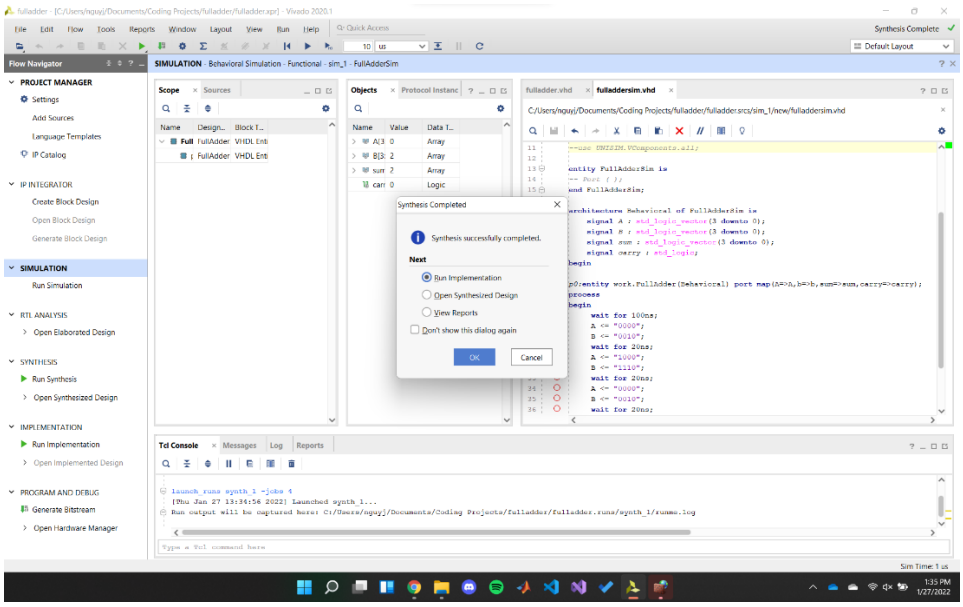
1. **Take a screenshot of Vivado screen after you have run synthesis, and the simulation**

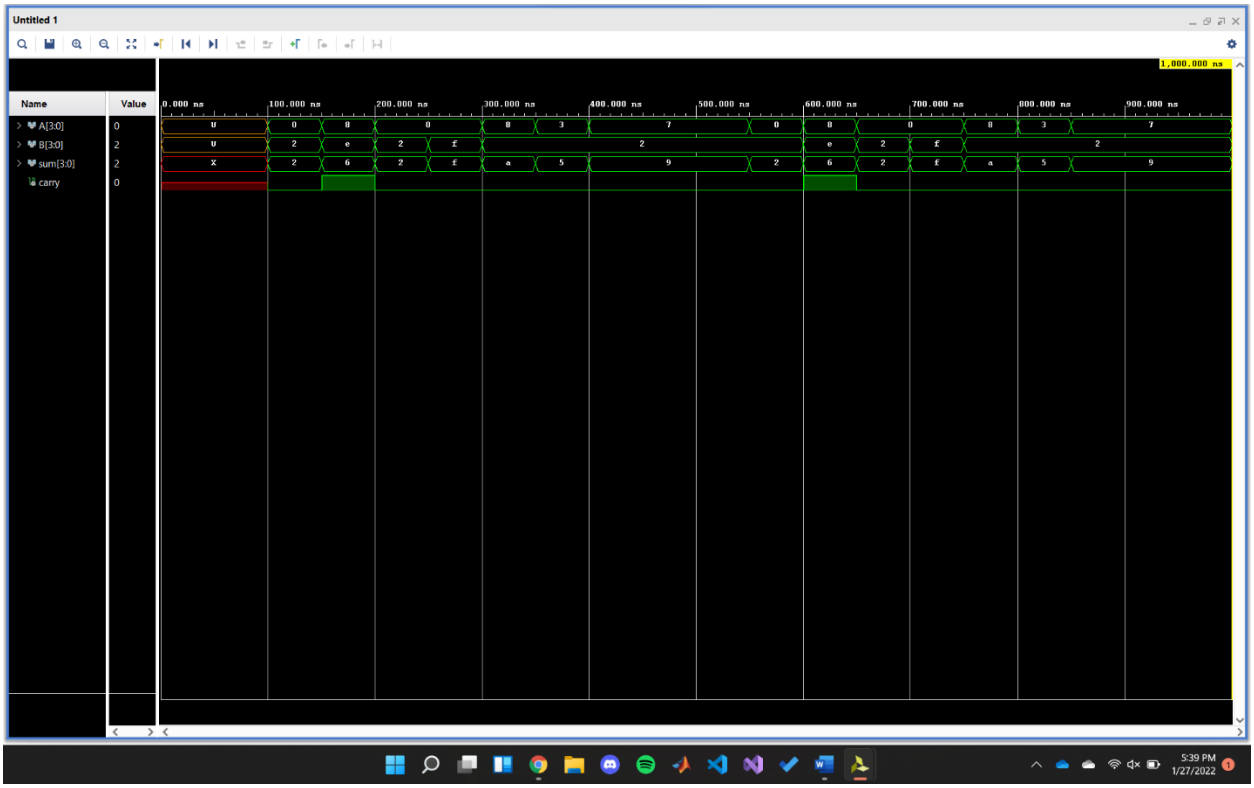
I added the full adder code to fulladder.vhd and added the testbench code to fulladdersim.vhd. I ran the synthesis on the code and screenshotted the completed screen. Then I ran the a simulation on the full adder code.



Synthesis screenshot

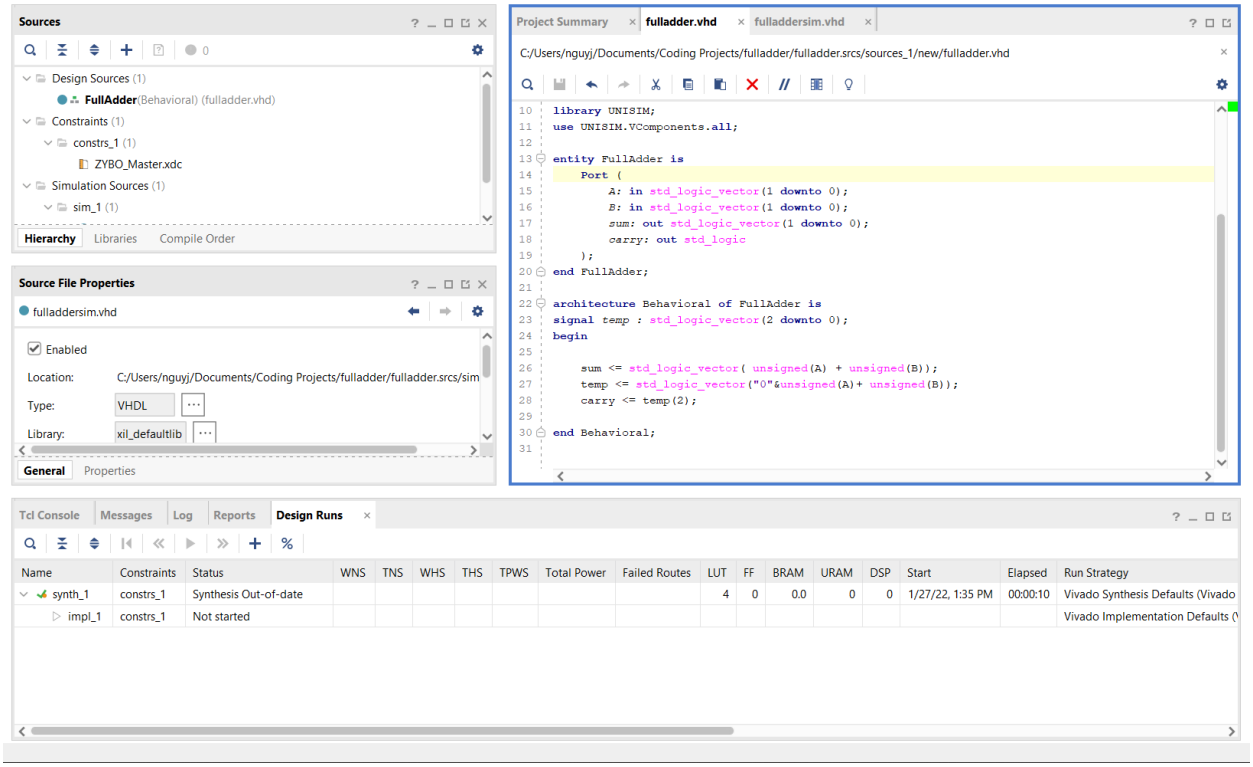
Simulation screenshot.

During the lab checkout, I changed the testbench to include more test and changed some of the old test. These are the simulation results.



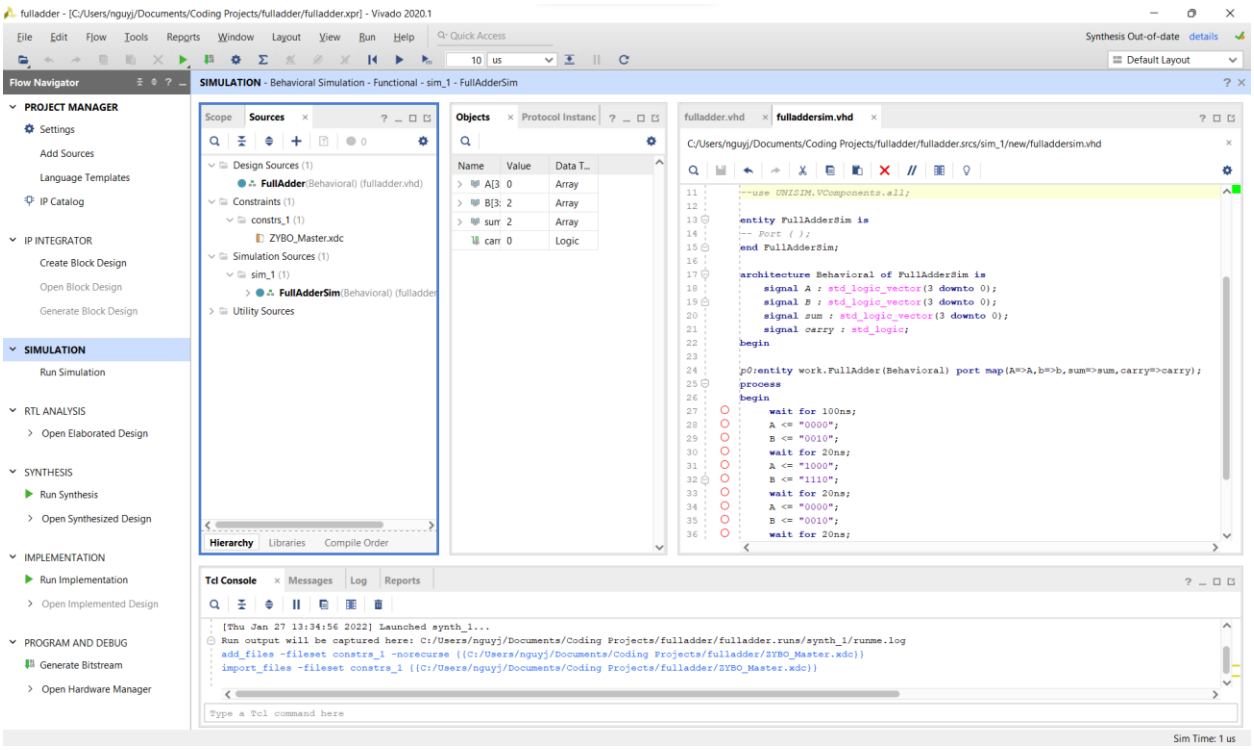
2. **Once done with the simulation you need to make some changes in the adder.vhd code to generate the bitstream.**

Here I made the adjustments to the code. The changes are found on the right side of the screenshot. The changes that was made was to change the both input to 2 bits and the output to 2 bits. Also in the archtecture the temp signal was uses 3 bits instead of 5 bits.



3. Add the constraint file provided in the constraint tab of vivado.

I downloaded the constraint file from canvas. Then went to add sources and added the constaint file. This is a screenshot of the constraint file in the project tab on the left of the picture.



4. Run synthesis, post place and route, and Generate Bitstream successfully.

I ran the synthesis, implemation and generated the bitstream. This is a screenshot of the completion screen of the generating the bitstream.