CMOS VLSI Design

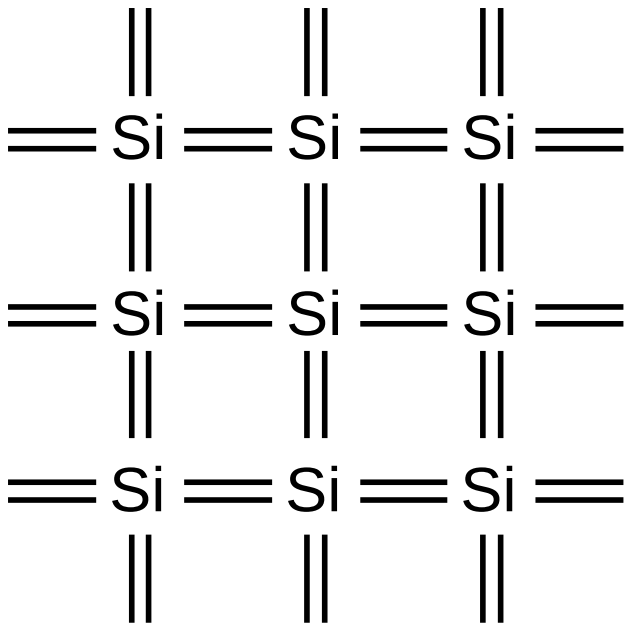
Introduction

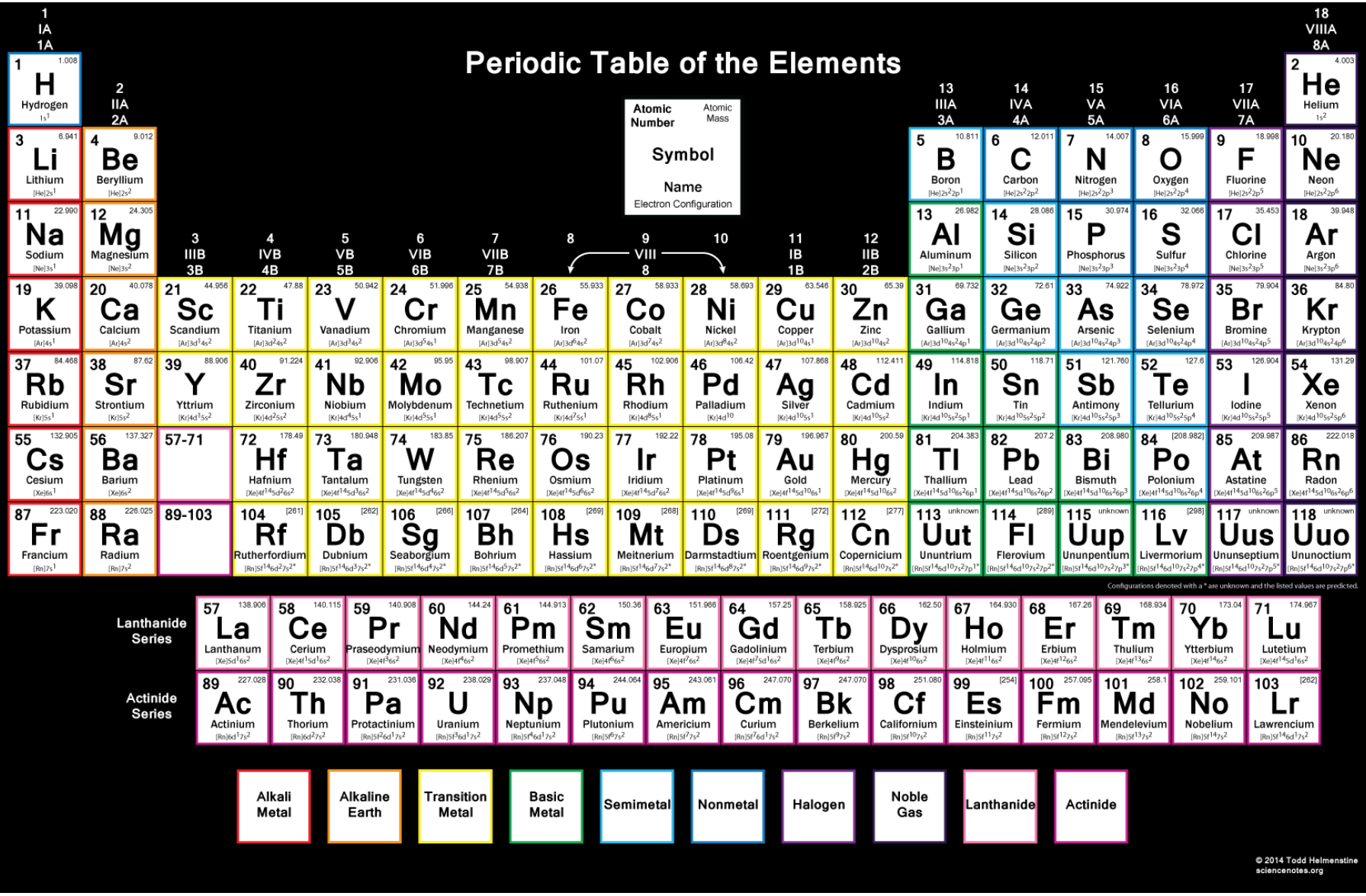
Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- This chapter: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors




Periodic Table of the Elements
Atomic Number
Atomic Mass
Symbol
Name
Electron Configuration
1 IA 1A
2 IIA 2A
3 IIIB 3B
4 IVB 4B
5 VB 5B
6 VIB 6B
7 VIIB 7B
8 9 10 VIII 8
11 IB 1B
12 IIB 2B
13 IIIA 3A
14 IVA 4A
15 VA 5A
16 VIA 6A
17 VIIA 7A
18 VIIIA 8A
1 1.008 H Hydrogen 1s1
2 4.003 He Helium 1s2
3 6.941 Li Lithium [He]2s1
4 9.012 Be Beryllium [He]2s2
5 10.811 B Boron [He]2s22p1
6 12.011 C Carbon [He]2s22p2
7 14.007 N Nitrogen [He]2s22p3
8 15.999 O Oxygen [He]2s22p4
9 18.998 F Fluorine [He]2s22p5
10 20.180 Ne Neon [He]2s22p6
11 22.990 Na Sodium [Ne]3s1
12 24.305 Mg Magnesium [Ne]3s2
13 26.982 Al Aluminum [Ne]3s23p1
14 28.086 Si Silicon [Ne]3s23p2
15 30.974 P Phosphorus [Ne]3s23p3
16 32.066 S Sulfur [Ne]3s23p4
17 35.453 Cl Chlorine [Ne]3s23p5
18 39.948 Ar Argon [Ne]3s23p6
19 39.098 K Potassium [Ar]4s1
20 40.078 Ca Calcium [Ar]4s2
21 44.956 Sc Scandium [Ar]3d14s2
22 47.88 Ti Titanium [Ar]3d24s2
23 50.942 V Vanadium [Ar]3d34s2
24 51.996 Cr Chromium [Ar]3d54s1
25 54.938 Mn Manganese [Ar]3d54s2
26 55.933 Fe Iron [Ar]3d64s2
27 58.933 Co Cobalt [Ar]3d74s2
28 58.693 Ni Nickel [Ar]3d84s2
29 63.546 Cu Copper [Ar]3d104s1
30 65.39 Zn Zinc [Ar]3d104s2
31 69.732 Ga Gallium [Ar]3d104s24p1
32 72.61 Ge Germanium [Ar]3d104s24p2
33 74.922 As Arsenic [Ar]3d104s24p3
34 78.972 Se Selenium [Ar]3d104s24p4
35 79.904 Br Bromine [Ar]3d104s24p5
36 84.80 Kr Krypton [Ar]3d104s24p6
37 84.468 Rb Rubidium [Kr]5s1
38 87.62 Sr Strontium [Kr]5s2
39 88.906 Y Yttrium [Kr]4d15s2
40 91.224 Zr Zirconium [Kr]4d25s2
41 92.906 Nb Niobium [Kr]4d45s1
42 95.95 Mo Molybdenum [Kr]4d55s1
43 98.907 Tc Technetium [Kr]4d55s2
44 101.07 Ru Ruthenium [Kr]4d75s1
45 102.906 Rh Rhodium [Kr]4d85s1
46 106.42 Pd Palladium [Kr]4d10
47 107.868 Ag Silver [Kr]4d105s1
48 112.411 Cd Cadmium [Kr]4d105s2
49 114.818 In Indium [Kr]4d105s25p1
50 118.71 Sn Tin [Kr]4d105s25p2
51 121.760 Sb Antimony [Kr]4d105s25p3
52 127.6 Te Tellurium [Kr]4d105s25p4
53 126.904 I Iodine [Kr]4d105s25p5
54 131.29 Xe Xenon [Kr]4d105s25p6
55 132.905 Cs Cesium [Xe]6s1
56 137.327 Ba Barium [Xe]6s2
57-71
72 178.49 Hf Hafnium [Xe]4f145d26s2
73 180.948 Ta Tantalum [Xe]4f145d36s2
74 183.85 W Tungsten [Xe]4f145d46s2
75 186.207 Re Rhenium [Xe]4f145d56s2
76 190.23 Os Osmium [Xe]4f145d66s2
77 192.22 Ir Iridium [Xe]4f145d76s2
78 195.08 Pt Platinum [Xe]4f145d96s1
79 196.967 Au Gold [Xe]4f145d106s1
80 200.59 Hg Mercury [Xe]4f145d106s2
81 204.383 Tl Thallium [Xe]4f145d106s26p1
82 207.2 Pb Lead [Xe]4f145d106s26p2
83 208.980 Bi Bismuth [Xe]4f145d106s26p3
84 [208.982] Po Polonium [Xe]4f145d106s26p4
85 209.987 At Astatine [Xe]4f145d106s26p5
86 222.018 Rn Radon [Xe]4f145d106s26p6
87 223.020 Fr Francium [Rn]7s1
88 226.025 Ra Radium [Rn]7s2
89-103
104 [261] Rf Rutherfordium [Rn]5f146d27s2*
105 [262] Db Dubnium [Rn]5f146d37s2*
106 [266] Sg Seaborgium [Rn]5f146d47s2*
107 [264] Bh Bohrium [Rn]5f146d57s2*
108 [269] Hs Hassium [Rn]5f146d67s2*
109 [268] Mt Meitnerium [Rn]5f146d77s2*
110 [269] Ds Darmstadtium [Rn]5f146d87s2*
111 [272] Rg Roentgenium [Rn]5f146d97s2*
112 [277] Cn Copernicium [Rn]5f146d107s2*
113 unknown Uut Ununtrium [Rn]5f146d107s27p1*
114 [289] Fl Flerovium [Rn]5f146d107s27p2*
115 unknown Uup Ununpentium [Rn]5f146d107s27p3*
116 [298] Lv Livermorium [Rn]5f146d107s27p4*
117 unknown Uus Ununseptium [Rn]5f146d107s27p5*
118 unknown Uuo Ununoctium [Rn]5f146d107s27p6*
Configurations denoted with a * are unknown and the listed values are predicted.
Lanthanide Series
57 138.906 La Lanthanum [Xe]5d16s2
58 140.115 Ce Cerium [Xe]4f15d16s2
59 140.908 Pr Praseodymium [Xe]4f36s2
60 144.24 Nd Neodymium [Xe]4f46s2
61 144.913 Pm Promethium [Xe]4f56s2
62 150.36 Sm Samarium [Xe]4f66s2
63 151.966 Eu Europium [Xe]4f76s2
64 157.25 Gd Gadolinium [Xe]4f75d16s2
65 158.925 Tb Terbium [Xe]4f96s2
66 162.50 Dy Dysprosium [Xe]4f106s2
67 164.930 Ho Holmium [Xe]4f116s2
68 167.26 Er Erbium [Xe]4f126s2
69 168.934 Tm Thulium [Xe]4f136s2
70 173.04 Yb Ytterbium [Xe]4f146s2
71 174.967 Lu Lutetium [Xe]4f145d16s2
Actinide Series
89 227.028 Ac Actinium [Rn]6d17s2
90 232.038 Th Thorium [Rn]6d27s2
91 231.036 Pa Protactinium [Rn]5f26d17s2
92 238.029 U Uranium [Rn]5f36d17s2
93 237.048 Np Neptunium [Rn]5f46d17s2
94 244.064 Pu Plutonium [Rn]5f67s2
95 243.061 Am Americium [Rn]5f77s2
96 247.070 Cm Curium [Rn]5f76d17s2
97 247.070 Bk Berkelium [Rn]5f97s2
98 251.080 Cf Californium [Rn]5f107s2
99 [254] Es Einsteinium [Rn]5f117s2
100 257.095 Fm Fermium [Rn]5f127s2
101 258.1 Md Mendelevium [Rn]5f137s2
102 259.101 No Nobelium [Rn]5f147s2
103 [262] Lr Lawrencium [Rn]5f146d17s2
Alkali Metal
Alkaline Earth
Transition Metal
Basic Metal
Semimetal
Nonmetal
Halogen
Noble Gas
Lanthanide
Actinide
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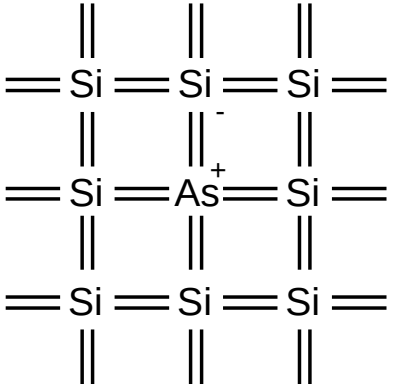
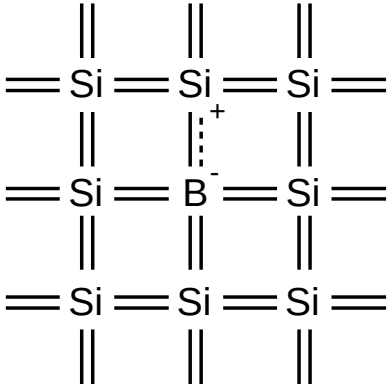
Dopants

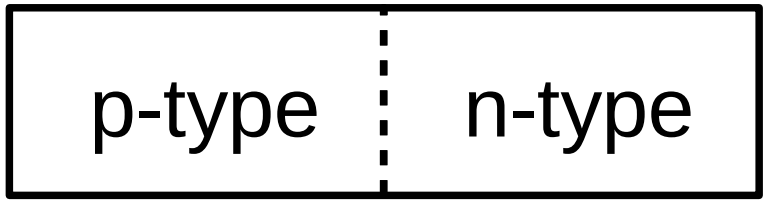
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



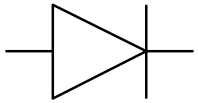


p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

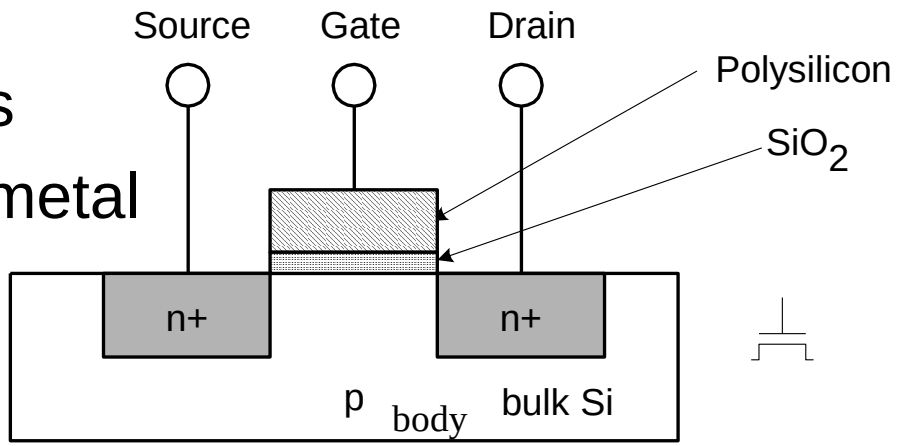


anode cathode



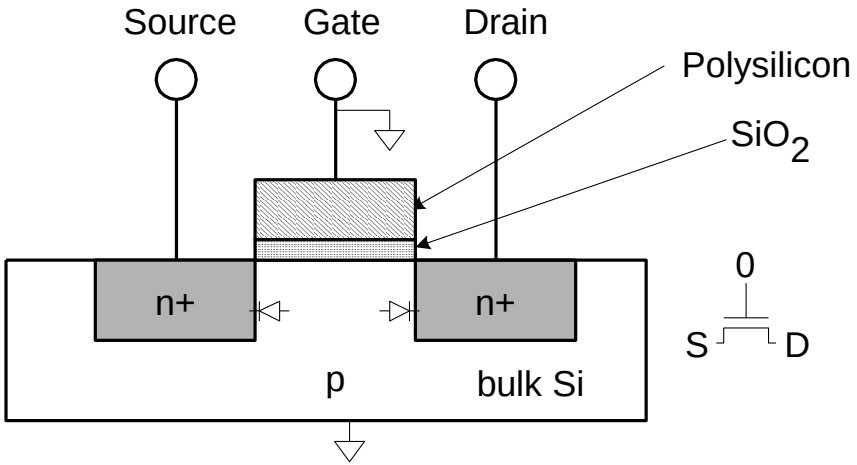
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal and different insulators



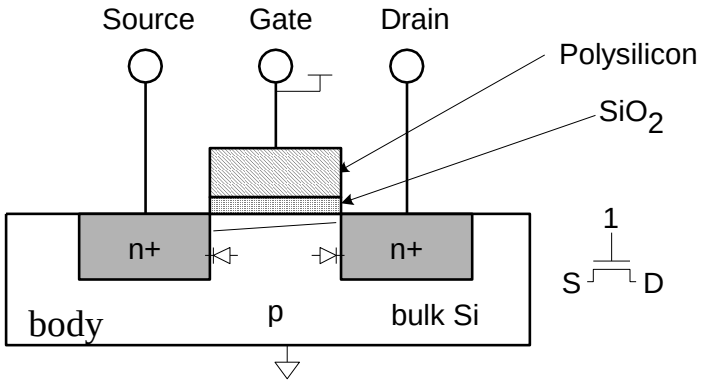
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



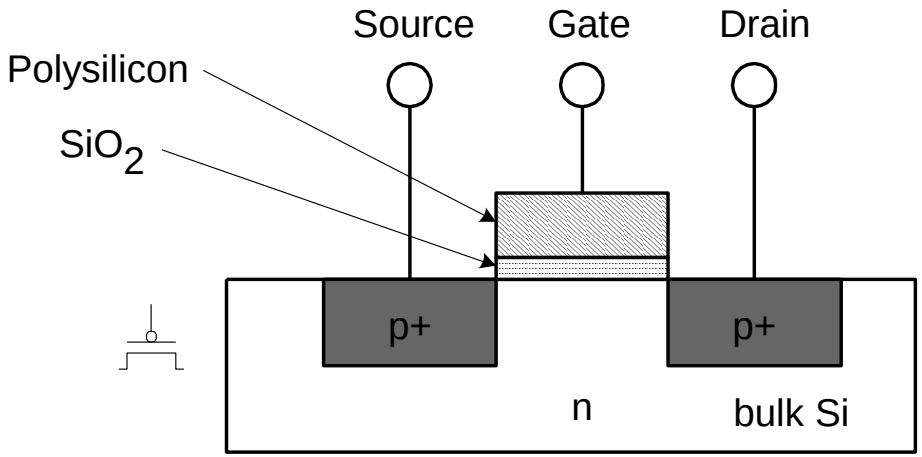
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to positive voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

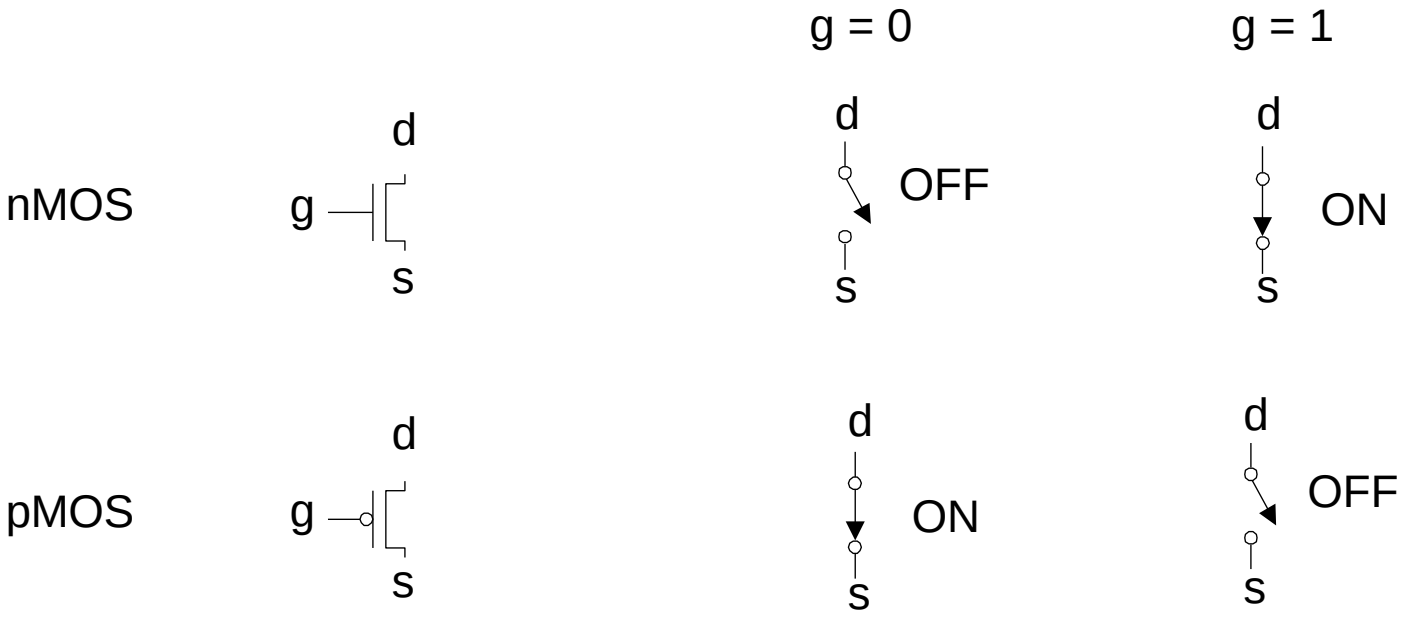


Power Supply Voltage

- GND = V_{SS} = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 5.0, 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, … 450V

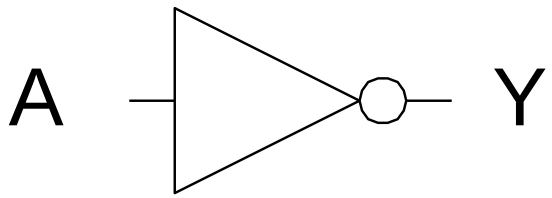
Transistors as Switches

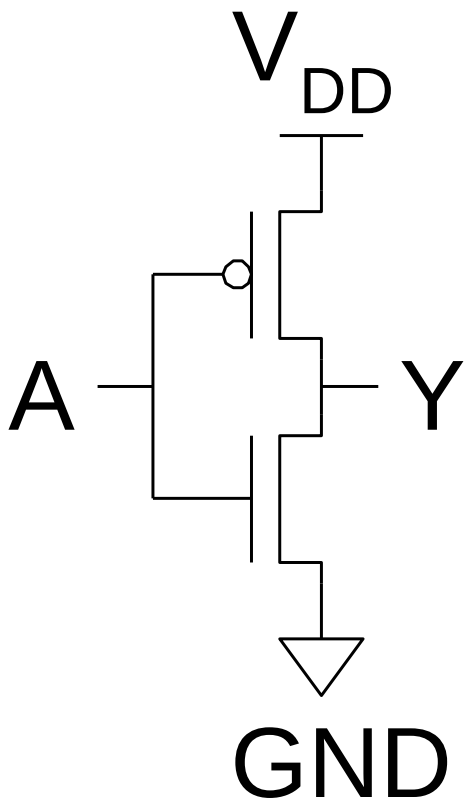
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

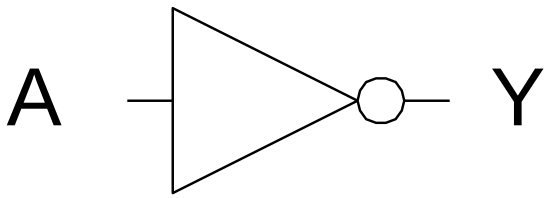
A	Y
0	
1	

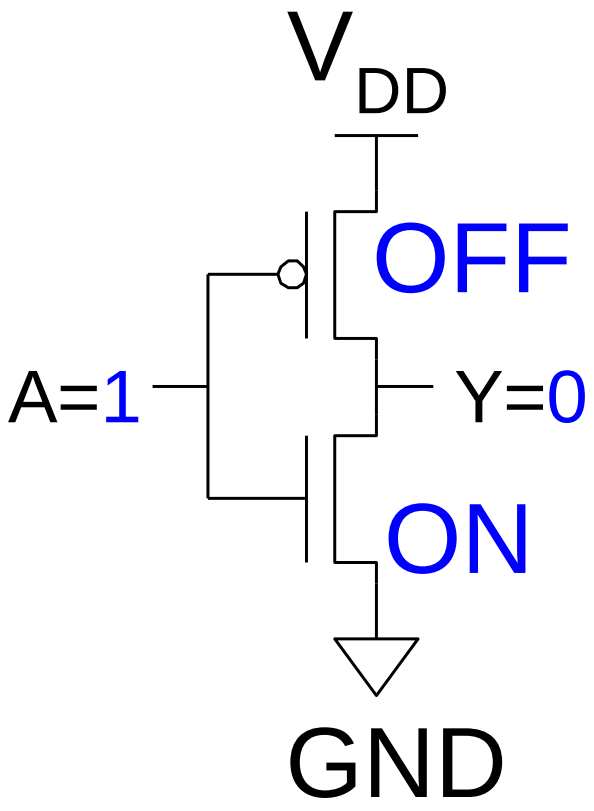




CMOS Inverter

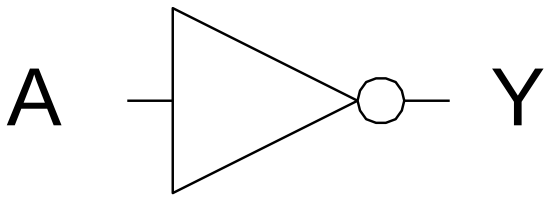
A	Y
0	
1	**0**

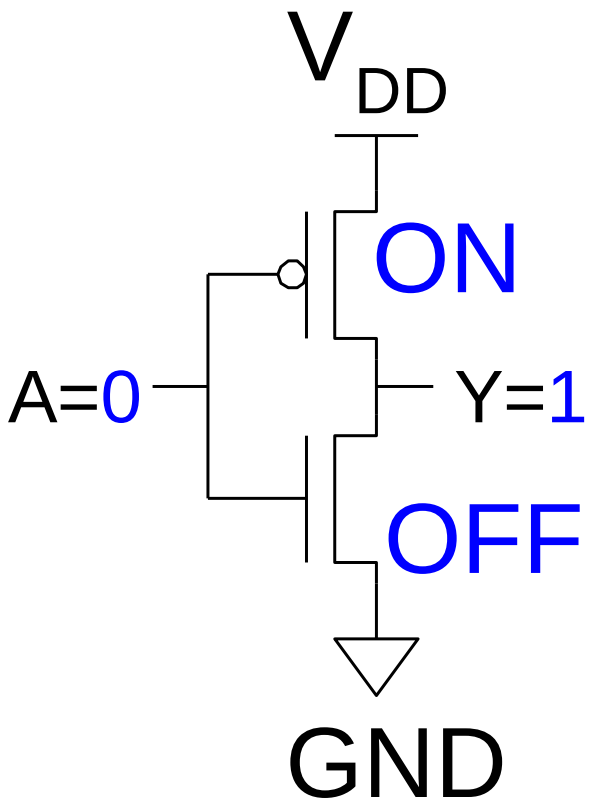




CMOS Inverter

A	Y
0	**1**
1	0



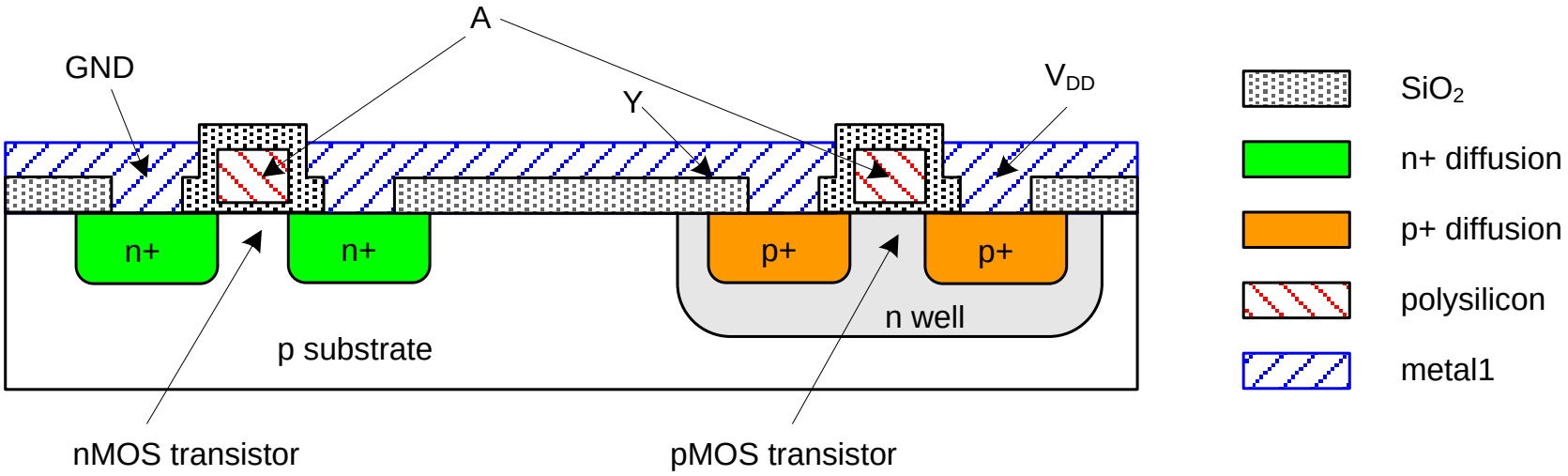


CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

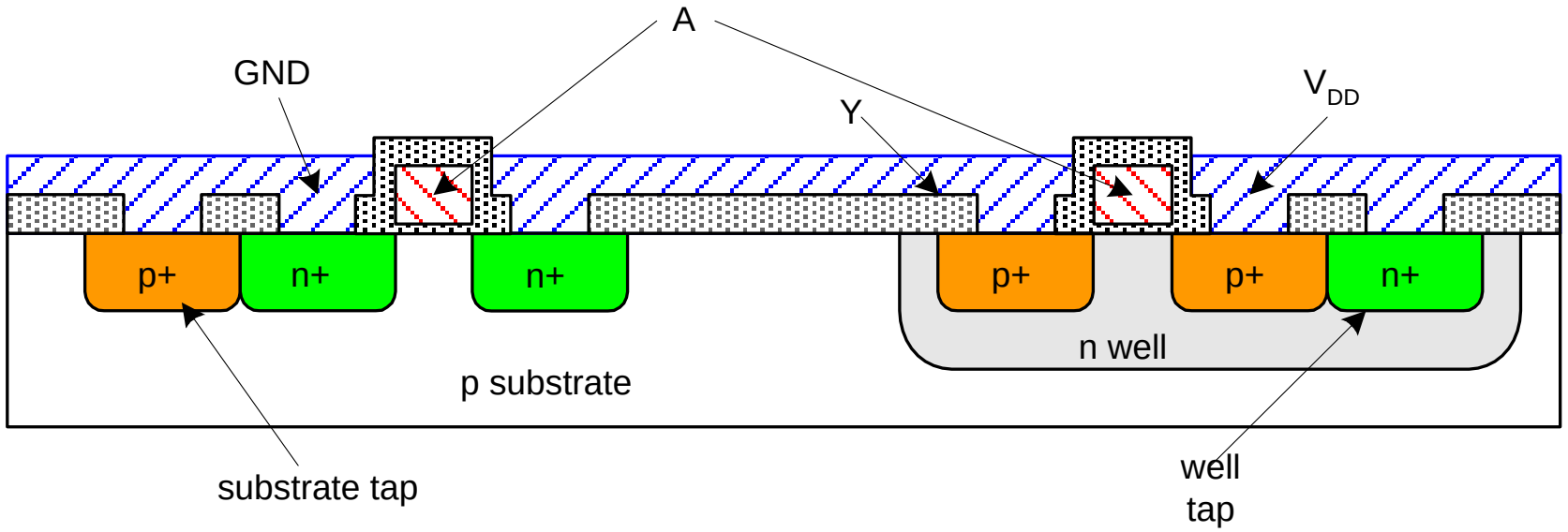
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



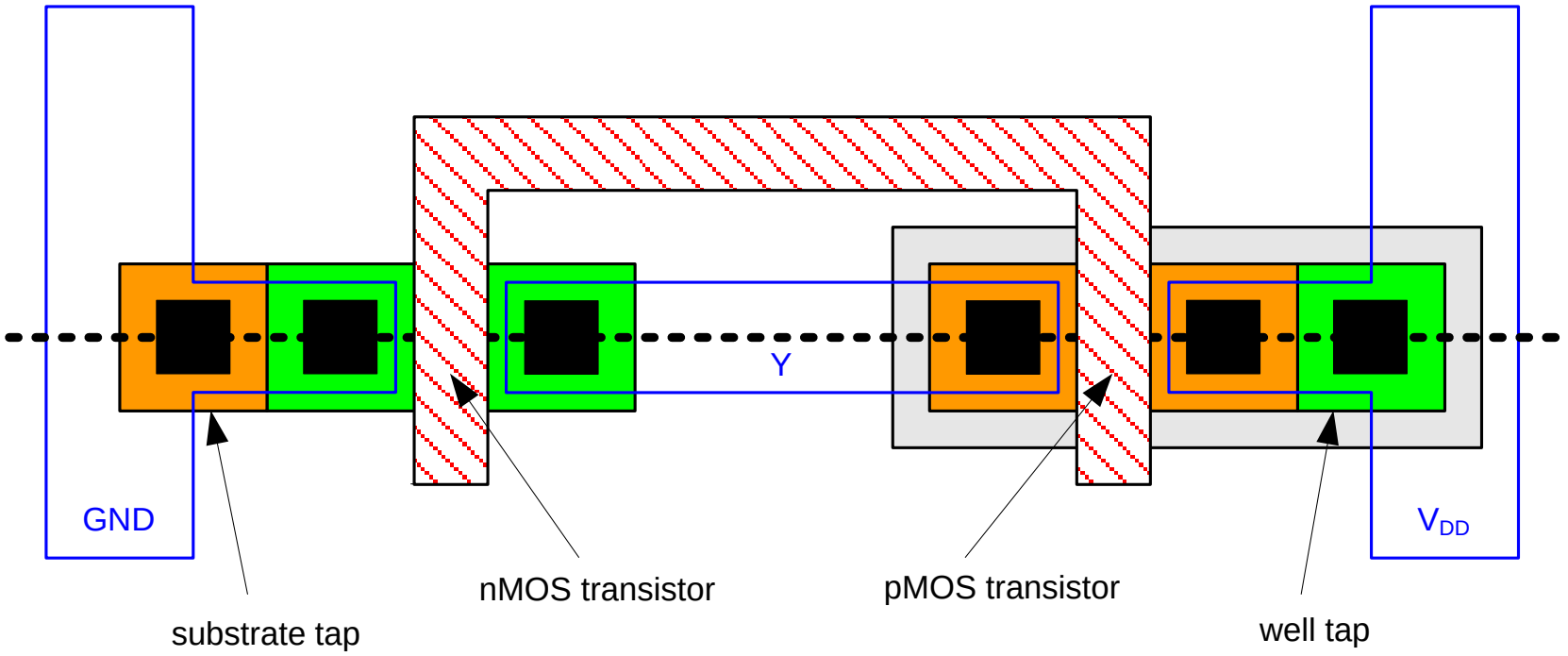
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

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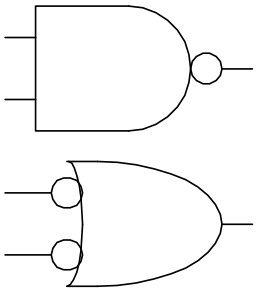
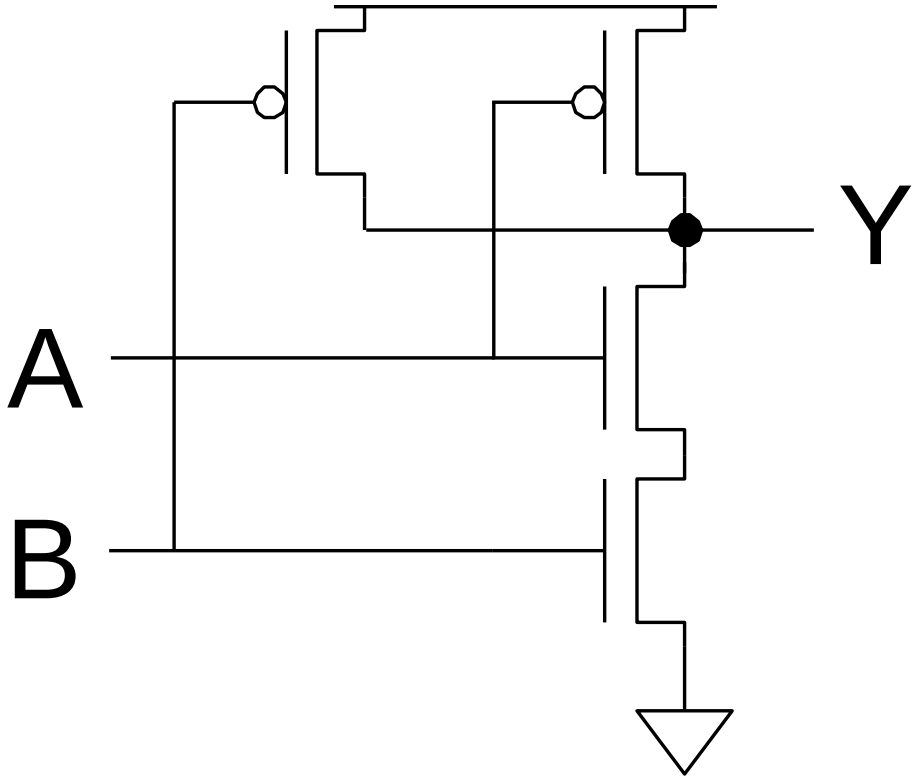
CMOS NAND Gate

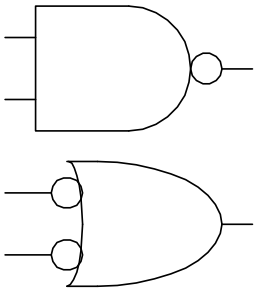
A	B	Y
0	0	
0	1	
1	0	
1	1	

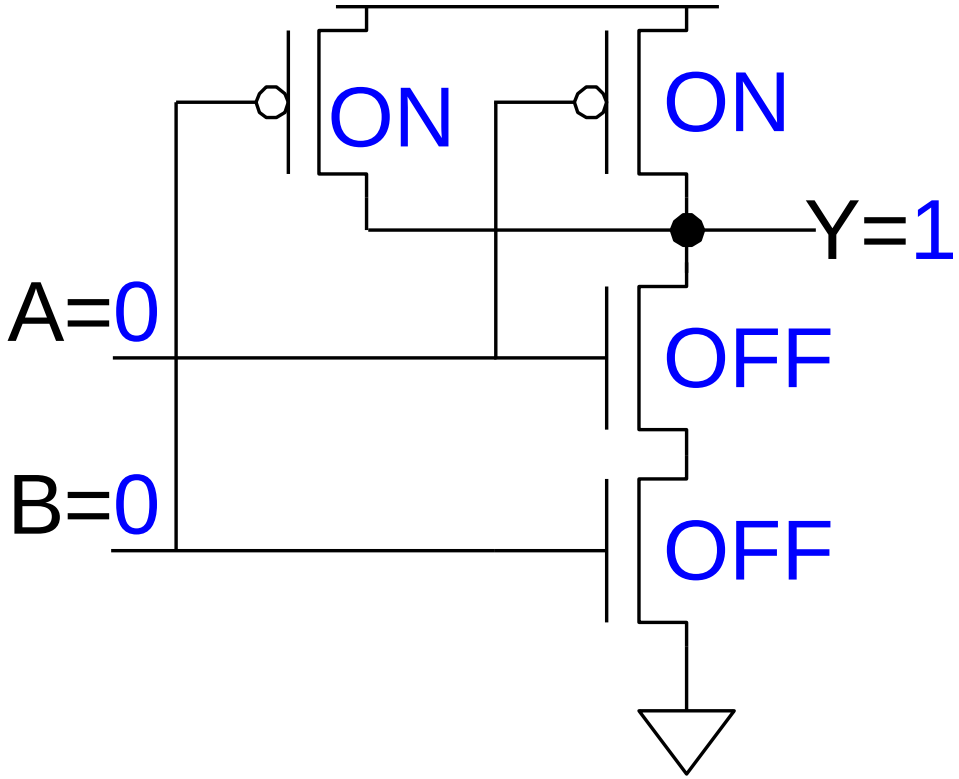




CMOS NAND Gate

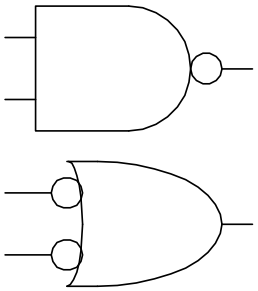
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

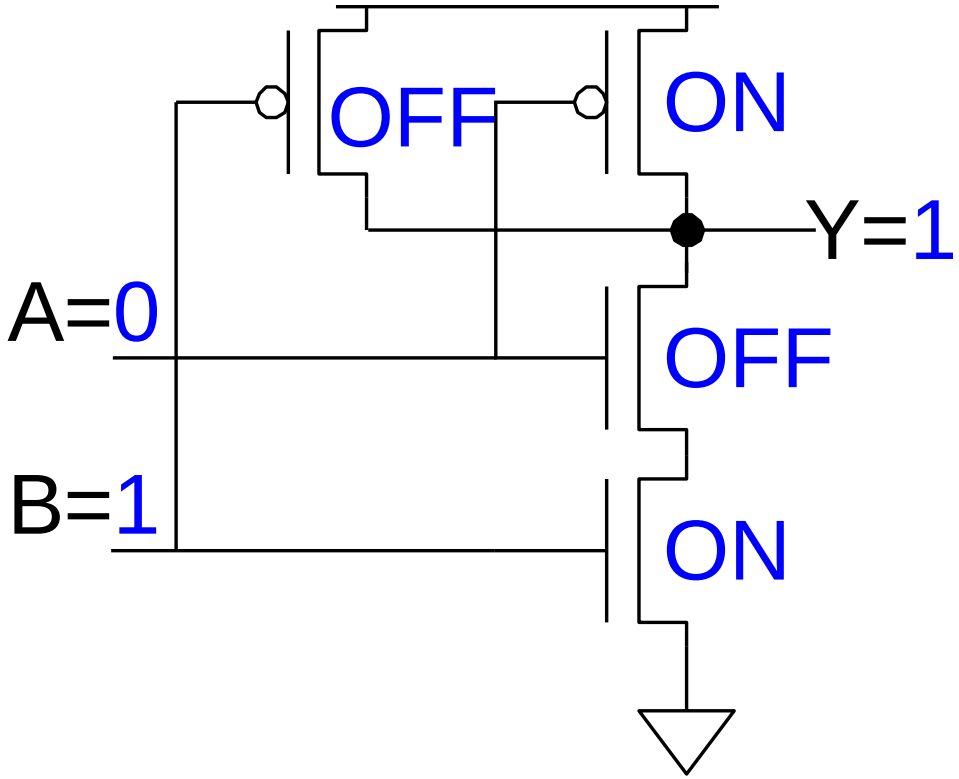




CMOS NAND Gate

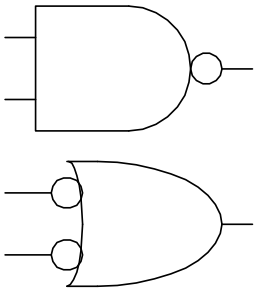
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

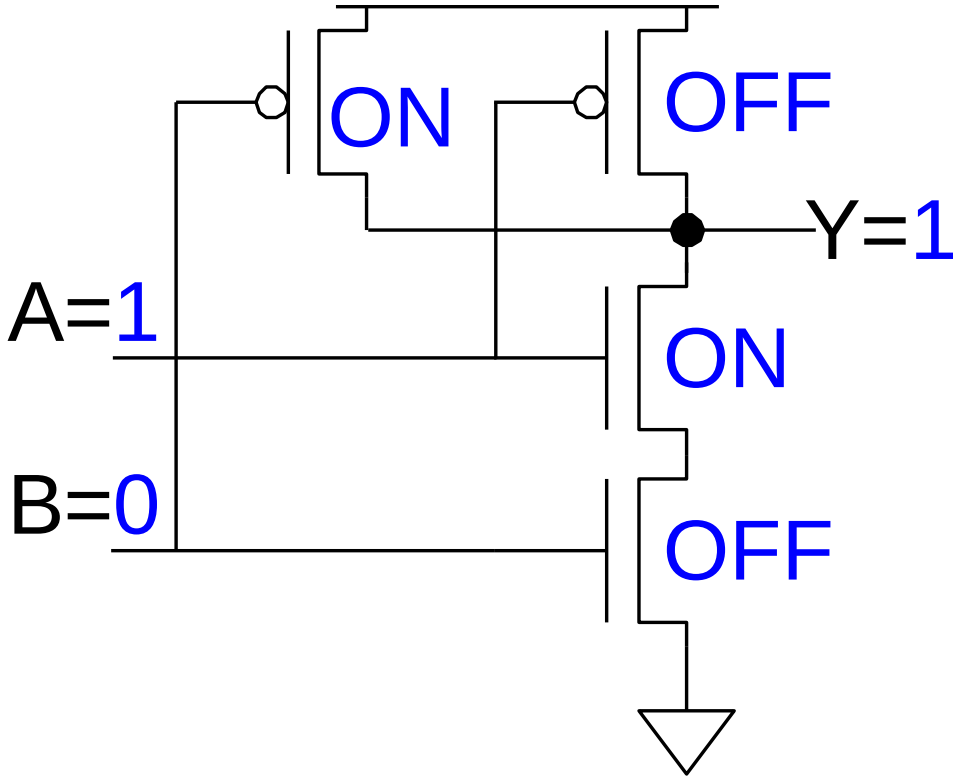




CMOS NAND Gate

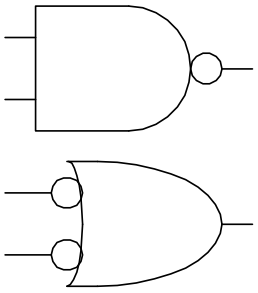
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

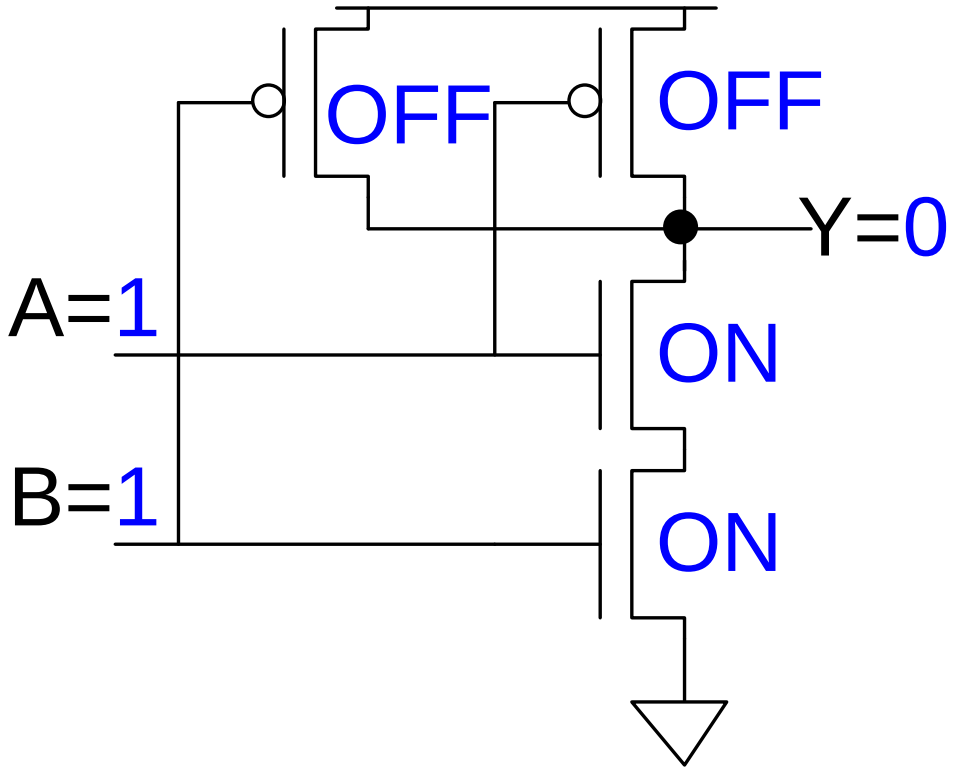




CMOS NAND Gate

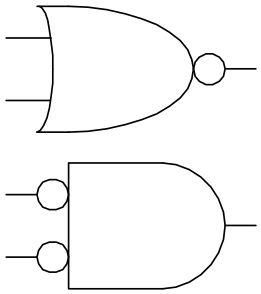
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

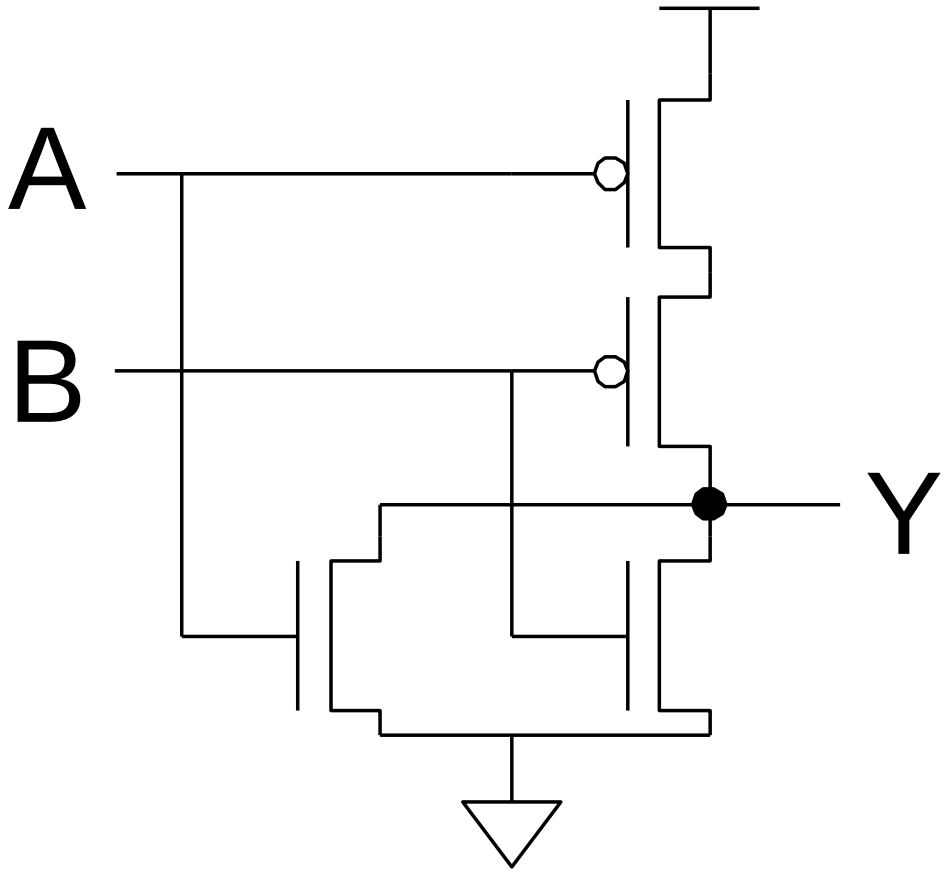




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





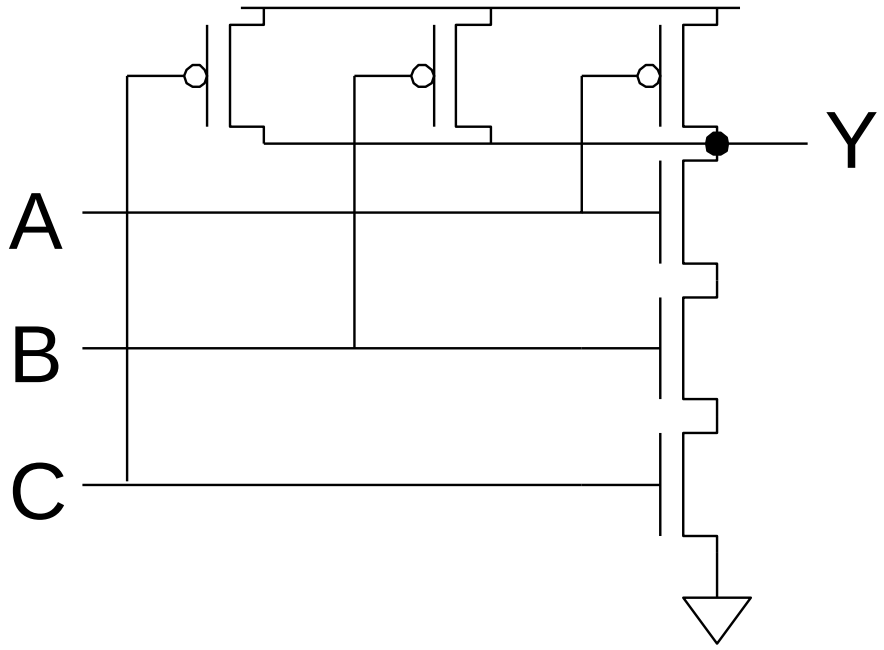
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

- ?

3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



CMOS Realization of Logic Gates

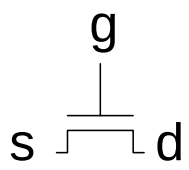
- NOT
- 2-NAND, 3-NAND
- NOR

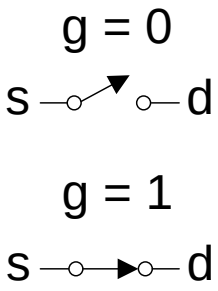
- OR
- 2-AND, 3-AND

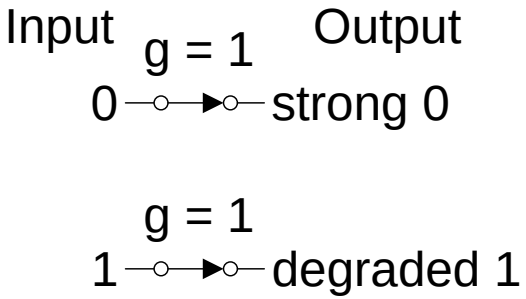
- Schematic
- Truth table with explanation

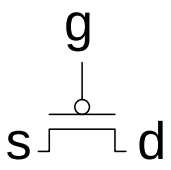
Pass Transistors

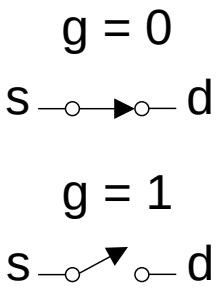
- Transistors can be used as switches

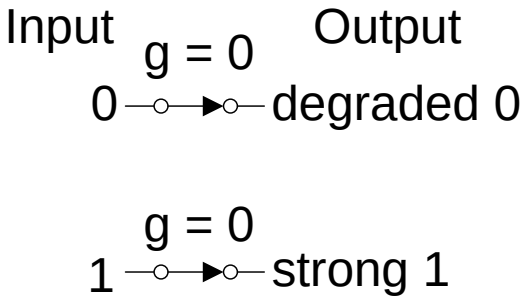






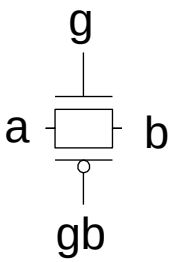


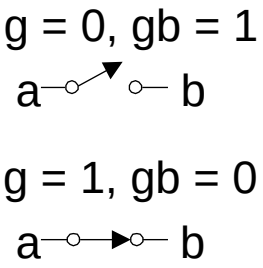


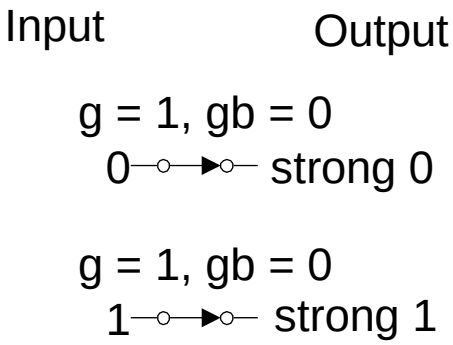


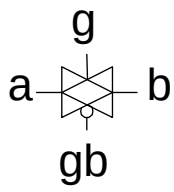
Transmission Gates

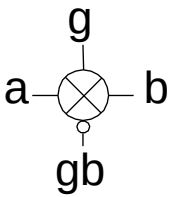
- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

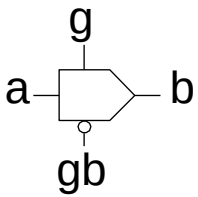








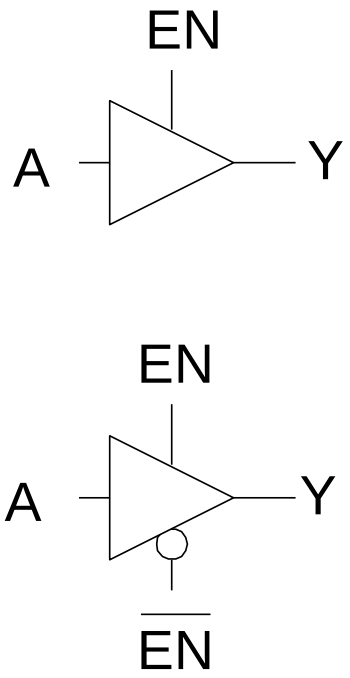




Tristates

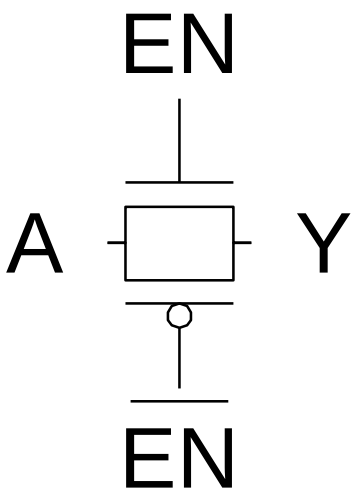
- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



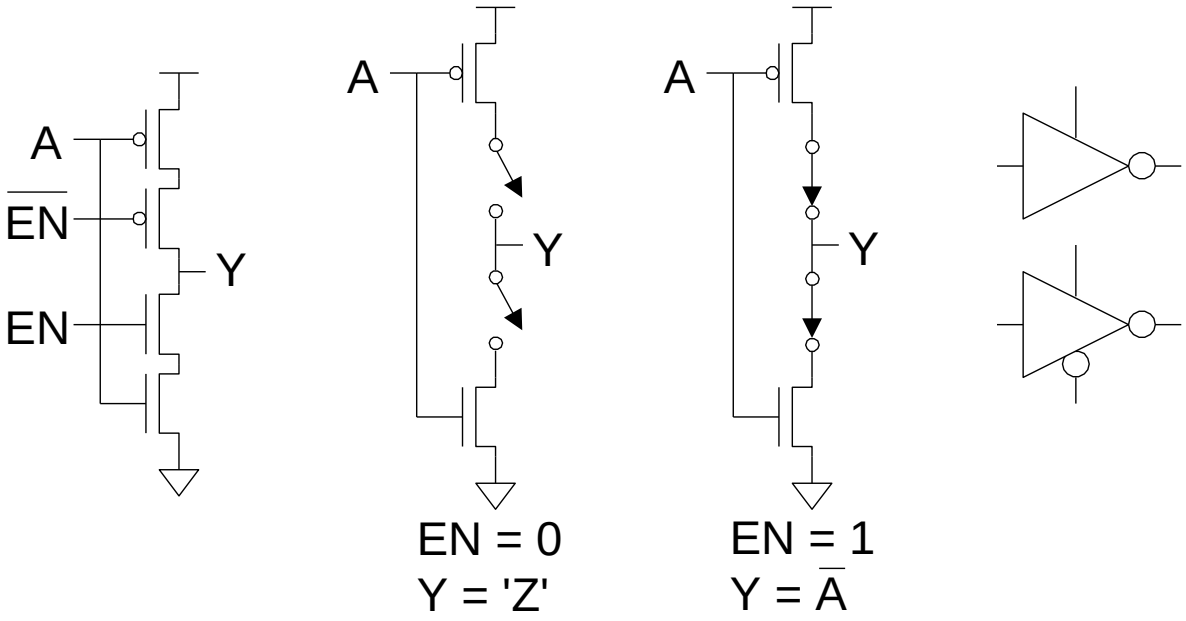
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y



Tristate Inverter

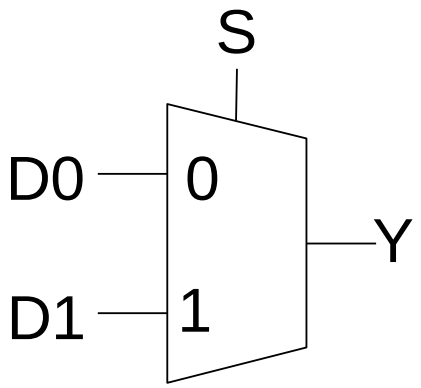
- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output



Multiplexers

- 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	
0	X	1	
1	0	X	
1	1	X	

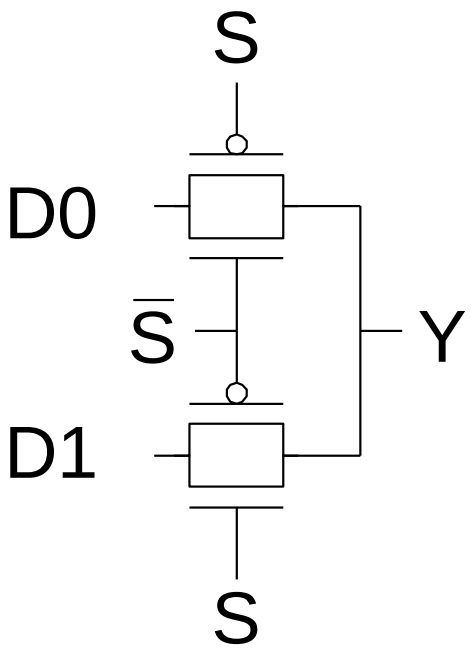


Gate-Level Mux Design

- $Y = SD_1 + \overline{S}D_0$ (too many transistors)
- How many transistors are needed?

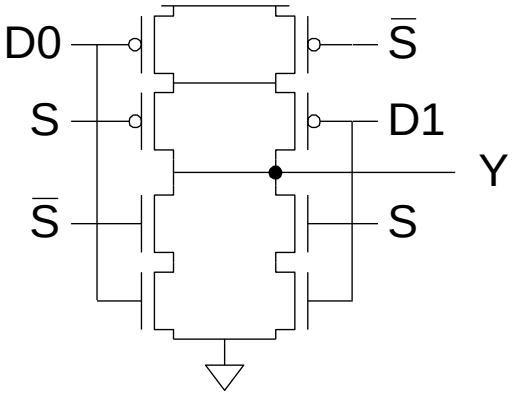
Transmission Gate Mux

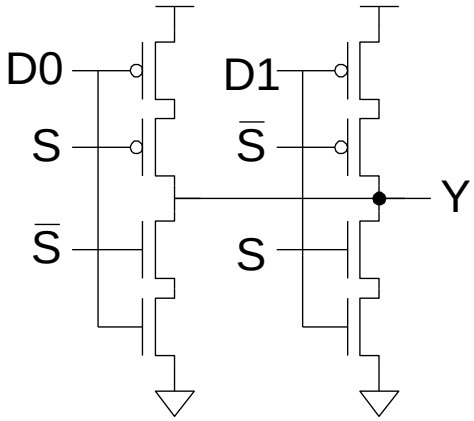
- Nonrestoring mux uses two transmission gates
  - Only 4 transistors

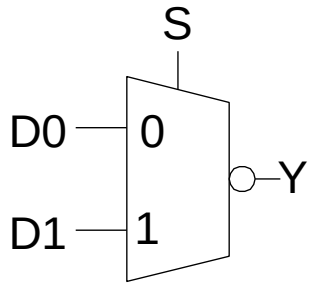


Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter

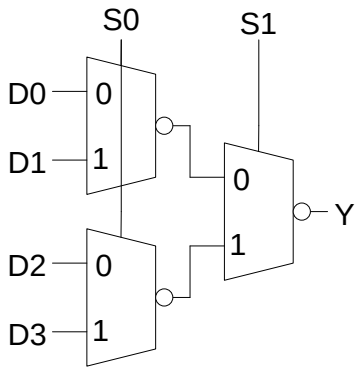


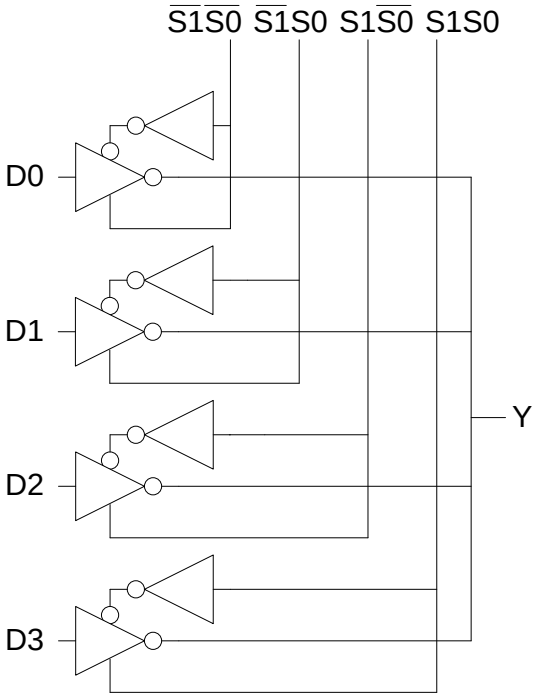




4:1 Multiplexer

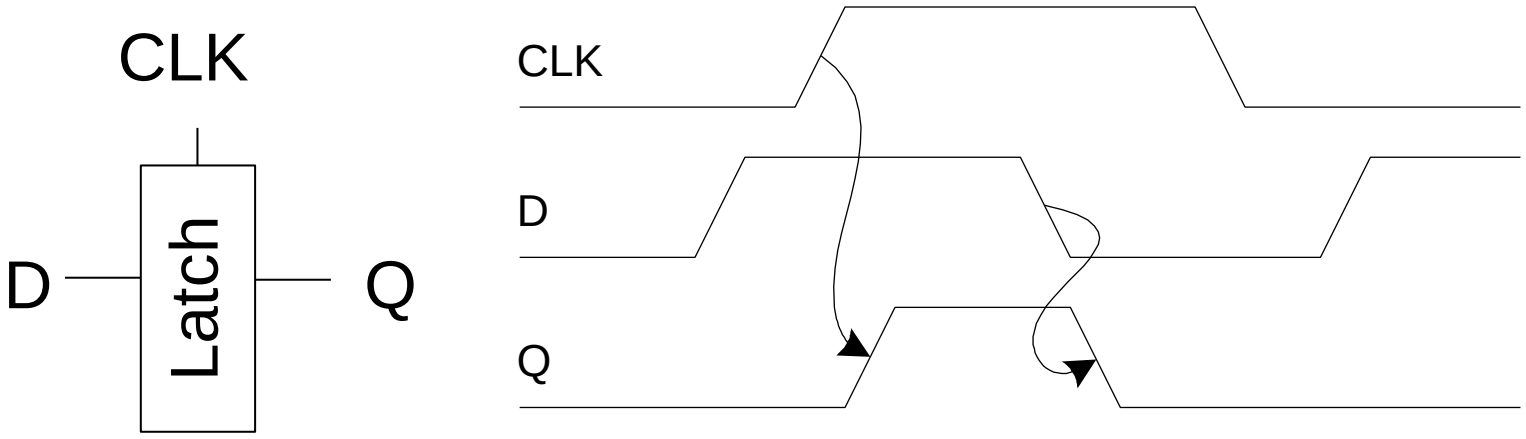
- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates





D Latch

- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*



D Latch Design

- Multiplexer chooses D or old Q