Môn học: TT Thiết kế hệ thống và Vi mạch tích hợp

GVHD: Trần Thị Quỳnh Như

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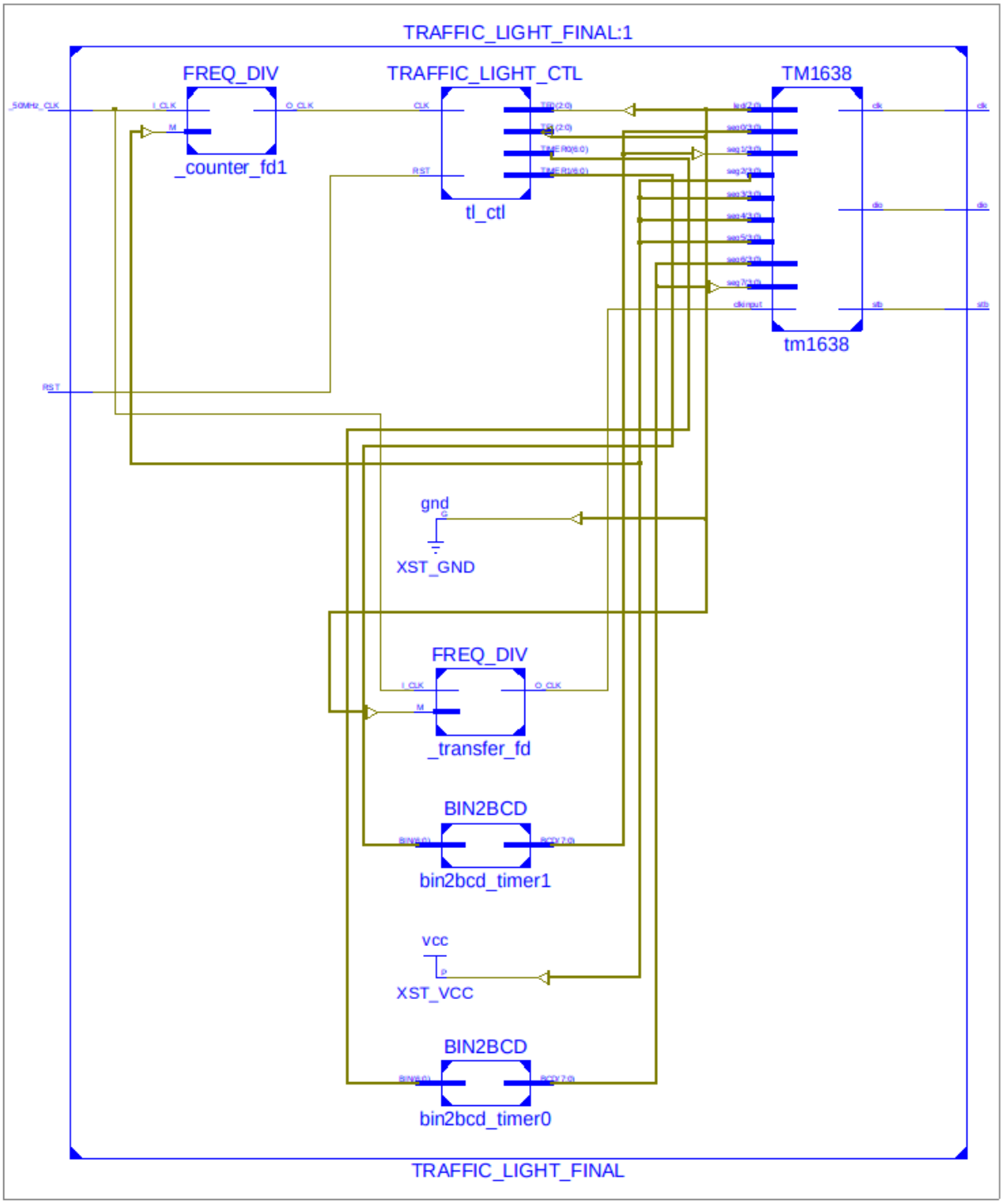
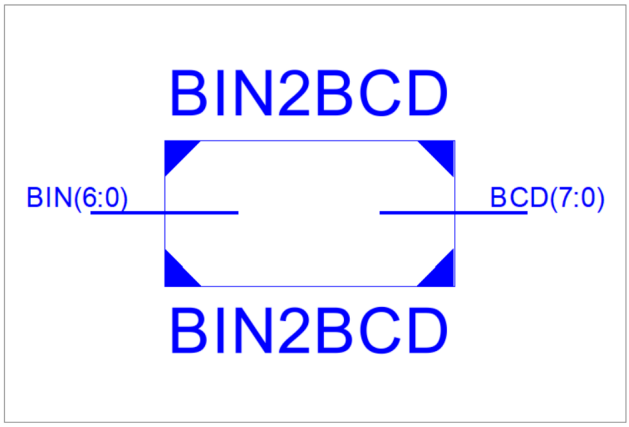
Thiết kế đồng đèn giao thông

1 - Sơ đồ khối tổng quát (Level 0/Top-module)



2 - Khối chuyển binary sang hex

Sơ đồ khối



Bảng trạng thái

INPUT	OUTPUT
BIN	HEX
0000000	1
0000001	2
0000010	3
.....	
1100001	97
1100010	98
1100011	99

Verilog HDL

BIN2BCD.v	

```
module BIN2BCD(
    input [6:0] BIN,
    output [7:0] BCD
);
    assign BCD = (BIN==0)?(8'H00):(BIN==1)?(8'H01):
    (BIN==2)?(8'H02):(BIN==3)?(8'H03):(BIN==4)?(8'H04):
    (BIN==5)?(8'H05):(BIN==6)?(8'H06):(BIN==7)?(8'H07):
    (BIN==8)?(8'H08):(BIN==9)?(8'H09):(BIN==10)?(8'H10):
```

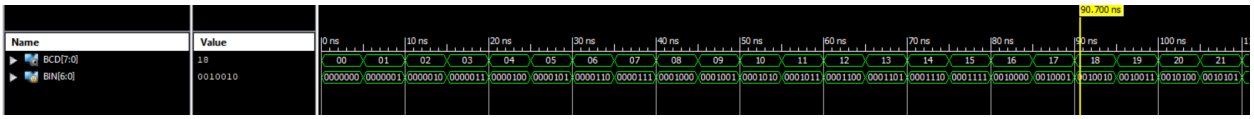
```
    (BIN==11)?(8'H11):(BIN==12)?(8'H12):(BIN==13)?(8'H13):
    (BIN==14)?(8'H14):(BIN==15)?(8'H15):(BIN==16)?(8'H16):
    (BIN==17)?(8'H17):(BIN==18)?(8'H18):(BIN==19)?(8'H19):
    (BIN==20)?(8'H20):(BIN==21)?(8'H21):(BIN==22)?(8'H22):
    (BIN==23)?(8'H23):(BIN==24)?(8'H24):(BIN==25)?(8'H25):
    (BIN==26)?(8'H26):(BIN==27)?(8'H27):(BIN==28)?(8'H28):
    (BIN==29)?(8'H29):
    (BIN==30)?(8'H30):(BIN==31)?(8'H31):(BIN==32)?(8'H32):
    (BIN==33)?(8'H33):(BIN==34)?(8'H34):(BIN==35)?(8'H35):
    (BIN==36)?(8'H36):(BIN==37)?(8'H37):(BIN==38)?(8'H38):
    (BIN==39)?(8'H39):(BIN==40)?(8'H40):(BIN==41)?(8'H41):
    (BIN==42)?(8'H42):(BIN==43)?(8'H43):(BIN==44)?(8'H44):
    (BIN==45)?(8'H45):(BIN==46)?(8'H46):(BIN==47)?(8'H47):
    (BIN==48)?(8'H48):(BIN==49)?(8'H49):(BIN==50)?(8'H50):
    (BIN==51)?(8'H51):(BIN==52)?(8'H52):(BIN==53)?(8'H53):
    (BIN==54)?(8'H54):(BIN==55)?(8'H55):(BIN==56)?(8'H56):
    (BIN==57)?(8'H57):(BIN==58)?(8'H58):(BIN==59)?(8'H59):
    (BIN==60)?(8'H60):(BIN==61)?(8'H61):(BIN==62)?(8'H62):
    (BIN==63)?(8'H63):(BIN==64)?(8'H64):(BIN==65)?(8'H65):
    (BIN==66)?(8'H66):(BIN==67)?(8'H67):(BIN==68)?(8'H68):
    (BIN==69)?(8'H69):(BIN==70)?(8'H70):(BIN==71)?(8'H71):
    (BIN==72)?(8'H72):(BIN==73)?(8'H73):(BIN==74)?(8'H74):
    (BIN==75)?(8'H75):(BIN==76)?(8'H76):(BIN==77)?(8'H77):
    (BIN==78)?(8'H78):(BIN==79)?(8'H79):(BIN==80)?(8'H80):
    (BIN==81)?(8'H81):(BIN==82)?(8'H82):(BIN==83)?(8'H83):
    (BIN==84)?(8'H84):(BIN==85)?(8'H85):(BIN==86)?(8'H86):
    (BIN==87)?(8'H87):(BIN==88)?(8'H88):(BIN==89)?(8'H89):
    (BIN==90)?(8'H90):(BIN==91)?(8'H91):(BIN==92)?(8'H92):
    (BIN==93)?(8'H93):(BIN==94)?(8'H94):(BIN==95)?(8'H95):
    (BIN==96)?(8'H96):(BIN==97)?(8'H97):(BIN==98)?(8'H98):
    (BIN==99)?(8'H99):(8'H99);

endmodule
```

Testbench

TEST_BIN2BCD.v

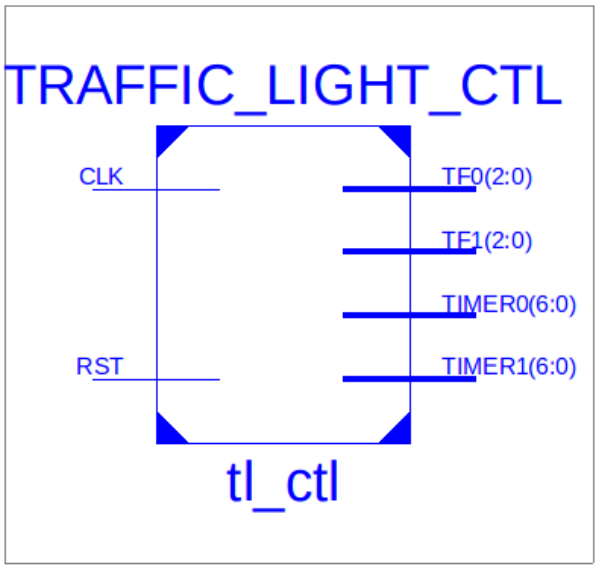
```
`timescale 1ns / 1ps
`include "BIN2BCD.v"
module tb;
   reg [6:0] BIN;
   wire [7:0] BCD;
   BIN2BCD uut (
       .BIN(BIN),
       .BCD(BCD)
```

```
    );
    initial begin
    for( BIN = 0; BIN < 100; BIN=BIN+1) begin
        #5;
    end
    end
endmodule
```



3 - Khối điều khiển đèn giao thông

Sơ đồ khối



Bảng miêu tả trạng thái

INPUT		OUTPUT			
CLK	RST	TIMER1[6:0]	TIMER0[6:0]	TF1[2:0]	TF0[2:0]
↑	0	12	9	100	001
↑	0	11	8	100	001

↑	1	12	9	100	001
↑	0	11	8	100	001
↑	0	10	7	100	001
↑	0	…	…	100	001
↑	0	3	0	100	100
↑	0	2	2	100	010
↑	0	1	1	100	010
↑	0	0	0	100	010
↑	0	9	12	001	100
↑	0	8	11	001	100
↑	0	7	10	001	100
↑	0	…	…	001	100
↑	0	0	3	010	100
↑	0	2	2	010	100
↑	0	1	1	010	100
↑	0	0	0	010	100
↑	0	12	9	100	001

Verilog HDL

TRAFFIC_LIGHT_CTL.v

```
`timescale 1ns / 1ps

module TRAFFIC_LIGHT_CTL(
    input CLK,
    input RST,
    output reg [6:0] TIMER0,//MAX: 110_0011B
    output reg [2:0] TF0,
    output reg [6:0] TIMER1,//MAX: 110_0011B
    output reg [2:0] TF1
);
```

```
wire [6:0] TIMER0_RST_VAL, TIMER1_RST_VAL;


initial begin
    TIMER0 = TIMER0_RST_VAL;
    TF0 = 3'B001;//R Y G
    TIMER1 = TIMER1_RST_VAL;
    TF1 = 3'B100;//R Y G
end

always @(posedge CLK) begin
    //Reset
    if(RST == 1) begin
        TIMER0 = TIMER0_RST_VAL;
        TF0 = 3'B001;//R Y G
        TIMER1 = TIMER1_RST_VAL;
        TF1 = 3'B100;//R Y G
    end else
    //-------------------------------------------
    begin
        if(TIMER1 > TIMER0 && TIMER0 > 0)begin
            //Count down
            //0: 0 0 1
            //1: 1 0 0
            TF0 = 3'B001;
            TF1 = 3'B100;
            TIMER0 = TIMER0 - 1;
            TIMER1 = TIMER1 - 1;
        end else
        if(TIMER1 > TIMER0 && TIMER0 == 0)begin
            //TF0 -> YELLOW; Count down
            //0: 0 1 0
            //1: 1 0 0
            TF0 = 3'B010;
            TF1 = 3'B100;
            TIMER1 = TIMER1 - 1;
            TIMER0 = TIMER1;
        end else
        if(TIMER1 == TIMER0 && TIMER0 > 0
```

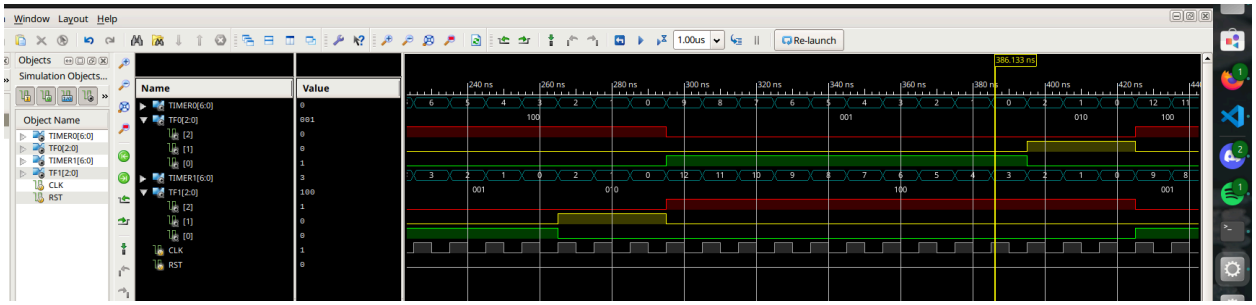
```
            && TF0 == 3'B010 && TF1 == 3'B100)begin
            //Countdown
            //0: 0 1 0
            //1: 1 0 0
            TF0 = 3'B010;
            TF1 = 3'B100;
            TIMER0 = TIMER0 - 1;
            TIMER1 = TIMER1 - 1;
        end else
        if(TIMER1 == TIMER0 && TIMER0 == 0
            && TF0 == 3'B010 && TF1 == 3'B100)begin
            //TF0 -> RED; Count down
            //TF1 -> GREEN; Count down
            //0: 1 0 0
            //1: 0 0 1
            TF0 = 3'B100;
            TF1 = 3'B001;
            TIMER0 = TIMER1_RST_VAL;
            TIMER1 = TIMER0_RST_VAL;
        end else
        //-----------------------------------------
        if(TIMER1 < TIMER0 && TIMER1 > 0)begin
            //Count down
            //0: 1 0 0
            //1: 0 0 1
            TF0 = 3'B100;
            TF1 = 3'B001;
            TIMER0 = TIMER0 - 6'D1;
            TIMER1 = TIMER1 - 6'D1;
        end else
        if(TIMER1 < TIMER0 && TIMER1 == 0)begin
            //TF1 -> YELLOW; Count down
            //0: 1 0 0
            //1: 0 1 0
            TF0 = 3'B100;
            TF1 = 3'B010;
            TIMER0 = TIMER0 - 1;
            TIMER1 = TIMER0;
        end else
```

```
            if(TIMER1 == TIMER0 && TIMER1 > 0
               && TF0 == 3'B100 && TF1 == 3'B010)begin
                //Count down
                //0: 1 0 0
                //1: 0 1 0
                TF0 = 3'B100;
                TF1 = 3'B010;
                TIMER0 = TIMER0 - 6'D1;
                TIMER1 = TIMER1 - 6'D1;
            end else
            if(TIMER1 == TIMER0 && TIMER1 == 0
               && TF0 == 3'B100 && TF1 == 3'B010)begin
                //TF0 -> GREEN; Count down
                //TF1 -> RED; Count down
                //0: 0 0 1
                //1: 1 0 0
                TF0 = 3'B001;
                TF1 = 3'B100;
                TIMER0 = TIMER0_RST_VAL;
                TIMER1 = TIMER1_RST_VAL;
            end else
            begin
                // :v
                TIMER0 = TIMER0_RST_VAL;
                TIMER1 = TIMER1_RST_VAL;
            end
        end
    end

    assign TIMER0_RST_VAL = 9;
    assign TIMER1_RST_VAL = 12;

endmodule
```

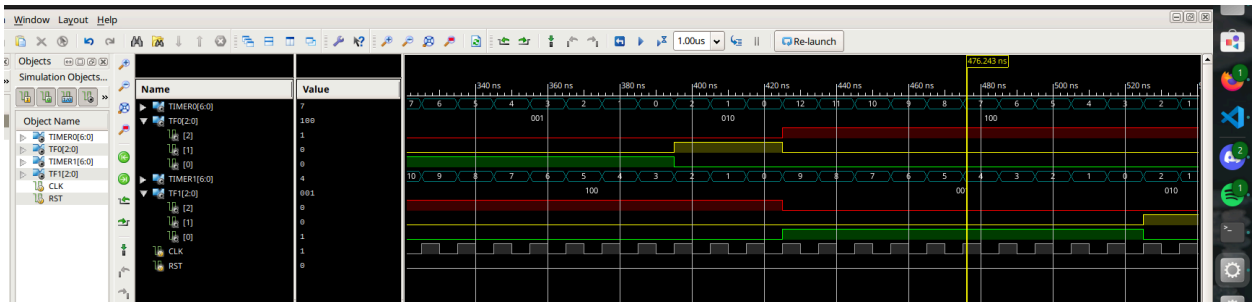
Testbench

```
`timescale 1ns / 1ps
```

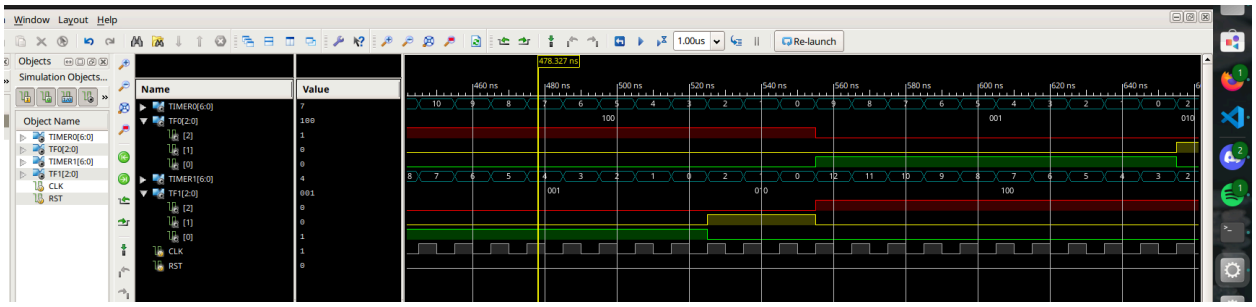
```
module TEST_TF_CTL;

    // Inputs
    reg CLK;
    reg RST;

    // Outputs
    wire [6:0] TIMER0;
    wire [2:0] TF0;
    wire [6:0] TIMER1;
    wire [2:0] TF1;

    // Instantiate the Unit Under Test (UUT)
    TRAFFIC_LIGHT_CTL uut (
        .CLK(CLK),
        .RST(RST),
        .TIMER0(TIMER0),
        .TF0(TF0),
        .TIMER1(TIMER1),
        .TF1(TF1)
    );

    initial begin
        CLK = 0;
        RST = 0;
    end
    initial begin
        forever #5 CLK = ~ CLK;
    end
    initial begin
        #30 RST = 1;
        #15 RST = 0;
    end
endmodule
```



RST tác động



TF0 chuyển từ xanh->vàng->đỏ
TF1 chuyển từ đỏ->xanh



TF0 chuyển từ đỏ->xanh
TF1 chuyển từ xanh->vàng->đỏ

4 - Khối tổng quát (Level 0/Top-module)

Verilog HDL

TRAFFIC_LIGHT_FINAL.v

```
`timescale 1ns / 1ps
`include "TRAFFIC_LIGHT_CTL.v"
`include "BIN2BCD.v"
`include "FREQ_DIV.v"
`include "TM1638.v"

module TRAFFIC_LIGHT_FINAL(
    input _50MHz_CLK,
    input RST,
   output clk,
   output stb,
   output dio
);
```

```
    wire VCC, GND;

    wire _transfer_freq_0;
    wire _counter_freq_1;

    wire [3:0] LED7SEG_0, LED7SEG_1, LED7SEG_2,
               LED7SEG_3, LED7SEG_4, LED7SEG_5,
               LED7SEG_6, LED7SEG_7;
    wire [7:0] LED;

    wire [6:0] TIMER0, TIMER1;
    wire [2:0] TF0, TF1;
    wire [7:0] BCD_TIMER0, BCD_TIMER1;

    FREQ_DIV
_transfer_fd(.I_CLK(_50MHz_CLK),.M(GND),.O_CLK(_transfer_freq_0
));
    FREQ_DIV
_counter_fd1(.I_CLK(_50MHz_CLK),.M(VCC),.O_CLK(_counter_freq_1)
);

    TRAFFIC_LIGHT_CTL tl_ctl(
        .CLK(_counter_freq_1),
        .RST(RST),
        .TIMER0(TIMER0),//MAX: 110_0011B
        .TF0(LED[2:1]),
        .TIMER1(TIMER1),//MAX: 110_0011B
        .TF1(LED[7:5])
    );

    BIN2BCD bin2bcd_timer0(
        .BIN(TIMER0),
        .BCD(BCD_TIMER0)
    );

    BIN2BCD bin2bcd_timer1(
        .BIN(TIMER1),
        .BCD(BCD_TIMER1)
    );
```

```
    TM1638  tm1638(
        .led(LED),
        .seg0(LED7SEG_0),
        .seg1(LED7SEG_1),
        .seg2(LED7SEG_2),
        .seg3(LED7SEG_3),
        .seg4(LED7SEG_4),
        .seg5(LED7SEG_5),
        .seg6(LED7SEG_6),
        .seg7(LED7SEG_7),
        .clkinput(_transfer_freq_0),
        .clk(clk),
        .stb(stb),
        .dio(dio)
    );

    assign LED[4] = 0;
    assign LED[3] = 0;
    assign LED7SEG_0 = BCD_TIMER1[7:4];
    assign LED7SEG_1 = BCD_TIMER1[3:0];
    assign LED7SEG_2 = 4'H0F;
    assign LED7SEG_3 = 4'H0F;
    assign LED7SEG_4 = 4'H0F;
    assign LED7SEG_5 = 4'h0F;
    assign LED7SEG_6 = BCD_TIMER0[7:4];
    assign LED7SEG_7 = BCD_TIMER0[3:0];

    assign VCC = 1;
    assign GND = 0;

endmodule
```