# Assignment: 8 bit Simple-As-Possible (SAP) Computer Design and Simulation

(For Section B, L3/T2)

## Problem description:

Students will have to design and simulate an 8 bit computer, which will be able to perform certain instructions (given later). Submission will be in two phases. In the 1st phase, students will have to submit the block diagram of the system and a table of all the control signals for each T states. Then, in the 2nd phase, students will have to demonstrate the simulation using any standard simulation software and face a question-answer session regarding the simulation.

## General Specifications:

1. Common bus architecture
2. 8 bit registers
3. 64 kbytes of memory
4. 8 bit Op-code
5. Hexadecimal input and output port
6. 4 bit Flag register – Zero, Sign, Carry, Overflow
7. Uses only 74XXX ICs (Except for timer/ Counter, RAM/ ROM)
8. Single stepping is possible
9. Program must be loaded from ROM at the startup

## Individual Specifications:

| 0906XX0 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 00 | ADD A, B |
| 01 | IN A |
| A2 | CALL [ADDRESS] |
| 03 | ROL A |
| 04 | CMP A, B |
| B5 | HLT |
| 06 | PUSH A |
| 07 | SHL A |
| B8 | POP B |
| 09 | OUT B |
| 0A | INC B |
| CC | RET |
| 0D | AND A, BYTE |
| 0E | XCHG A, [ADDRESS] |
| DF | JZ [ADDRESS] |
| 10 | MOV B, BYTE |

| 0906XX1 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 10 | SUB B, BYTE |
| 01 | IN B |
| 02 | RET |
| 03 | SHR A |
| 04 | TEST A, B |
| B5 | HLT |
| 06 | PUSHF |
| 07 | ROR A |
| 08 | POPF |
| C9 | OUT B |
| 0A | DEC A |
| 0C | CALL [ADDRESS] |
| 0D | XOR B, [ADDRESS] |
| DE | XCHG B, [ADDRESS] |
| 0F | JGE [ADDRESS] |
| F0 | MOV [ADDRESS], B |

| 0906XX2 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 00 | JL [ADDRESS] |
| 01 | ADD B, BYTE |
| 02 | MOV A, [ADDRESS] |
| 03 | SHR A |
| 44 | CMP A, B |
| 05 | POP B |
| 06 | PUSH A |
| 67 | ROR A |
| 08 | CALL [ADDRESS] |
| 89 | RET |
| 0A | HLT |
| 0C | OUT B |
| AD | OR A, BYTE |
| 0E | IN B |
| 0F | XCHG A, B |
| F0 | DEC A |

| 0906XX3 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 00 | HLT |
| A1 | PUSH B |
| 02 | POP A |
| 03 | IN A |
| 04 | OUT B |
| 05 | ROL B |
| B6 | CALL [ADDRESS] |
| 07 | RET |
| 08 | SUB A,B |
| 09 | CMP A, [ADDRESS] |
| CA | JNZ [ADDRESS] |
| 0C | MOV [ADDRESS], B |
| 0D | NOT B |
| 0E | DEC B |
| DF | SHR A |
| 10 | XCHG B, [ADDRESS] |

| 0906XX4 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 30 | SHR A |
| 01 | XCHG [ADDRESS], B |
| 62 | INC A |
| 03 | OR [ADDRESS], B |
| 04 | MOV B, [ADDRESS] |
| 85 | JNA [ADDRESS] |
| 06 | TEST A, B |
| 07 | SUB B, [ADDRESS] |
| A8 | RET |
| 09 | CALL [ADDRESS] |
| 0A | ROR B |
| BC | OUT B |
| 0D | IN B |
| FE | POPF |
| 0F | PUSHF |
| 10 | MOV [ADDRESS], B |

| 0906XX5 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| B0 | SUB B, BYTE |
| 21 | OUT B |
| 02 | RET |
| 03 | SHL A |
| 04 | AND A, B |
| C5 | HLT |
| 06 | PUSHF |
| 07 | ROR B |
| D8 | POPF |
| 09 | OUT B |
| 0A | DEC B |
| EC | CALL [ADDRESS] |
| 0D | TEST B, [ADDRESS] |
| FE | XCHG A, [ADDRESS] |
| 0F | JNZ [ADDRESS] |
| 10 | MOV A, B |

| 0906XX6 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| A0 | CALL [ADDRESS] |
| A1 | ROL A |
| A2 | OUT A |
| 03 | IN A |
| 04 | PUSH B |
| 05 | POP A |
| B6 | HLT |
| 07 | RET |
| 08 | SHL B |
| C9 | XCHG A, B |
| 0A | INC B |
| CC | NOT [ADDRESS] |
| 0D | MOV A, BYTE |
| FE | CMP A, [ADDRESS] |
| 0F | JZ [ADDRESS] |
| D0 | ADD [ADDRESS], B |

| 0906XX7 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| 03 | SUB A, B |
| B1 | IN B |
| C2 | CALL [ADDRESS] |
| A3 | SHL A |
| F4 | TEST A, [ADDRESS] |
| F5 | HLT |
| 06 | PUSHF |
| A7 | ROR A |
| D8 | POPF |
| 09 | DEC B |
| EA | OUT B |
| 0C | RET |
| FD | XOR A, BYTE |
| 0E | MOV A, [ADDRESS] |
| FF | ADD B, [ADDRESS] |
| 10 | JL [ADDRESS] |

| 0906XX8 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| C0 | ADD A, B |
| D1 | TEST A, [ADDRESS] |
| E2 | XCHG B, [ADDRESS] |
| F3 | ROL B |
| A4 | SHR A |
| B5 | MOV [ADDRESS],A |
| C6 | XOR A, [ADDRESS] |
| E7 | IN [ADDRESS] |
| 08 | INC [ADDRESS] |
| 09 | OUT A |
| AA | JZ ADDRESS |
| AC | PUSH B |
| 0D | POP B |
| BE | CALL [ADDRESS] |
| DF | RET |
| F0 | HLT |

| 0906XX9 | |
|---|---|
| **Opcode (Hex)** | **Instruction** |
| A0 | CMP A, [ADDRESS] |
| 01 | HLT |
| B2 | XCHG B, A |
| 03 | IN B |
| C4 | OUT A |
| 05 | INC A |
| D6 | RCL A |
| 07 | MOV B, BYTE |
| 08 | JNZ [ADDRESS] |
| F9 | PUSH B |
| 0A | POP B |
| 0C | NOT A |
| AD | CALL [ADDRESS] |
| 0E | RET |
| DF | SHR B |
| F2 | ADD [ADDRESS], B |

## Submission Deadline:

1st phase: Friday of 1st week of Midterm (Through e-mail, **Subject: EEE 315 Assignment**)

2nd phase: 1st week after Midterm

## Mark distribution: (Total 30)

1. Block diagram and control word table: 8
2. Simulation: 12
3. Viva: 10
4. Compactness/Innovative Idea/Extra feature: 5 (Bonus)

## Special Instructions:

- For any query regarding anything about the assignment, send e-mail at sohel1081@gmail.com
- Delayed submission in any phase will result in deduction of marks
- Any act of unfair means, if found, will result in zero or even negative marks.