Computer Architecture and Programming Languages
Jacobs University Bremen
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Homework 9

Problem 9.1

Solution:

(a) This is because program counter is updated in every cycle. The Branch and Jump signals feed the multiplexers at the end of the datapath pipeline. This determines the input to the Program Counter. When these control inputs are absent, the PC is automatically incremented by its default value, which is 4. Thus, an explict write control is not needed for the PC in a single cycle data path.

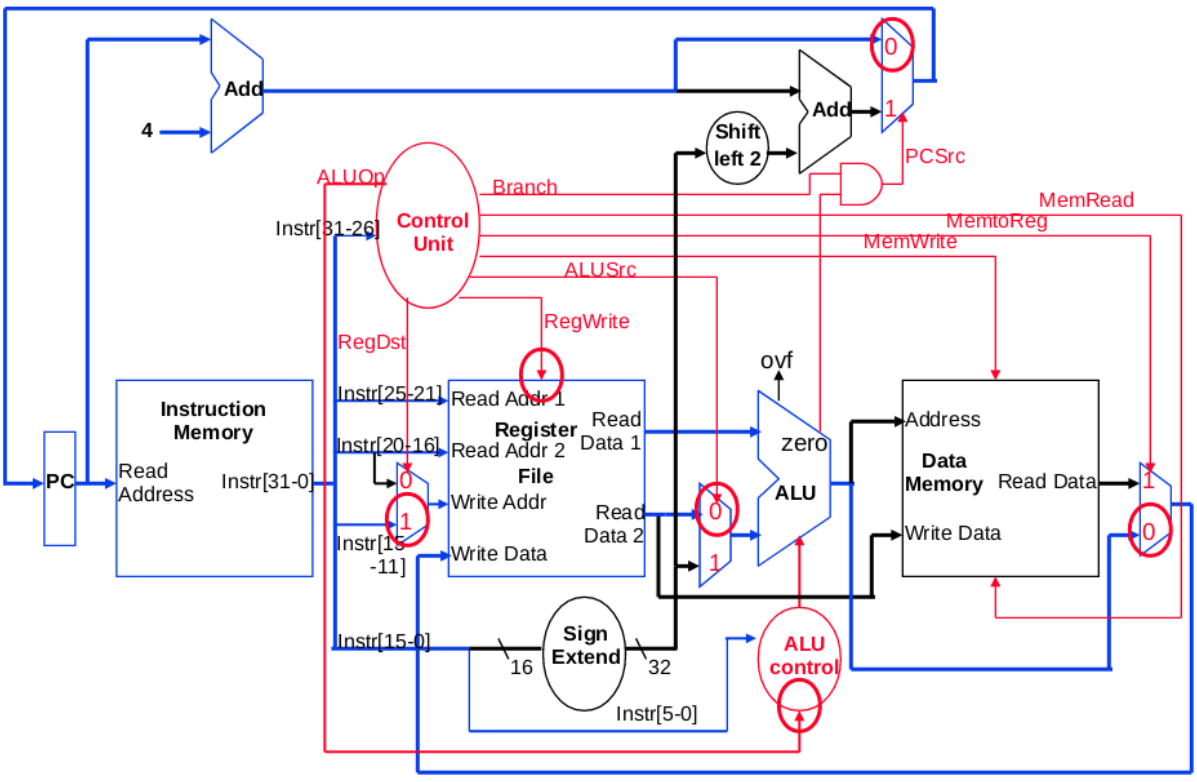
(b) In multicycle datapaths, several operations are happening in parallel. Thus, an explicit control is required in order to determine which path is to be picked in determining the address of the next instruction.

Source: https://stackoverflow.com/questions/40835418/why-an-explicit-single-cycle-datapath-is-not-needed

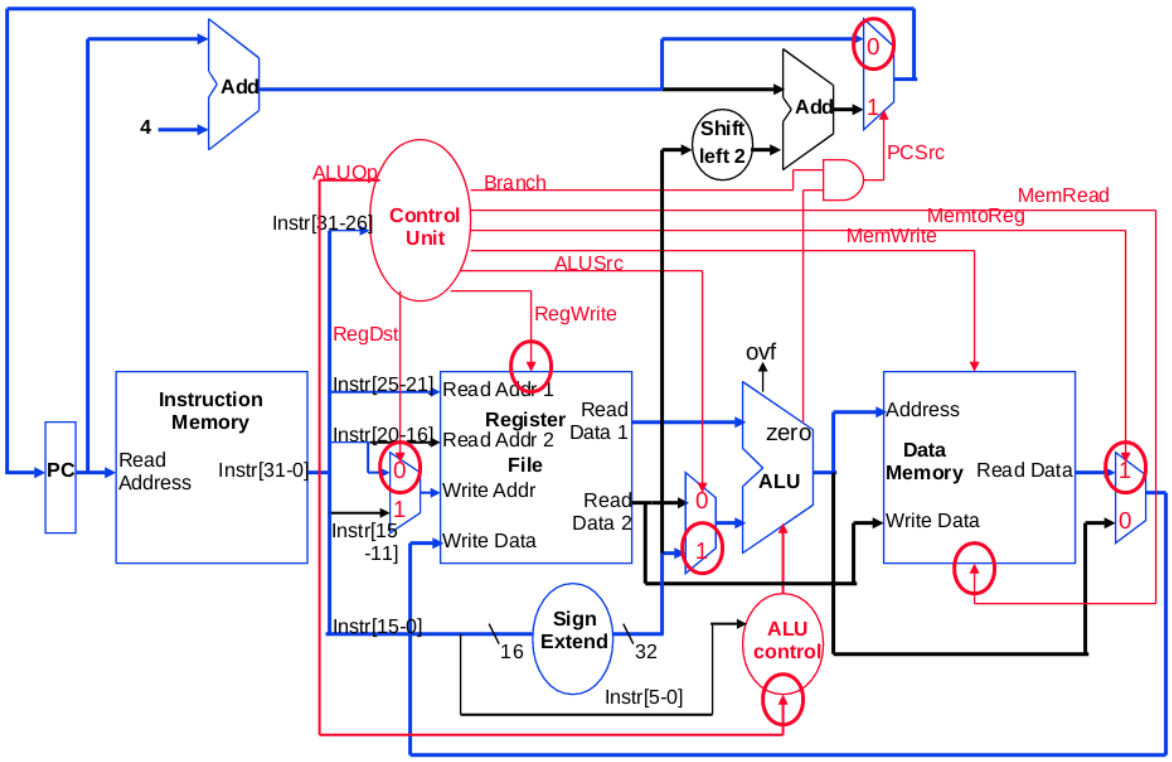
Problem 9.2

Solution:

(a) add instruction:



lw instruction:



Unlike the add instruction, sign extended is also used here.

Note: As CS students, we must be smart and find optimal solutions in terms of time, which is why solutions from slides must be acceptable :D

Instruction	RegDst	ALUSrc	MemtoReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp
add	1	0	0	1	0	0	1	0
lw	0	1	1	1	1	0	0	0

Source: Course Slides

(b) ALU adds its inputs when the control input is 0010. In this case, only two I type instructions are possible. Load Word (lw) or Save Word (sw). The ALUOp is 00 in both scenarios. Here, the base address of a register and the offset are added.

Additionally, this also happens when the R type add instruction is executed. Here, ALUOp is 10 while the Funct field is 100000. Here, sum of two values is calculated.

Moreover, addition also occurs when the I type addi instruction is run. ALUOp is 11 in this case. Here again, sum of 2 values is calculated where one of the values is a given constant.(info given on the internet but not on the slides so not sure if this is to be included or not).