TIMER DESIGN

1. Overview

This 8-bit timer module operates on the basis of an 8-bit counter. The 8-bit timer module can be used to count external events and be used as a multifunction timer in a variety of applications, such as generation of counter reset, and interrupt requests.

1.1 Feature

- Selection of four clock sources.
- Read/Write control using APB protocol. PSLVERR will activate high when the transmission fails.
- Two counting operations, including normal operation and load data from TDR register operation.
- Setting the Timer counter (TCNT) through the TCR register.
- Showing Overflow and Underflow status on the TSR register, and the register status can be reset using APB transfer.

1.2 Block diagram

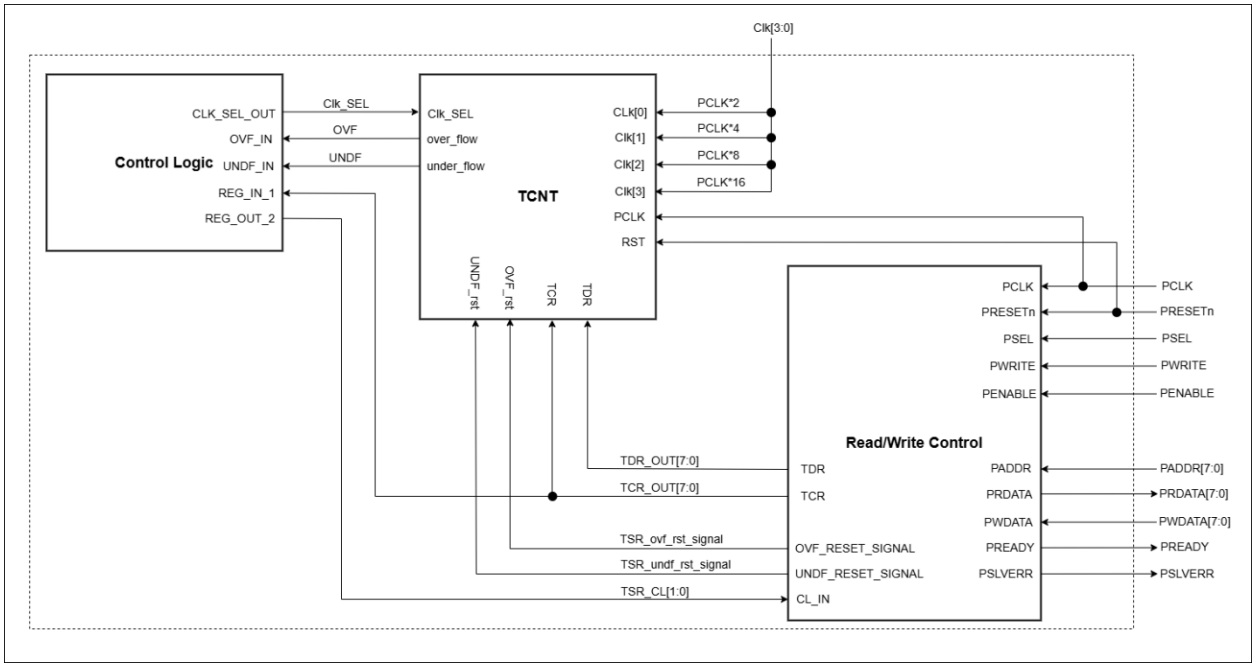

Figure 1-1 Block diagram of 8-bit Timer

1.3 Input/Output pin (LSI pin – CHIP PIN/PORT)

Pin name	Bit width	I/O	Function
Clk[3:0]	4-bit	Input	The clock source for the counter timer. Each clock has a different frequency.
PCLK	1-bit	Input	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	1-bit	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	1-bit	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PWRITE	1-bit	Input	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PENABLE	1-bit	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PADDR[7:0]	8-bit	Input	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PWDATA[7:0]	8-bit	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PRDATA[7:0]	8-bit	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY	1-bit	Output	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	1-bit	Output	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

1.4 Register specification

The 8-bit timer module has the following registers.

- Timer Data Register (TDR).
- Timer counter Control Register (TCR).
- Timer Status Register (TSR).

1.4.1 Timer Data Register (TDR)

The APB protocol sets this register value, the TDR register contains the counting value the user wants to start within the loading data mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDR[7]	TDR[6]	TDR[5]	TDR[4]	TDR[3]	TDR[2]	TDR[1]	TDR[0]

Bit name	F/V	Description
TDR[7:0]	R/W	Data is used to update the value of the counter.

1.4.2 Timer Counter Control Register (TCR)

The APB protocol is setting this register value, each bit in the TCR register consists of a setting for the bellow attributes:

- Operations selection between loading data from TDR to TCNT or normal operation.
- Counting order selection.
- Enabling the counter.
- Select the internal clock, based on the selections *2, *4, *8, *16.

*Internal _clock = PCLK (system clock) * Selected_value.*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Load	Reserved	Up/Dw	En	Reserved	Reserved	Cks1	Cks0

Bit name	F/V	Description
Load[7]	R/W	Manual load data from TDR to TCNT when it is active High. 1: load data to TCNT 0: Normal operation
Bit 6	Reserved	Reserved
Up/Dw[5]	R/W	Control counter up or counter down 0: counter up 1: counter down
En[4]	R/W	0: disable 1: enable
Bit 3:2	Reserved	Reserved
Cks[1:0]	R/W	Select internal clocks for the circuit 00: T*2 01: T*4 10: T*8 11: T*16

1.4.3 Timer Status Register (TSR)

TSR displays status flags and controls to compare match output.

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_TMR_UDF	S_TMR_OVF

Bit name	**R/W**	**Description**
7:2	R	Reserved
S_TMR_UDF[1]	R/W*	Timer counter underflow when counter 8'h00 down to 8'hff: This bit is only set by hardware, clear by software
S_TMR_OVF[0]	R/W*	Timer counter overflow when counter 8'hFF to 8'h00: This bit is only set by hardware, clear by software

2. Read/Write control

2.1 Block diagram

The Read/Write control block is a combination of these sub-modules:

- Read Write control module: this module acts as an APB peripheral slave and performs read-and-write transactions on three registers TDR, TCR, and TSR.
- The TDR register.
- The TCR register.
- The TSR module: this module will receive input signals from APB write transaction and Control Logic block, then decide the status on the TSR register.

Figure 2-1 shows the connections between sub-modules in the Read/Write control block.

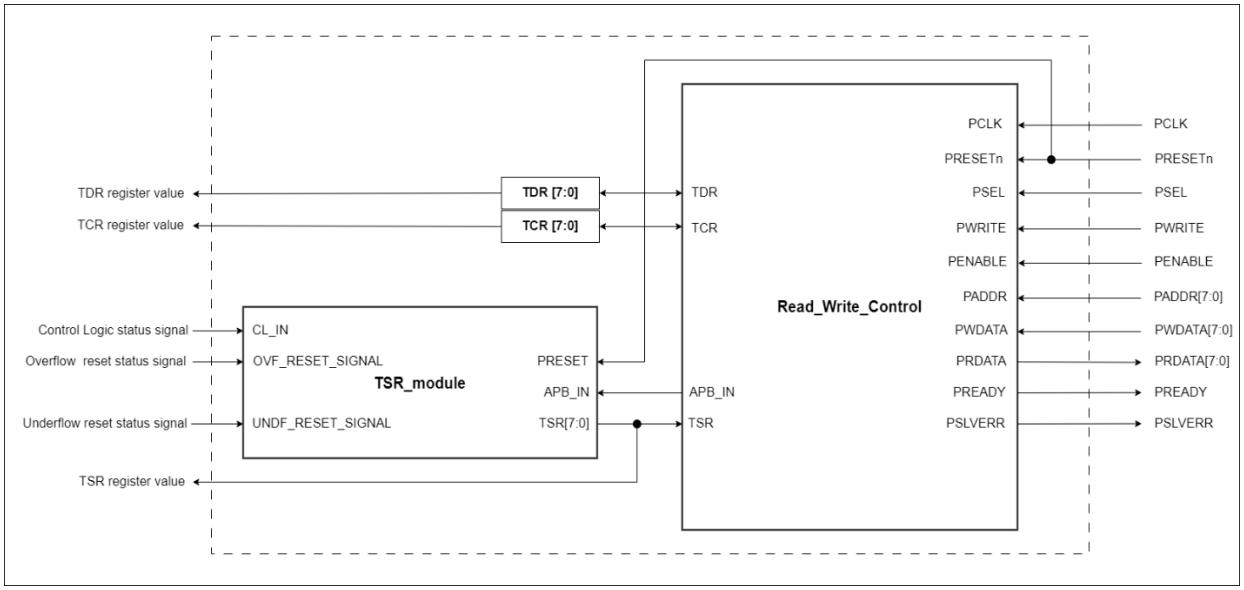

Figure 2-1 Read/Write Control block diagram

2.2 Logic diagram

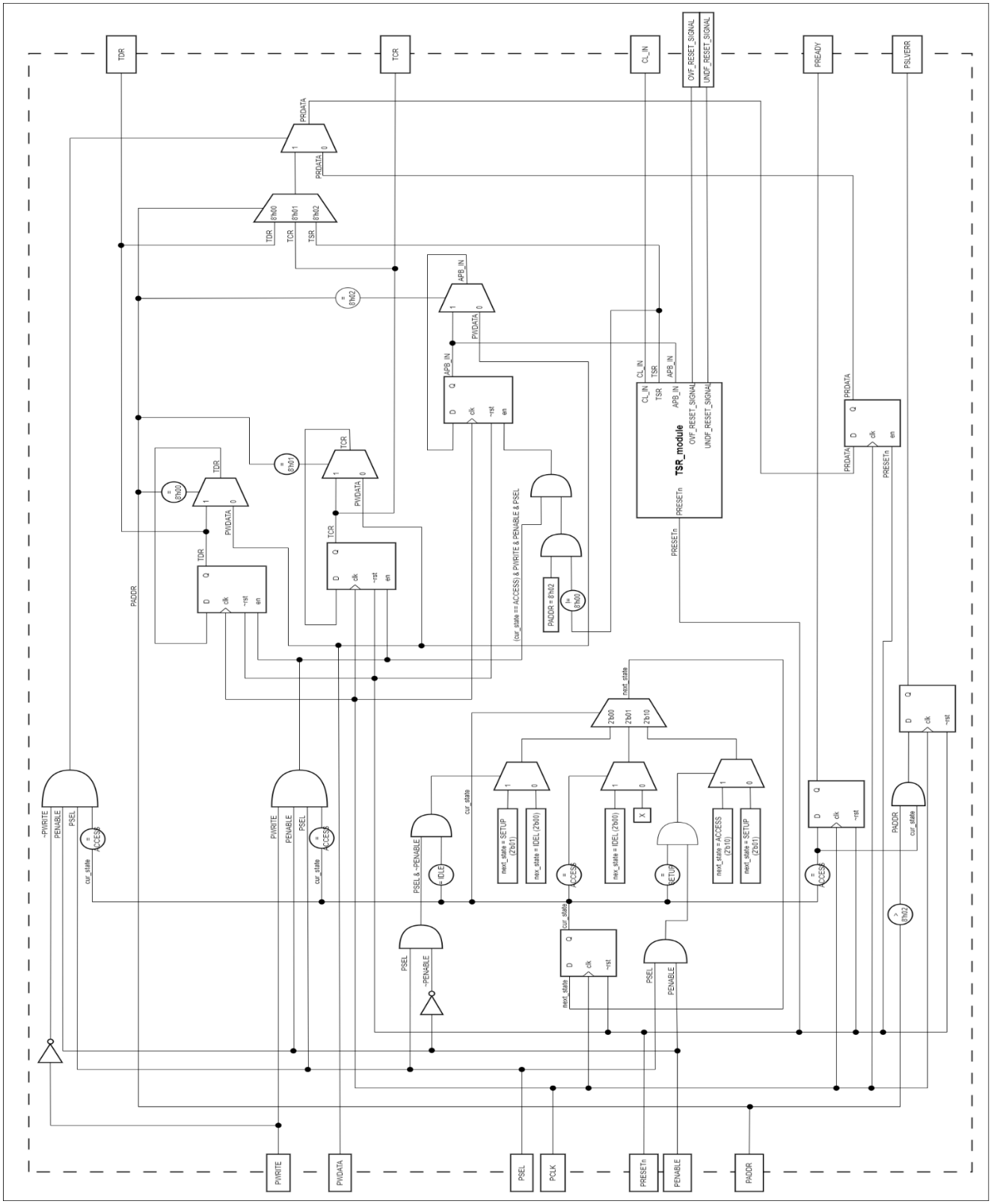

Figure 2-2 The Read/Write Control logic diagram

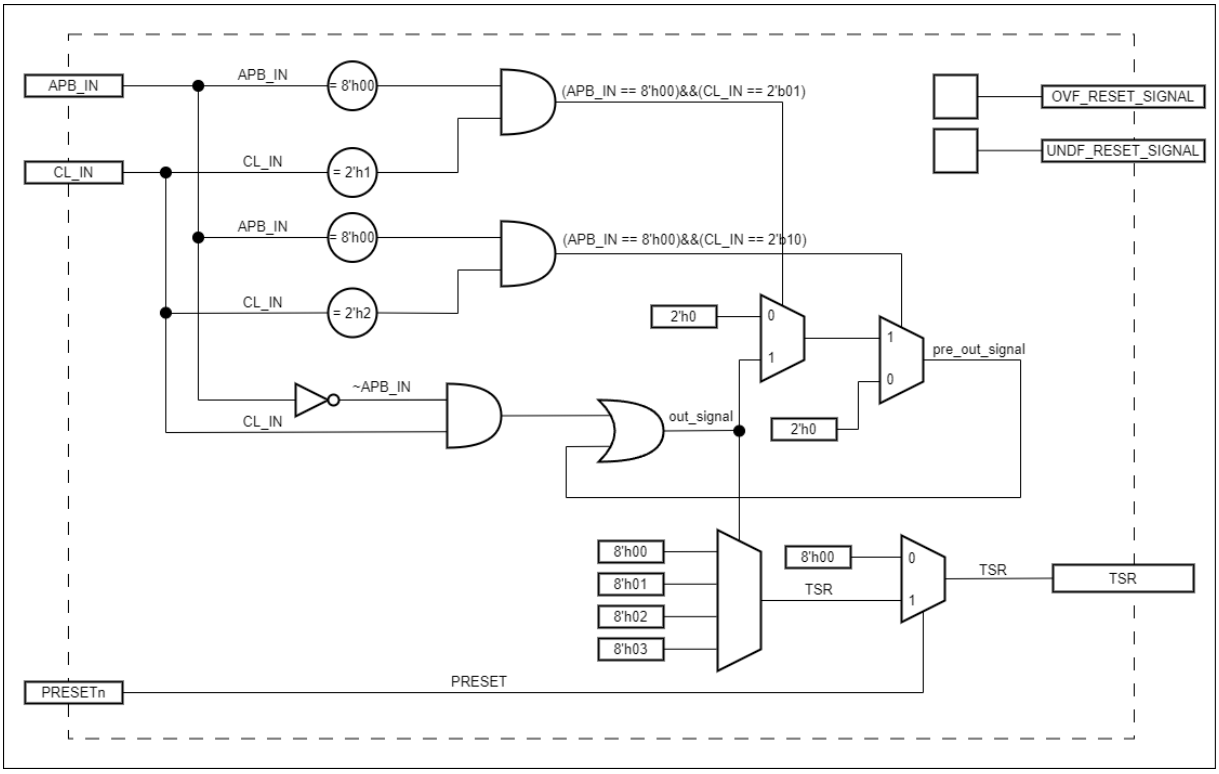

Figure 2-3 The TSR_module logic diagram

2.3 Input/Output pin

Pin name	Bit width	I/O	Function
PCLK	1-bit	Input	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	1-bit	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	1-bit	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PWRITE	1-bit	Input	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PENABLE	1-bit	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PADDR[7:0]	8-bit	Input	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.

PWDATA[7:0]	8-bit	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PRDATA[7:0]	8-bit	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY	1-bit	Output	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	1-bit	Output	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.
TDR	8-bit	Input/Output	This register contains the data used to update the value of the counter when this register is updated to the new value.
TCR	8-bit	Input/Output	TCR selects the clock source and the time at which TCNT is cleared and controls interrupts.
TSR	8-bit	Input/Output	TSR displays status flags and controls to compare match output.
CL_IN	2-bit	Input	Whenever overflow or underflow status register in the TCNT active HIGH, the Control Logic block will send a 2-bit signal to inform the TSR register to update its status. • CL_IN[0]: overflow status. • CL_IN[1]: underflow status.
OVF_RESET_SIGNAL	1-bit	Output	OVF_RESET_SIGNAL signal will reset the overflow register of the TCNT, through APB write transaction. The reset operation only worked when the overflow status in the TSR register has been raised.
UNDF_RESET_SIGNAL	1-bit	Output	UNDF_RESET_SIGNAL signal will reset the underflow register of the TCNT, through APB write transaction. The reset operation only worked when the underflow status in the TSR register has been raised.

2.4 Functional/Protocol

The Read/Write Control module operation is based on the AMBA 3 APB protocol, which consists of 3 types of responses:

- Write transfers with wait state.
- Read transfers with wait state.
- Error response.

The Read/Write Control module uses the APB protocol to perform Read/Write value on three registers described below:

- The TDR register: perform full Read/Write transaction.
- The TCR register: perform full Read/Write transaction.
- The TSR register: perform Read transaction on normal operation, the Write transactions are only allowed when Overflow, Underflow, or both statuses exist in the TSR register.

2.4.1 Read transfer

The APB read transaction can be performed on three registers TDR, TCR, and TSR.

- The transaction starts when both the PWRITE signal is driven LOW and the PSEL signal is asserted.
- After one cycle, the PENABLE signal will be asserted to inform the Read/Write Control that the SETUP state is beginning.
- The Read/Write Control block will wait for 2 cycles before driving the PREADY signal HIGH, informing that the beginning of the ACCESS state.
- During the ACCESS state, data from the appropriate address will be written to the PRDATA register.
- The ACCESS state exits after one cycle and signals PSEL, PENABLE, and PREADY are de-asserted.

Figure 2-4 shows a timing chart of a read transaction on the TDR register. Since the TDR register's default value is 8'h00, the received value after the transaction is 8'h00.

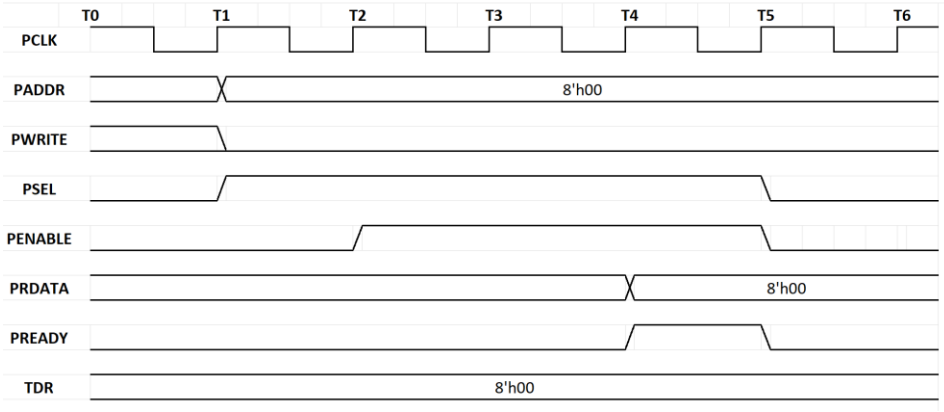

Figure 2-4 Read transfer with wait states on the TDR register

2.4.2 Write transfer

The APB write transaction can be performed on three registers TDR, TCR, and TSR.

- The transaction starts when both the PWRITE signal and PSEL are asserted.
- After one cycle, the PENABLE signal will be asserted to inform the Read/Write Control to start the SETUP state.
- The Read/Write Control block will wait for 2 cycles before driving the PREADY signal HIGH, and inform the beginning of the ACCESS state.
- During the ACCESS state, data from the PWDATA will be written to the appropriate address.
- The ACCESS state exits after one cycle and signals PSEL, PENABLE, and PREADY are de-asserted.

Figure 2-5 shows a timing chart of a write transaction on the TDR register. In this example, value 8'h01 will be written to the TDR register.

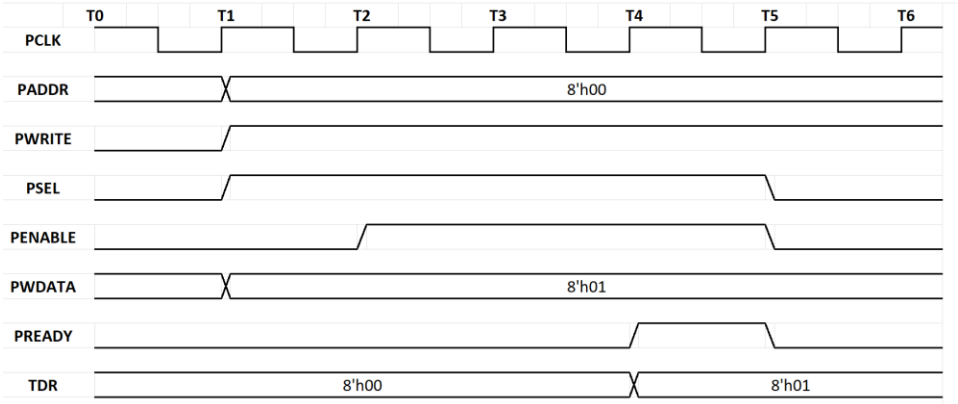

Figure 2-5 Write transfer with wait states on the TDR register

For the TSR register, write transaction only available when the Overflow or Underflow status has existed. If the condition is not met, the write transaction has no effect on the value of the TSR register.

The logic table below summarizes the status of the TSR[0] bit based on two signal inputs APB[0] and CL_IN[0].

APB[0]	CL_IN[0]	TSR[0]
0	0	0
0	1	1
1	0	0
1	1	0

Figure 2-6 shows the write transaction performed on the TSR register when its overflow and underflow status has not been activated.

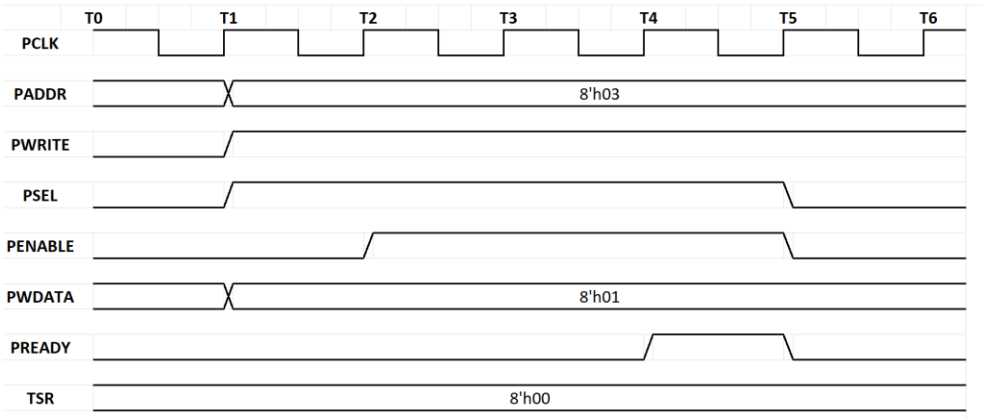

Figure 2-6 Write transfer with wait states on the TSR register (default value)

Figures 2-7, 2-8, and 2-9 show the write transaction performed on the TSR register when:

- Only overflow status is on (TSR register status bit number [0]).
- Only underflow status is on (TSR register status bit number [1]).
- Both overflow and underflow status are activated.

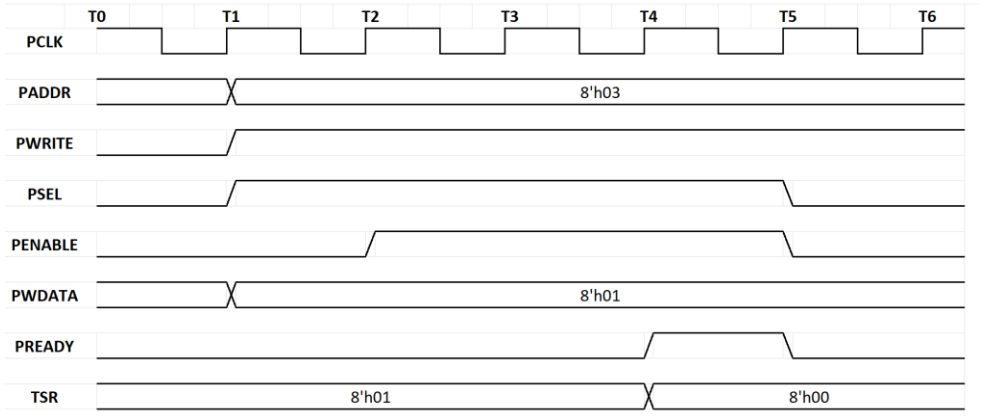

Figure 2-7 Write transfer on the TSR register when overflow has been raised

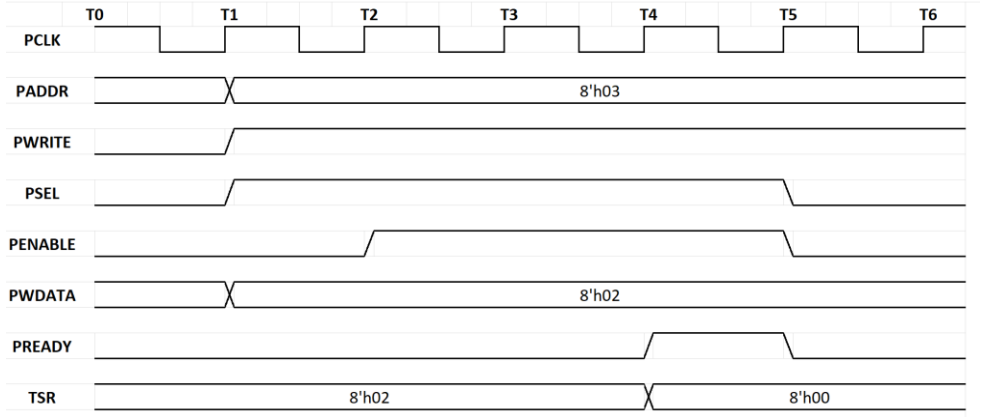

Figure 2-8 Write transfer on the TSR register when underflow has been raised

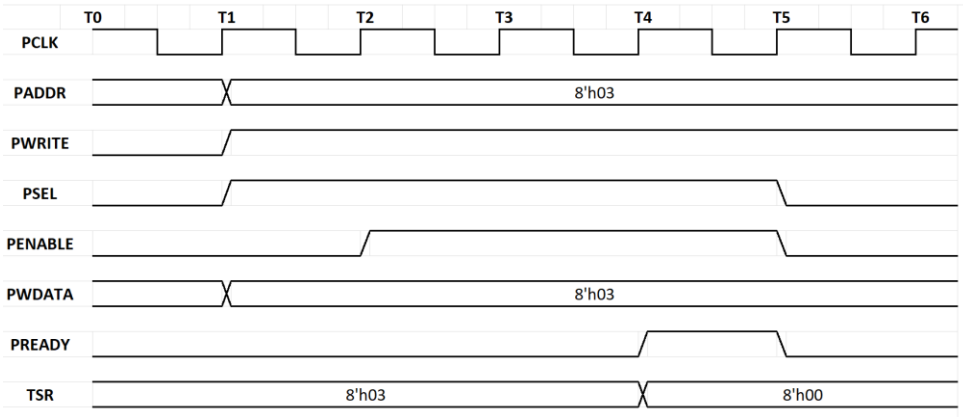

Figure 2-9 Write transfer on the TSR register when both flags have been raised

2.4.3 Error response

The PSLVERR signal will be asserted if one of these scenarios happens:

- Write transactions to an undefined address (the address must be equal to 8'h00 OR 8'h01 OR 8'h02).
- Read transactions on an undefined address.

PSLVERR is only considered valid during the last cycle of an APB transfer when PSEL, PENABLE, and PREADY are all HIGH.

[1] Write transfer

Figure 2-10 shows an example of a failing write transfer. In this example, the write transaction is performed on an undefined address 8'hFF.

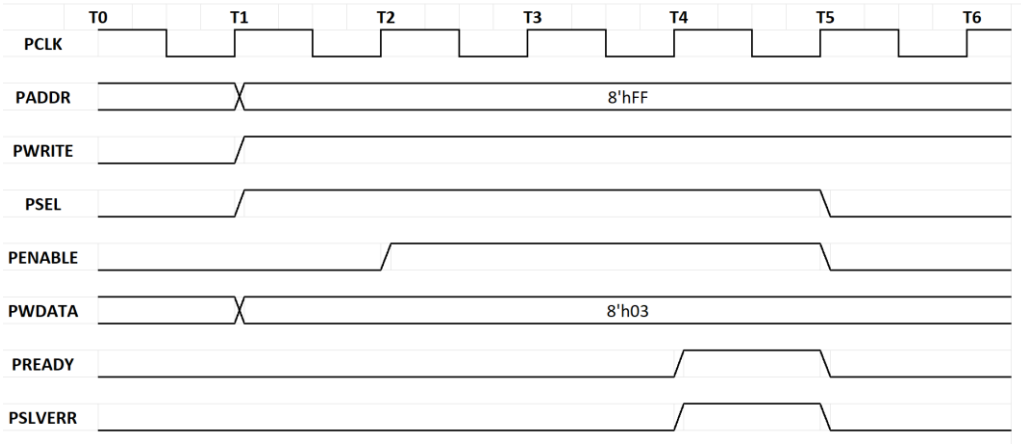

Figure 2-10 Example failing write transfer

[2] Read transfer

Figure 2-11 shows a read transfer completed with an error response, the operation performed on an undefined address. The value return on the PRDATA register is 8’hxx.

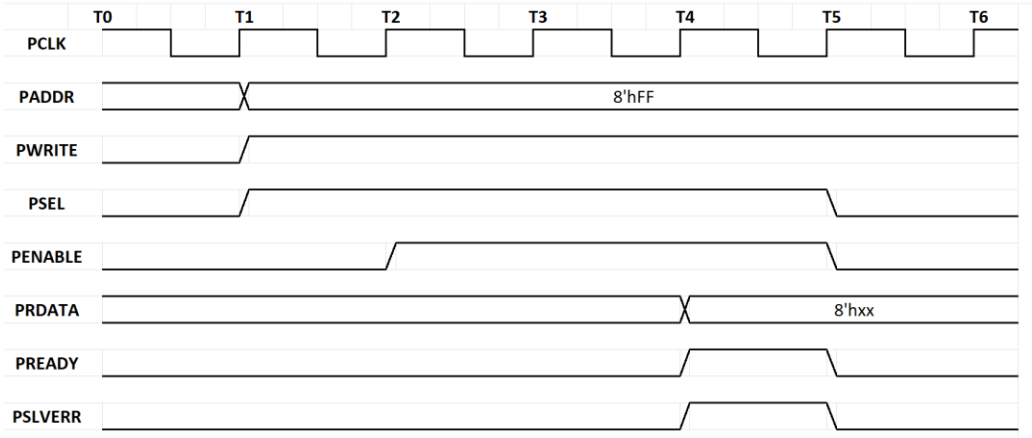

Figure 2-11 Example failing read transfer

3. Timer counter (TCNT)

3.1 Logic diagrams

Figure 3-1 shows the logic diagram of the TCNT module.

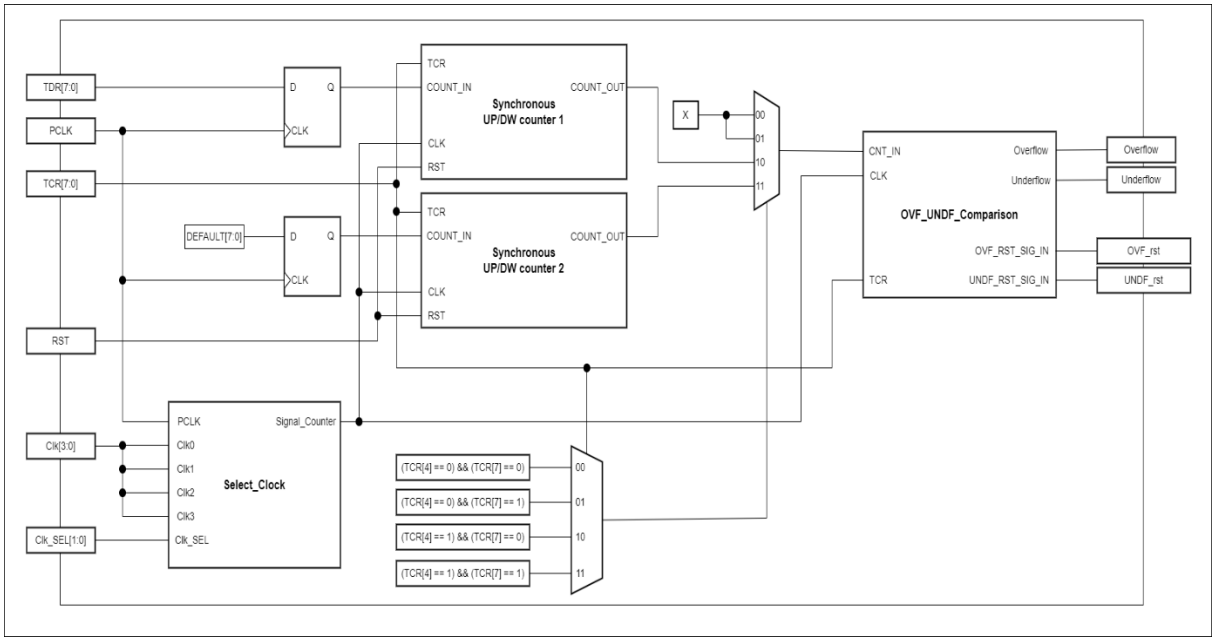

Figure 3-1 The TCNT module logic diagram

Figure 3-2 and 3-3 show the logic diagrams of the Select Clock module and the synchronous UP/DW counter.

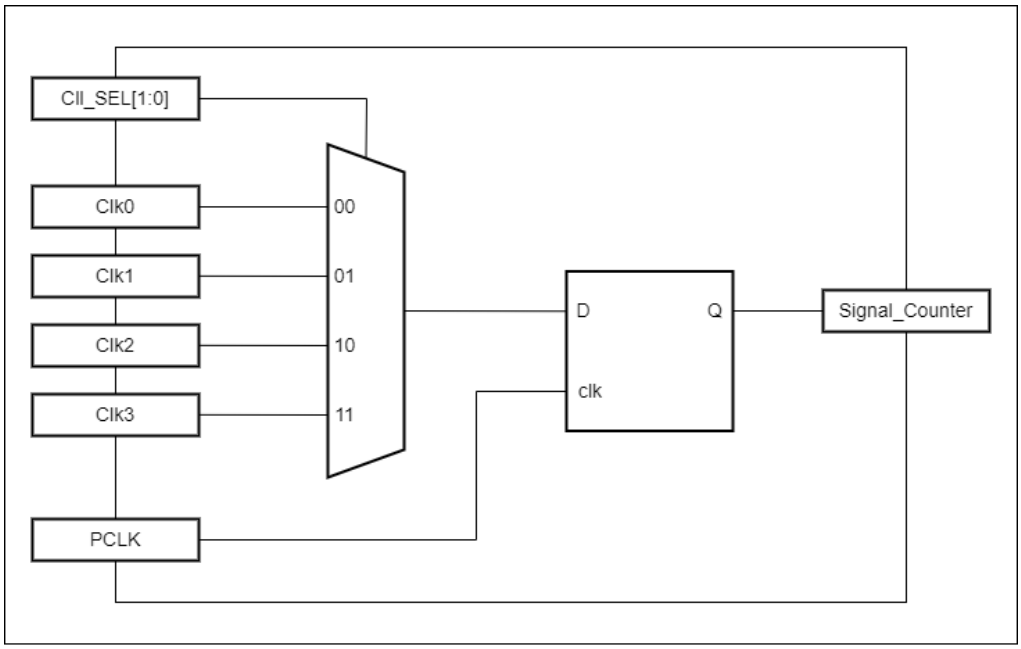

Figure 3-2 The Select Clock module logic diagram

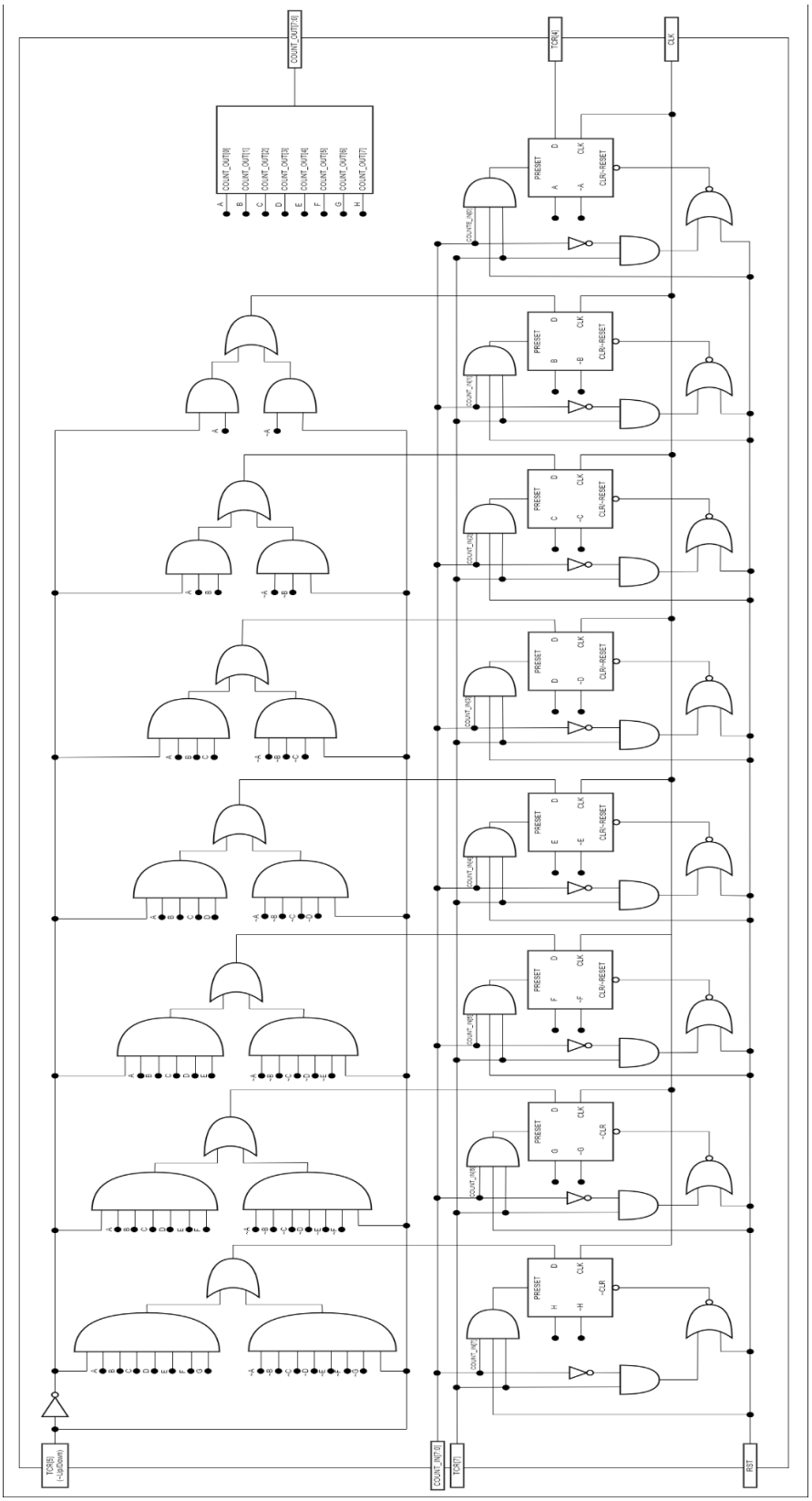

Figure 3-3 The synchronous UP/DW counter

3.2 Input/Output pins

Pin name	Bit width	I/O	Function
PCLK	1-bit	Input	System clock. The rising edge of PCLK times all transfers on the APB.
RST	1-bit	Input	Reset signal
Clk	4-bit	Input	The clock source for the counter timer. Each clock has a different frequency.
Clk_SEL	2-bit	Input	Input signal from the Control Logic module is used to choose the appropriate internal clock pulse.
TDR	8-bits	Input	The TDR value is used for the TCNT's load data mode.
TCR	8-bit	Input	The TCR register value contains the configurations bit for the TCNT
OVF_rst	1-bit	Input	The reset signal for the internal Overflow register, comes from the Read/Write Control module.
UNDF_rst	1-bit	Input	The reset signal for the internal Underflow register, comes from the Read/Write Control module.
Overflow	1-bit	Output	The output signal from the internal register indicates the Overflow status.
Underflow	1-bit	Output	The output signal from the internal register indicates the Underflow status.

3.3 Functional/Protocol

The TCNT contains two synchronous UP/DW counters. First, the TCNT reads the configurations bit from the TCR register and then decides the appropriate operations.

Figure 3-4 shows a normal operation of the TCNT module with the TCR register value equal to 8'h10:

- TCR[7] = 0: Normal operation, start count from 8'h00, the DEFAULT register will equal to 8'h00.
- TCR[5] = 0: Count up.
- TCR[4] = 1: Enable the TCNT module.
- TCR[1:0] = 2'b00: Select internal clock pulse T*2.

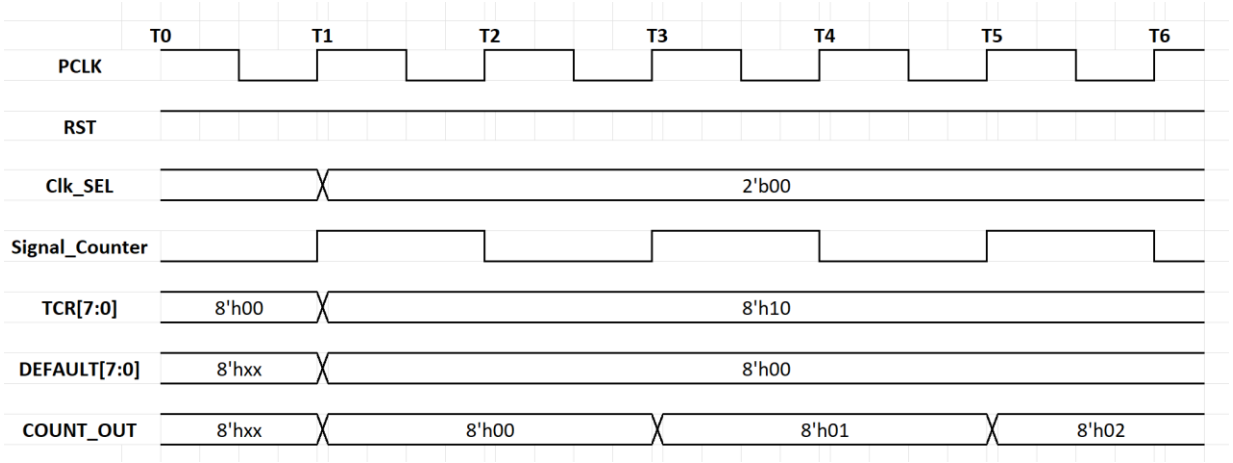

Figure 3-4 The TCNT normal operation.

Figure 3-5 shows a load data operation of the TCNT module with the TCR register value equal to 8'h90 and the TDR register value equal to 8'h8A.

- TDR[7:0] = 8'h8A.
- TCR[7] = 0: Load data operation, start count from 8'h8A.
- TCR[5] = 0: Count up.
- TCR[4] = 1: Enable the TCNT module.
- TCR[1:0] = 2'b00: Select internal clock pulse T*2.

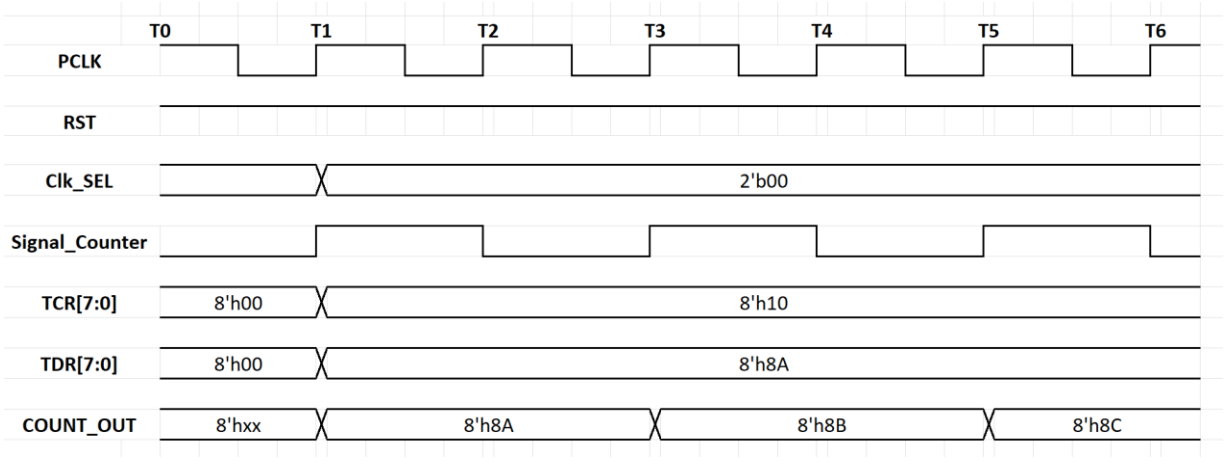

Figure 3-5 The TCNT load data operation.

Figure 3-6 shows the TCNT module operation when Overflow happened. The TCR register value is 8'h10. The internal Overflow register is set to HIGH when the COUNT_OUT signal is switched from 8'hFF to 8'h00.

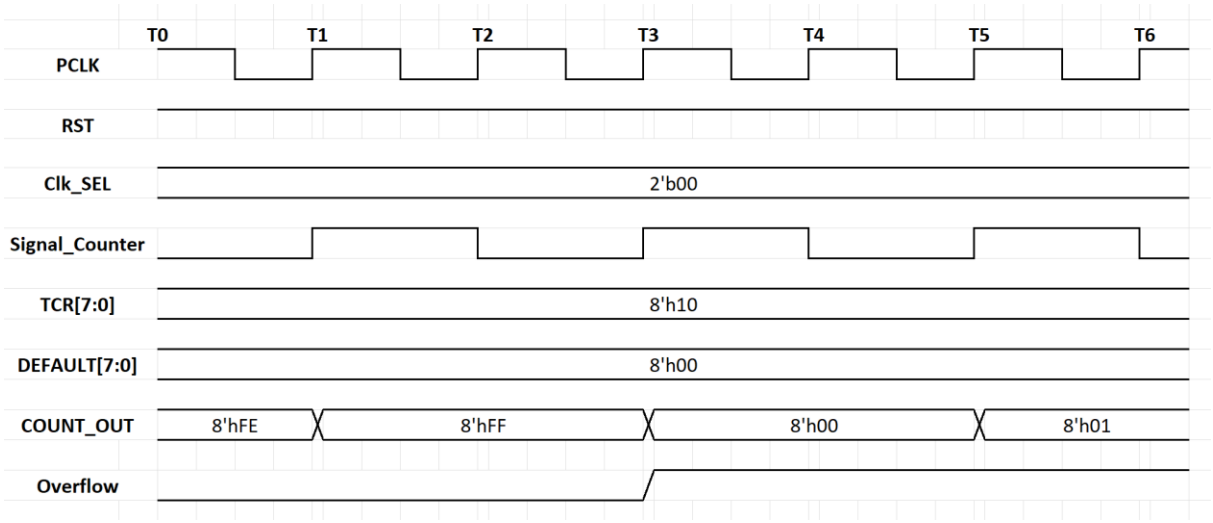

Figure 3-6 The TCNT when Overflow occurs.

Figure 3-7 shows the TCNT module operation when toggle the RST signal (Reset). The COUNT_OUT signal value will be reset to 8'h00, however, if either of the Overflow or Underflow status has appeared previously, it will not be affected by this signal.

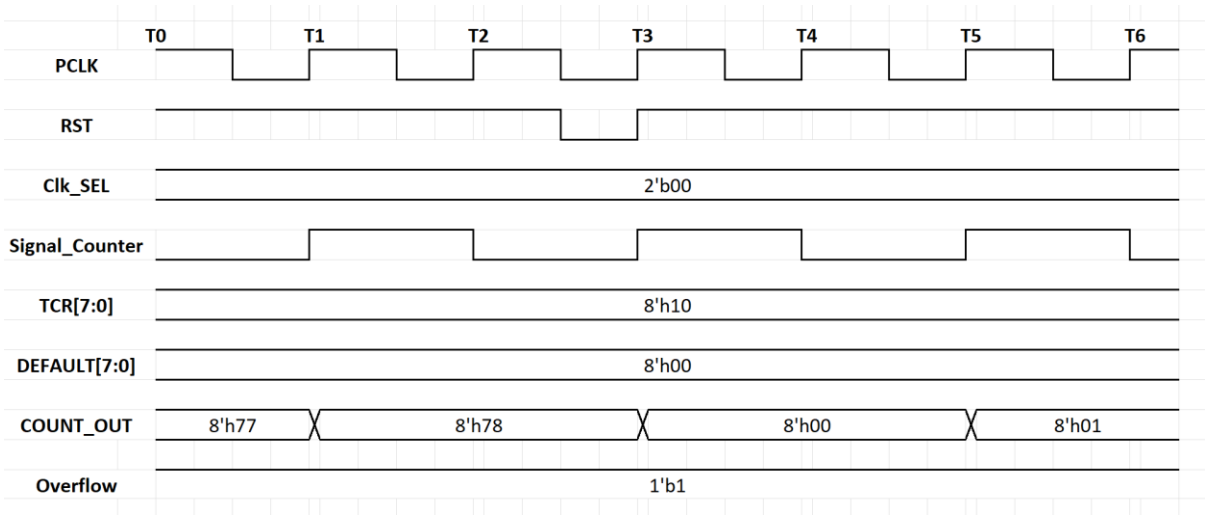

Figure 3-7 The TCNT reset counting operation.

Figure 3-8 shows the TCNT module operation when the Overflow status bit in the TSR register is cleared by the APB WRITE transaction. The Read/Write Control module will send a signal to reset the status register on the TCNT module.

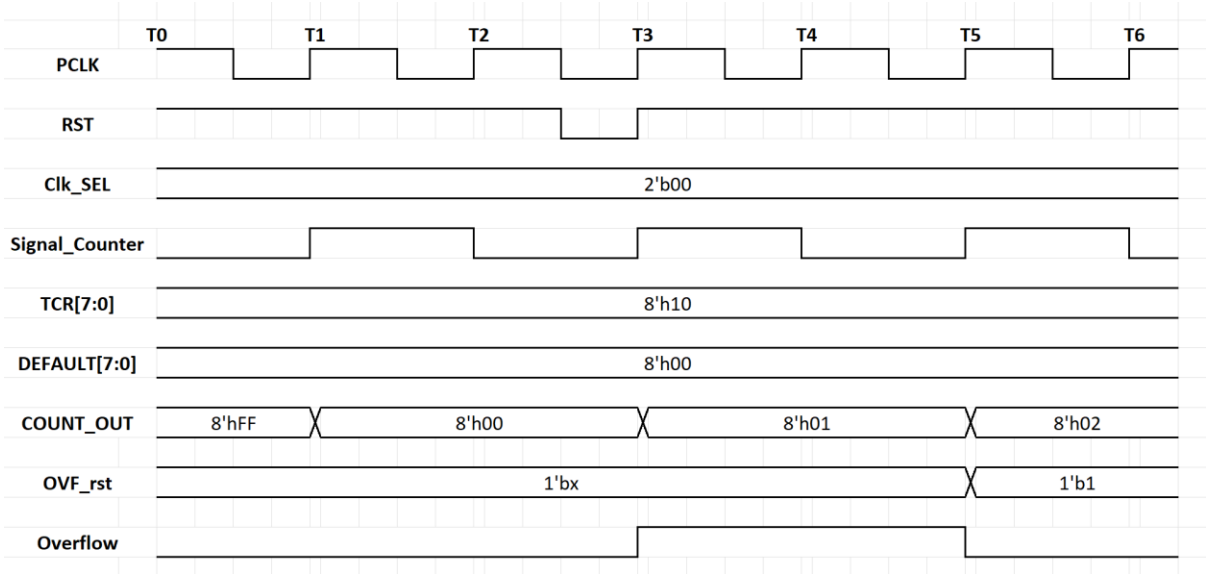

Figure 3-8 The TCNT reset Overflow register status operation.

Figure 3-9 shows the TCNT module operation when it is being disabled for 2 cycles. After being enabled, the TCNT continues to count from the previous value.

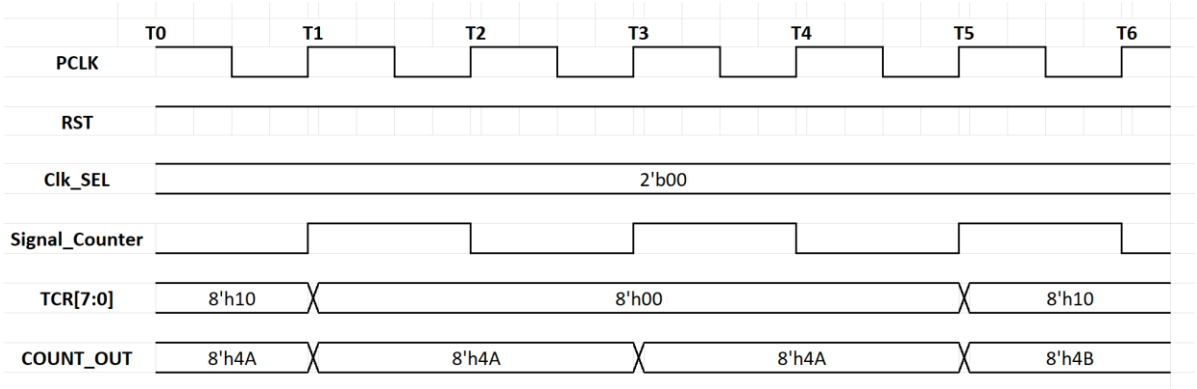

Figure 3-9 The TCNT operation during 2 cycles disabled.

4. Control logic

4.1 Logic diagram

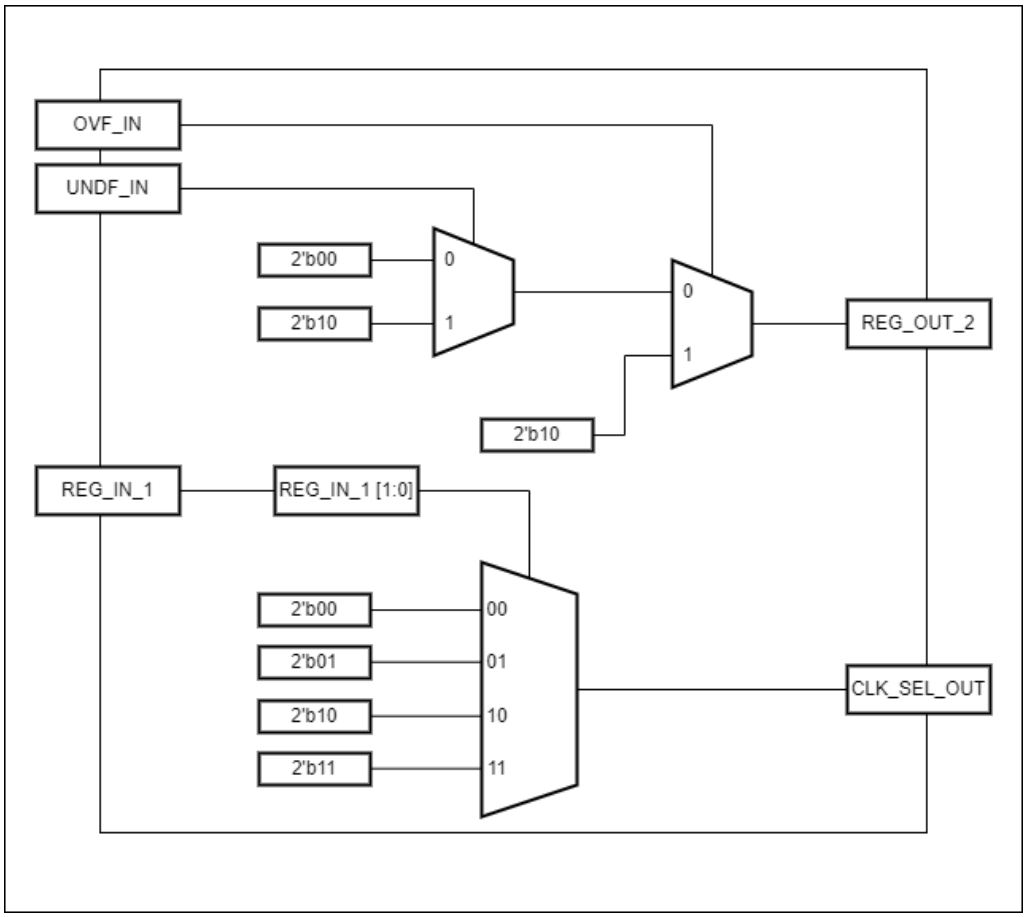

Figure 4-1: The Control logic diagram

4.2 Input/Outputs pin

Pin name	Bit width	I/O	Function
OVF_IN	1-bit	Input	Input signal, toggle when Overflow state is triggered in the TCNT block.
UNDF_IN	1-bit	Input	Input signal, toggle when Underflow state is triggered in the TCNT block.
REG_IN_1	8-bit	Input	Input signal from the TCR register, the Control Logic block reads the Cks[1:0], then decides the internal clock pulse.
REG_OUT_2	8-bit	Output	Output signal, sent from the Control Logic module to set bit status in the TSR register.
CLK_SEL_OUT	2-bit	Output	Output signal, after the clock selection, the value arranges from:

			• 00: T*2 • 01: T*4 • 10: T*8 • 11: T*16

4.3 Functional/Protocol

4.3.1 Set the status bit on the TSR register

Receive Overflow or Underflow signal from the TCNT and set the status bits 1 and 0 on the TSR register.

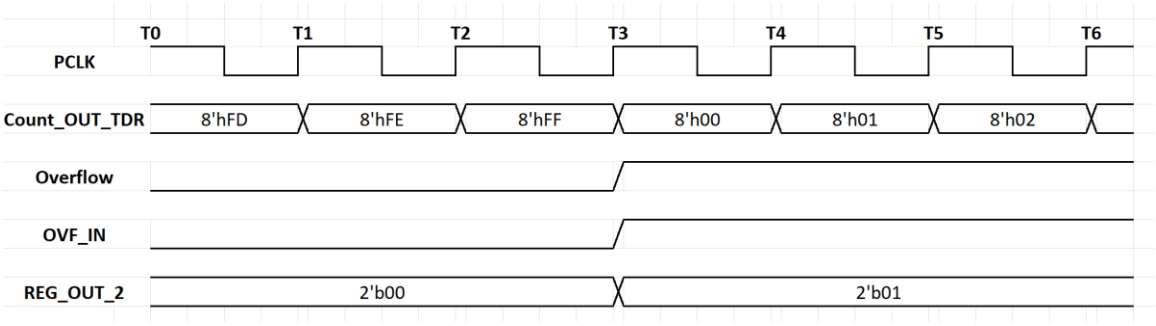

Figure 4-2: The Control Logic timing chart when the Overflow flag is raised.

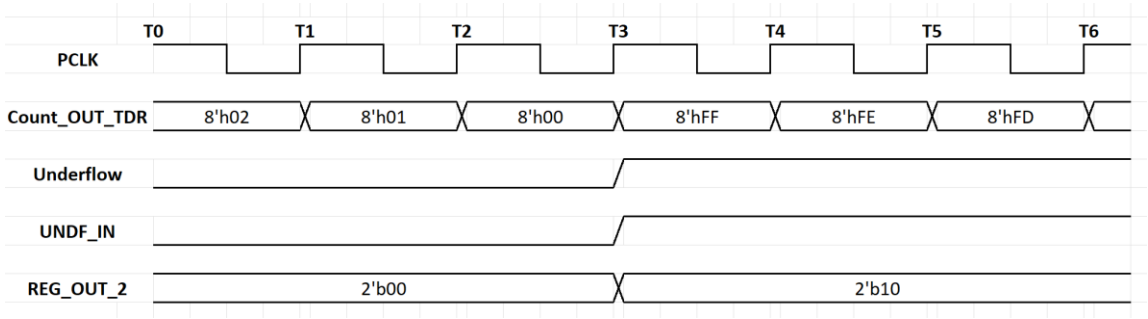

Figure 4-3: The Control Logic timing chart when the Underflow flag is raised.

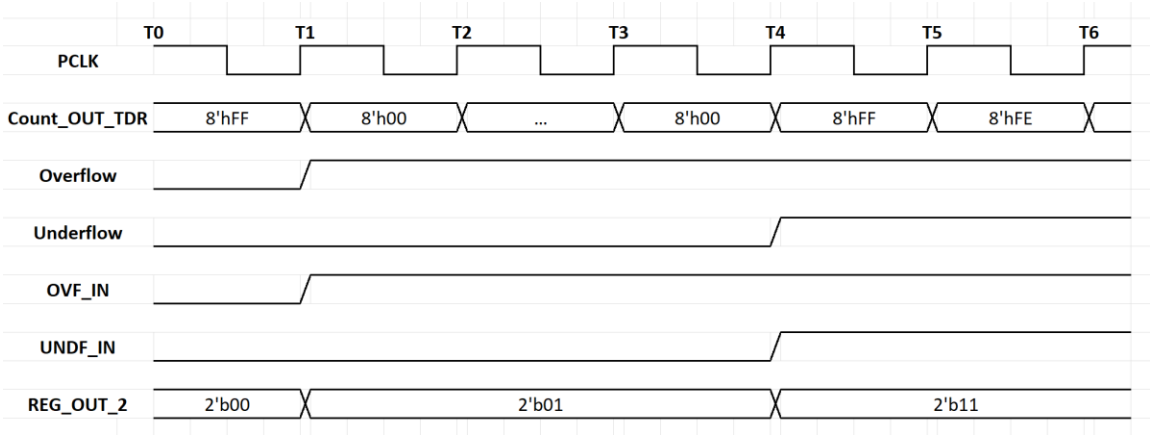

Figure 4-4: The Control Logic when both flags are raised.

4.3.2 Select the internal clock pulse based on the TCR's Cks[1:0] bit.

Receive bits Cks[1:0] from the TCR register and decide which internal clock pulse will be used for the TCNT. The clock pulse selected will be transmitted through the CLK_SEL_OUT signal.

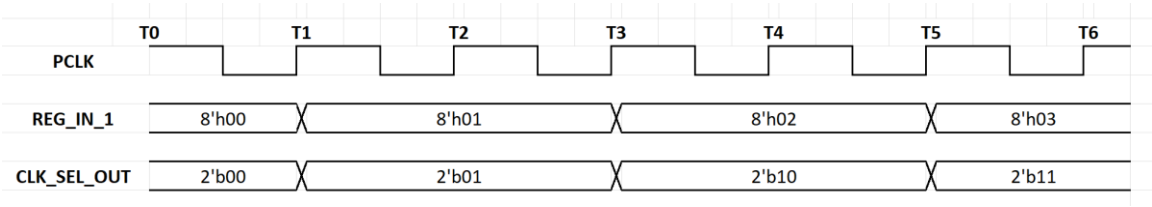

Figure 4-5: The Control Logic output based on Cks[1:0] bit status.