TIMER DESIGN

1. Overview

This 8-bit timer module operates on the basis of an 8-bit counter. The 8-bit timer module can be used to count external events and be used as a multifunction timer in a variety of applications, such as generation of counter reset, and interrupt requests.

1.1 Feature

- Selection of four clock sources.
- Read/Write control using APB protocol. PSLVERR will activate high when the transmission fails.
- Two counting operations, including normal operation and load data from TDR register operation.
- Setting the Timer counter (TCNT) through the TCR register.
- Showing Overflow and Underflow status on the TSR register, and the register status can be reset using APB transfer.

1.2 Block diagram

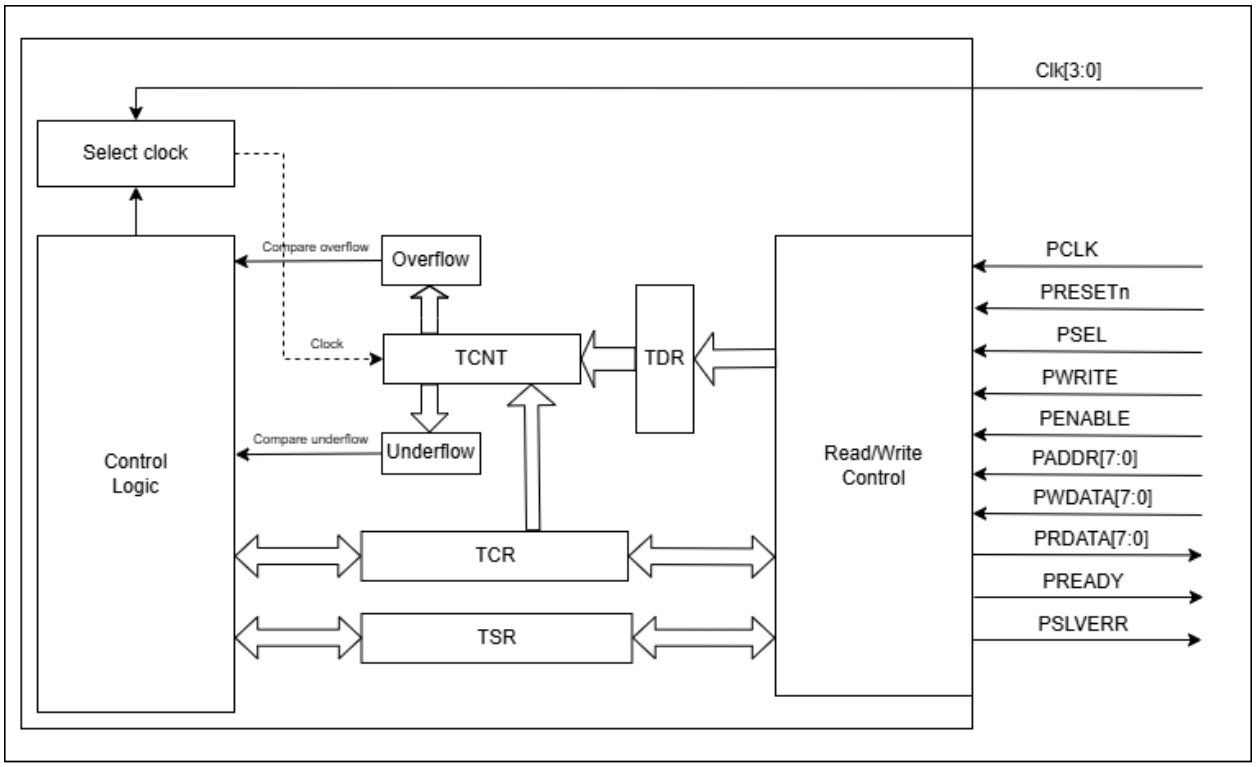

Figure 1-1 Block diagram of TMR Block (Timer)

1.3 Input/Output pin (LSI pin – CHIP PIN/PORT)

Pin name	Source	Bit width	I/O	Function

Clk[3:0]	Clock source	4 bits	Input	The clock source for the counter timer. Each clock has a different frequency.
PCLK	System clock	1 bit	Input	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	System reset	1 bit	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	APB bridge	1 bit	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PWRITE	APB bridge	1 bit	Input	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PENABLE	APB bridge	1 bit	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PADDR[7:0]	APB bridge	8 bits	Input	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PWDATA[7:0]	APB bridge	8 bits	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PRDATA[7:0]	Slave interface	8 bits	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY	Slave interface	1 bit	Output	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	Slave interface	1 bit	Output	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

1.4 Register specification

The 8-bit timer module has the following registers.

- Timer Data Register (TDR).
- Timer counter Control Register (TCR).
- Timer Status Register (TSR).

1.4.1 Timer Data Register (TDR)

This register contains the data used to update the value of the counter when this register is updated to the new value.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDR[7]	TDR[6]	TDR[5]	TDR[4]	TDR[3]	TDR[2]	TDR[1]	TDR[0]

Bit name	F/V	Description
TDR[7:0]	R/W	Data is used to update the value of the counter.

1.4.2 Timer counter Control Register (TCR)

The APB protocol is setting this register value, each bit in the TCR register consists of a setting for the bellow attributes:

- Operations selection between loading data from TDR to TCNT and normal operation.
- Counting order selection.
- Enabling counting mode.
- Select the internal clock, based on the selections *2, *4, *8, *16.
  Internal _clock = PCLK (system clock) * Selected_value

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Load	Reserved	Up/Dw	En	Reserved	Reserved	Cks1	Cks0

Bit name	F/V	Description
Load[7]	R/W	Manual load data from TDR to TCNT when it is active High. 1: load data to TCNT 0: Normal operation
6	Reserved	Reserved
Up/Dw[5]	R/W	Control counter up or counter down 0: counter up 1: counter down
En[4]	R/W	0: disable 1: enable
3:2	Reserved	Reserved
Cks[1:0]	R/W	Select internal clocks for the circuit

		00: T*2 01: T*4 10: T*8 11: T*16

1.4.3 Timer Status Register (TSR)

TSR displays status flags and controls to compare match output.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_TMR_UDF	S_TMR_OVF

Bit name	R/W	Description
7:2	R	Reserved
S_TMR_UDF[1]	R/W*	Timer counter underflow when counter 8'h00 down to 8'hff: This bit is only set by hardware, clear by software
S_TMR_OVF[0]	R/W*	Timer counter overflow when counter 8'hFF to 8'h00: This bit is only set by hardware, clear by software

2. Read/write register control

2.1 Block diagram

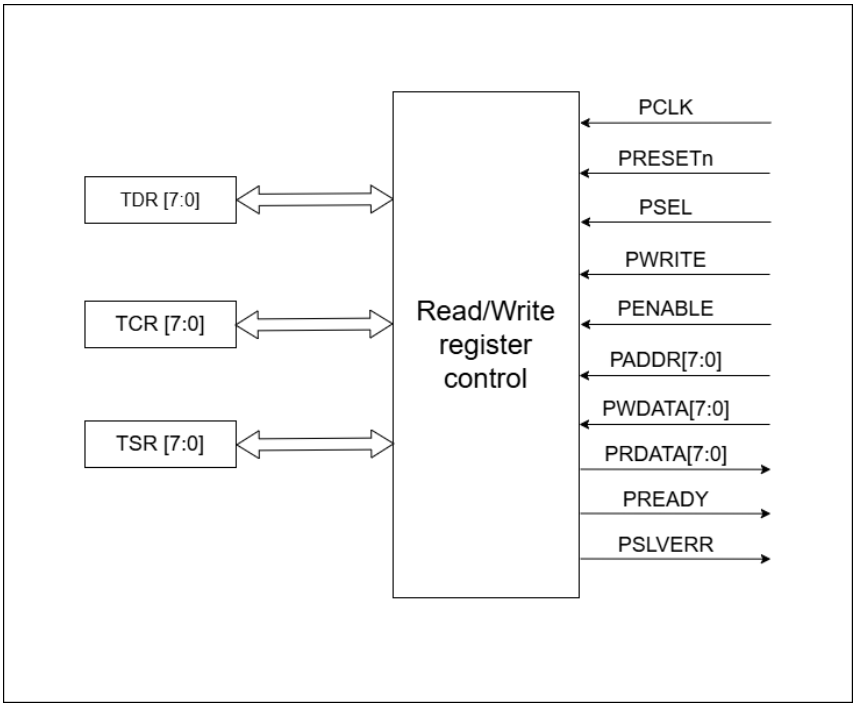

Figure 2-1 Read/Write register control block

2.2 Input/Output pin

Pin name	Bit width	I/O	Function
PCLK	1 bit	Input	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	1 bit	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	1 bit	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PWRITE	1 bit	Input	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PENABLE	1 bit	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.

PADDR[7:0]	8 bits	Input	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PWDATA[7:0]	8 bits	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PRDATA[7:0]	8 bits	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY	1 bit	Output	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	1 bit	Output	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.
TDR	8 bits	Input/ Output	This register contains the data used to update the value of the counter when this register is updated to the new value.
TCR	8 bits	Input/ Output	TCR selects the clock source and the time at which TCNT is cleared and controls interrupts.
TSR	8 bits	Input/ Output	TSR displays status flags and controls to compare match output.

2.3 Functional/Protocol

The Read/Write register block operation is based on the AMBA 3 APB protocol, which consists of 3 types of responses:

- Write transfers.
- Read transfers.
- Error response.

2.3.1 Write transfer

Two types of write transfer are described in this section:

• With no wait states

• With wait states.

[1] With no wait state

Figure 2-2 shows a basic write transfer with no wait states.

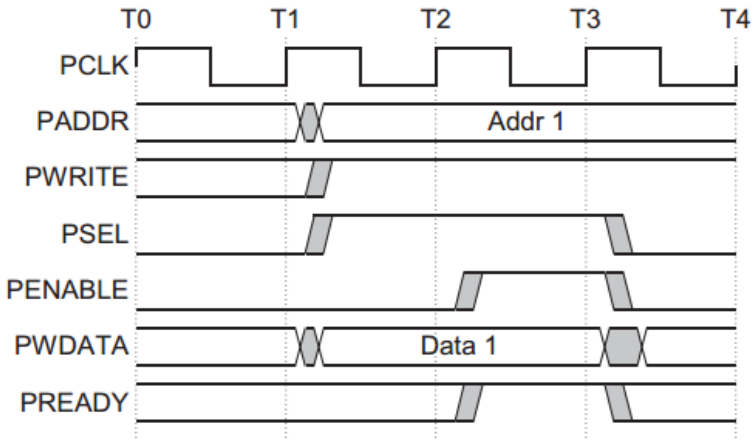

Figure 2-2 Write transfer with no wait states

The write transfer starts with the address, write data, write signal, and select signal all changing after the rising edge of the clock. The first clock cycle of the transfer is called the Setup phase. After the following clock edge, the enable signal is asserted, PENABLE, and this indicates that the Access phase is taking place. The address, data, and control signals all remain valid throughout the Access phase. The transfer is completed at the end of this cycle.

The enable signal, PENABLE, is deasserted at the end of the transfer. The select signal, PSELx, also goes LOW unless the transfer is to be followed immediately by another transfer to the same peripheral.

[2] With wait state

Figure 2-3 shows how the PREADY signal from the slave can extend the

transfer. During an Access phase, when PENABLE is HIGH, the transfer can be

extended by driving PREADY LOW. The following signals remain unchanged for the

additional cycles:

- address, PADDR.
- write signal, PWRITE.
- select signal, PSEL.
- enable signal, PENABLE.
- write data, PWDATA.

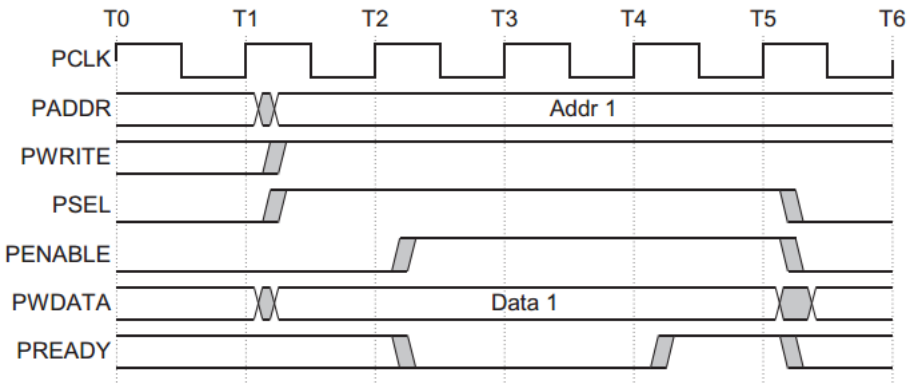

Figure 2-3 Write transfer with wait states

PREADY can take any value when PENABLE is LOW. This ensures that peripherals that have a fixed two-cycle access can tie PREADY HIGH.

Note: It is recommended that the address and write signals are not changed immediately after a transfer but remain stable until another access occurs. This reduces power consumption.

2.3.2 Read transfer

Two types of read transfer are described in this section:

- With no wait states
- With wait states.

[1] With no wait state

Figure 2-4 shows a read transfer. The timing of the address, write, select, and enable signals are as described in Write transfers in section 2.3.1. The slave must provide the data before the end of the read transfer.

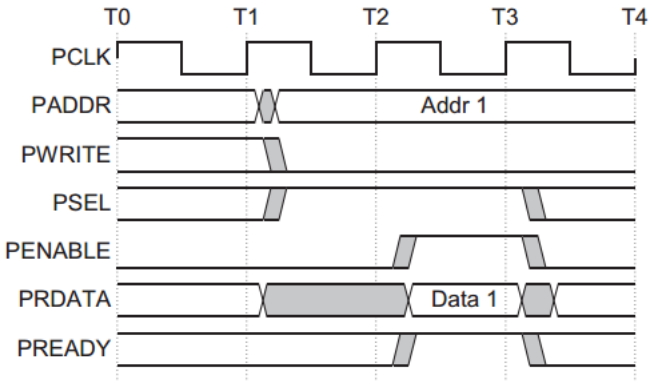

Figure 2-4 Read transfer with no wait states

[2] With wait state

Figure 2-5 shows how the PREADY signal can extend the transfer. The transfer is extended if PREADY is driven LOW during an Access phase. The protocol ensures that the following remain unchanged for the additional cycles:

- address, PADDR
- write signal, PWRITE
- select signal, PSEL
- enable signal, PENABLE.

Figure 2-5 shows that two cycles are added using the PREADY signal.

However, you can add any number of additional cycles, from zero upwards.

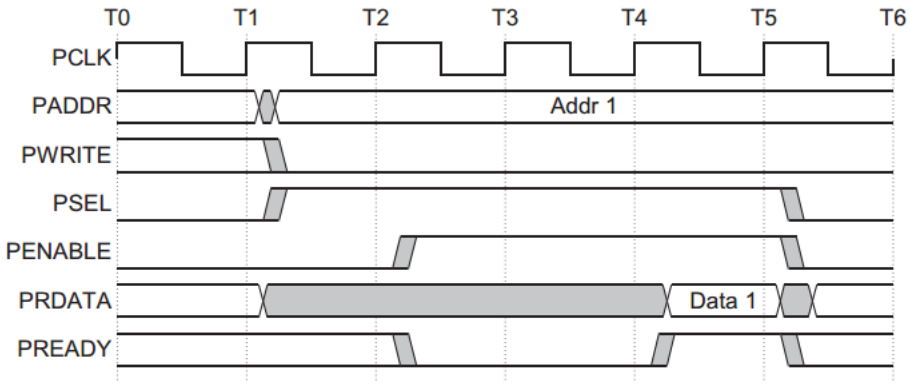

Figure 2-5 Read transfer with wait states

2.3.3 Error response

- You can use PSLVERR to indicate an error condition on an APB transfer. Error conditions can occur on both read and write transactions.
- PSLVERR is only considered valid during the last cycle of an APB transfer when PSEL, PENABLE, and PREADY are all HIGH.
- It is recommended, but not mandatory, that you drive PSLVERR LOW when it is not being sampled. That is when any of PSEL, PENABLE, or PREADY are LOW.
- Transactions that receive an error, might or might not have changed the state of the peripheral. This is peripheral-specific and either is acceptable. When a write transaction receives an error this does not mean that the register within the peripheral has not been updated. Read transactions that receive an error can return invalid data. There is no requirement for the peripheral to drive the data bus to all 0s for a read error.
- APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

[1] Write transfer

Figure 2-6 shows an example of a failing write transfer that completes with an error.

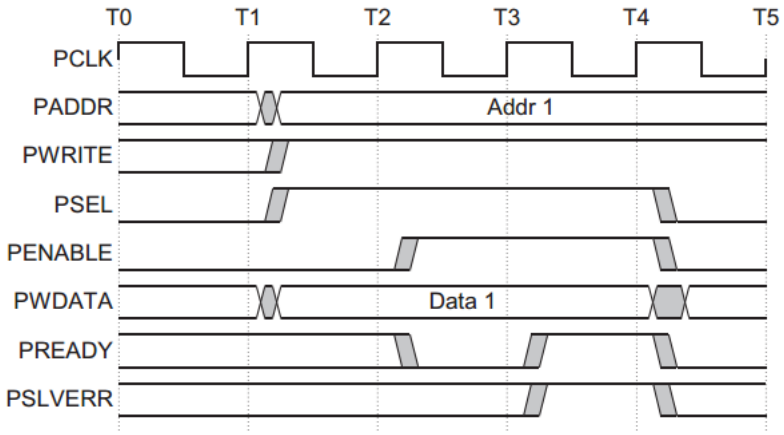

Figure 2-6 Example failing write transfer

[2] Read transfer

A read transfer can also be completed with an error response, indicating that there is no valid read data available. Figure 2-7 shows a read transfer completed with an error response.

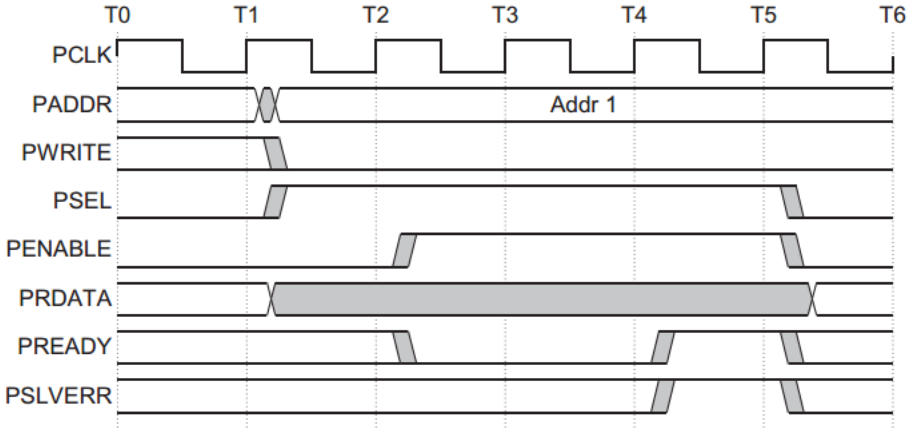

Figure 2-7 Example failing read transfer

[3] Mapping of PSLVERR

When bridging:

- From AXI to APB An APB error is mapped back to RRESP/BRESP = SLVERR. This is achieved by mapping PSLVERR to the AXI signals RRESP[1] for reads and BRESP[1] for writes.

- From AHB to APB PSLVERR is mapped back to HRESP = ERROR for both reads and writes. This is achieved by mapping PSLVERR to the AHB signal HRESP[0].

2.4 Design circuit

Figure 2-8 shows the operational activity of the APB.

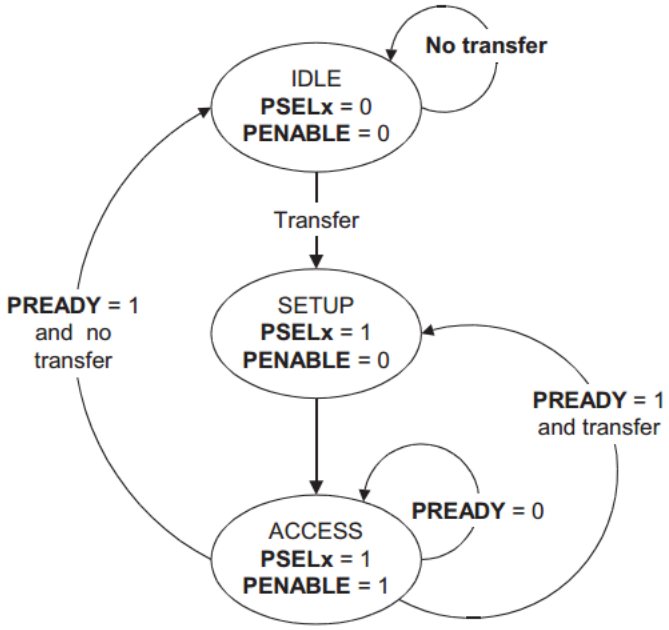

Figure 2-8 State diagram

The state machine operates through the following states:

State	Description
IDLE	This is the default state of the APB.
SETUP	When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, PSELx, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.
ACCESS	The enable signal, PENABLE, is asserted in the ACCESS state. The address, write, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the PREADY signal from the slave: • If PREADY is held LOW by the slave then the peripheral bus remains in the ACCESS state. • If PREADY is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

2.5 Timing chart

For details of each timing chart, refer to section 2.3, Function/Protocol.

- Write transfer with no wait state timing chart – Figure 2-2
- Write transfer with wait state timing chart – Figure 2-3
- Read transfer with no wait state timing chart – Figure 2-4
- Read transfer with wait state timing chart – Figure 2-5
- Error response in write transfer timing chart – Figure 2-6
- Error response in read transfer timing chart – Figure 2-7

3. Timer counter (TCNT)

3.1 Block diagram

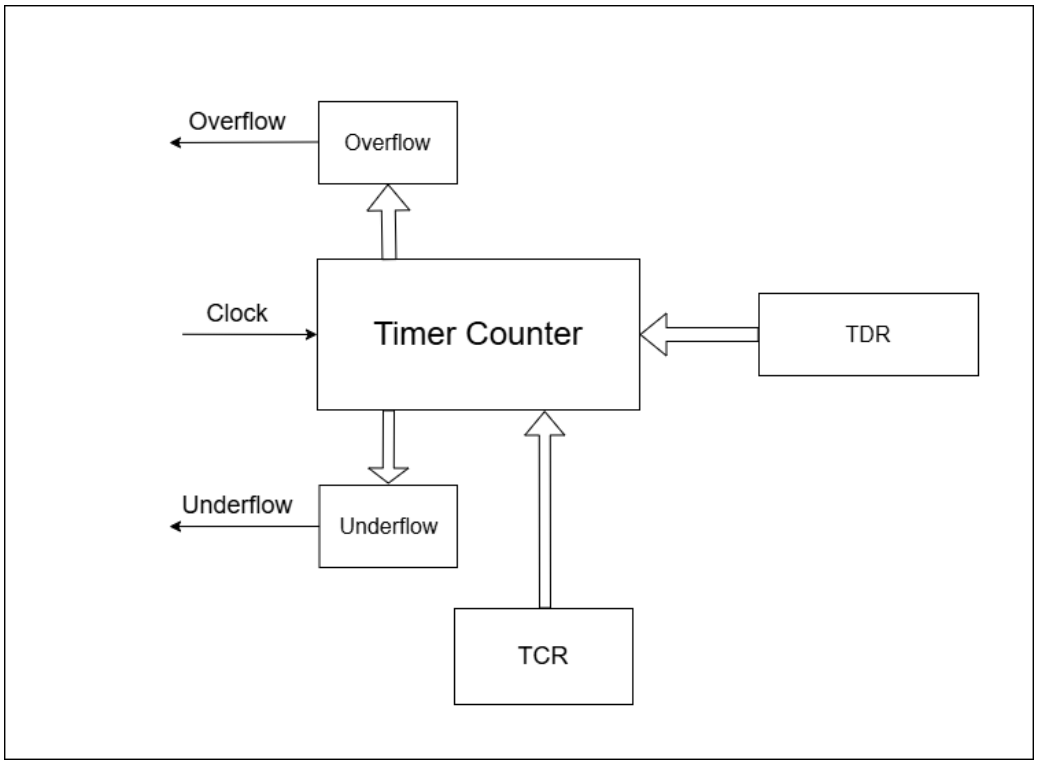

Figure 3-1 Timer counter block

3.2 Input/Output pins

Pin name	Bit width	I/O	Function
PCLK	1 bit	Input	System clock. The rising edge of PCLK times all transfers on the APB.
Overflow	1 bit	Output	The control logic block uses this signal to know when the overflow event happened.
Underflow	1 bit	Output	The control logic block uses this signal to know when the underflow event happened.
Clock_count	1 bit	Input	The selected clock frequency signal from the Clock select block
TDR	8 bits	Input	The signal came from the TDR register, which contains

			the data used to update the value of the counter when this register is updated to the new value.
TCR	8 bits	Input	This register has the counter configurations on bits 7, 5, and 4.

3.3 Functional/Protocol

TCNT is an 8-bit counter. The counter is connected to two registers Overflow and Underflow. Each register holds a value if one of the above events happens. TDR register will save the status of the counter in bit S_TMR_UDF[1] and bit S_TMR_OVF[0]. Overflow and Underflow status can be cleared by setting an APB signal to the TDR register.

TCNT operation can be set by sending data to the TCR register:

Bit name	F/V	Description
Load[7]	R/W	Manual load data from TDR to TCNT when it is active High. 1: load data to TCNT 0: Normal operation
Up/Dw[5]	R/W	Control counter up or counter down 0: counter up 1: counter down
En[4]	R/W	0: disable 1: enable
Cks[1:0]	R/W	Select internal clocks for the circuit 00: T*2 01: T*4 10: T*8 11: T*16

3.4 Design circuit

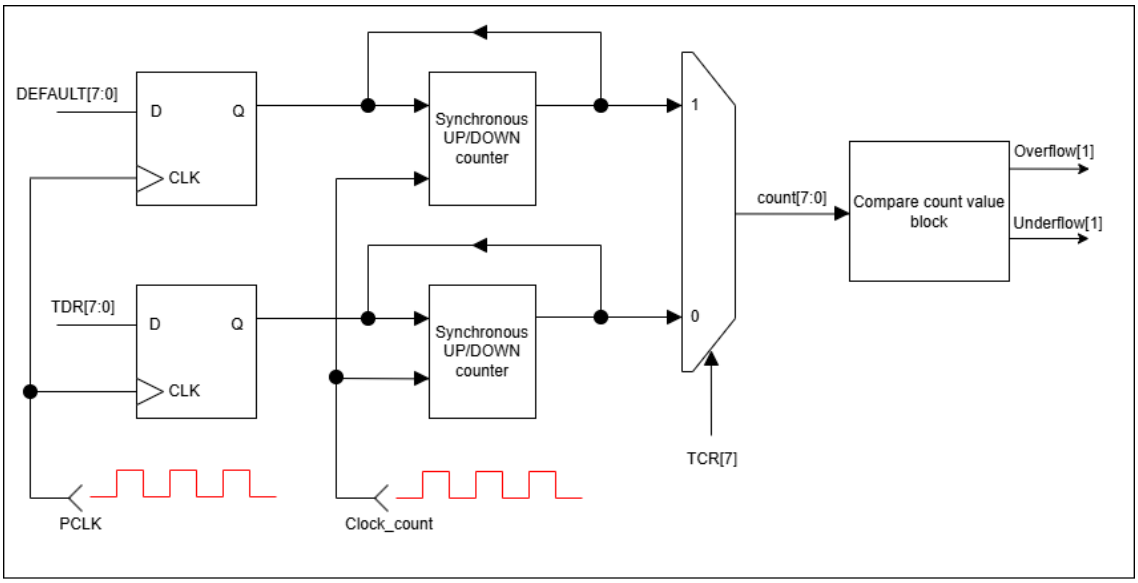

Figure 3-2: Timer counter circuit diagram

3.5 Timing chart

The below timing charts show the operation for 2 modes in bit 7 of the register TCR. The counting order is increasing in this example.

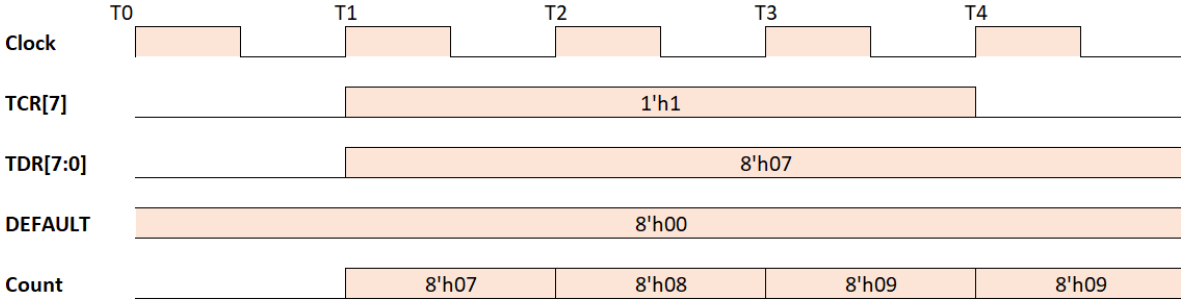

Figure 3-3: Operation when loading data from the TDR register to the TCNT

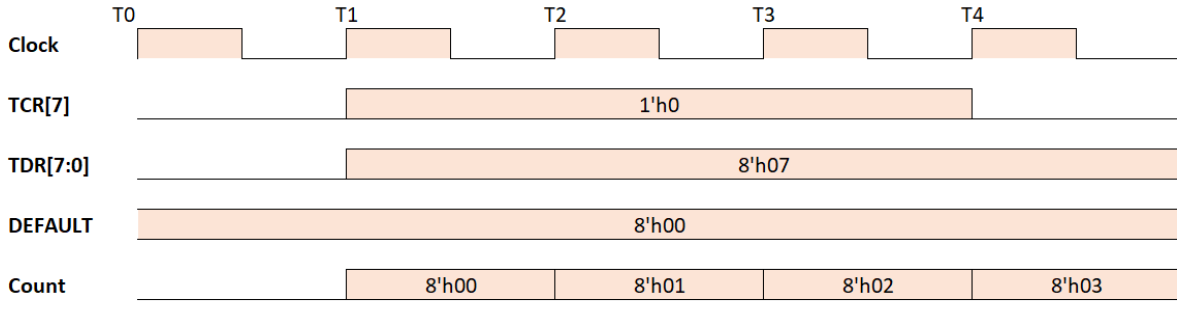

Figure 3-4: Operation of TCNT when counting from the default value

4. Control logic

4.1 Block diagram

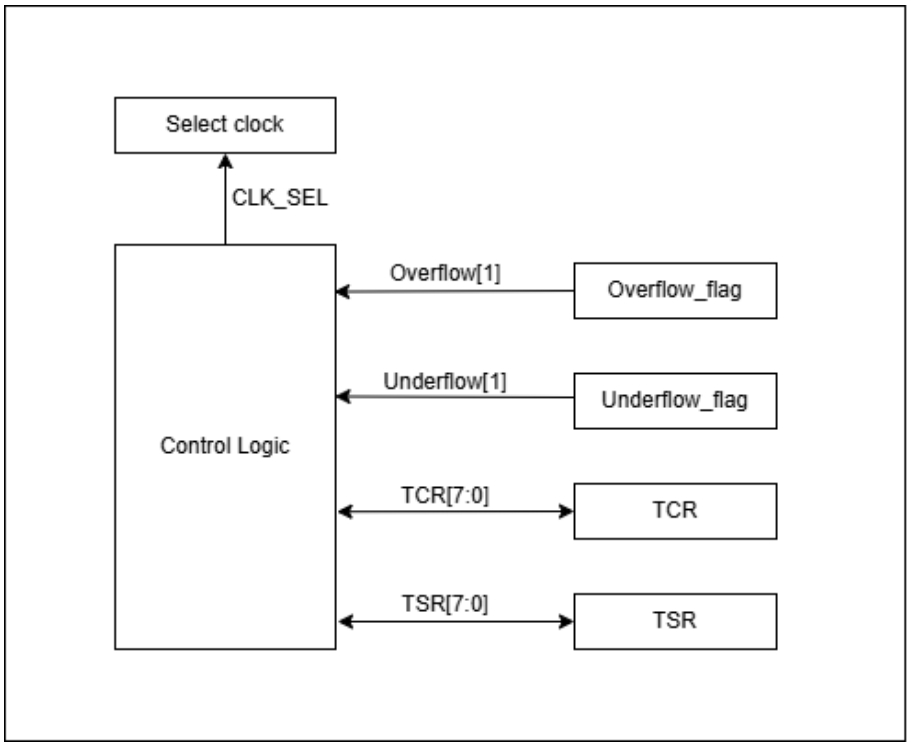

Figure 4-1: The Control logic block diagram

4.2 Input/Outputs pin

Pin name	Bit width	I/O	Function
Overflow	1 bit	Input	The signal represents the Overflow state.
Underflow	1 bit	Input	The signal represents the Underflow state.
TCR	8 bits	Input/Output	TCR selects the clock source and the time TCNT is cleared and controls interrupts.
TSR	8 bits	Input/Output	TSR displays status flags and controls to compare match output.
CLK_SEL	2 bits	Output	Select internal clocks for the circuit 00: T*2 01: T*4 10: T*8 11: T*16

4.3 Functional/Protocol

The Control logic will handle these bellow actions:

- Receive Overflow or Underflow signal from the TCNT and set the status bits 1 and 0 on the TSR register.
- Receive bits Cks[1:0] from the TCR register and decide which frequency will be used for the internal clock in the TCNT. The clock pulse selected will be transmitted through the CLK_SEL signal.

4.4 Timing chart

The below timing chart shows the operation of the Control logic when Overflow/Underflow happens.

The third chart shows the output of the Control logic when the Cks[1:0] is sent, and the following output in CLK_SEL[1:0] signal.

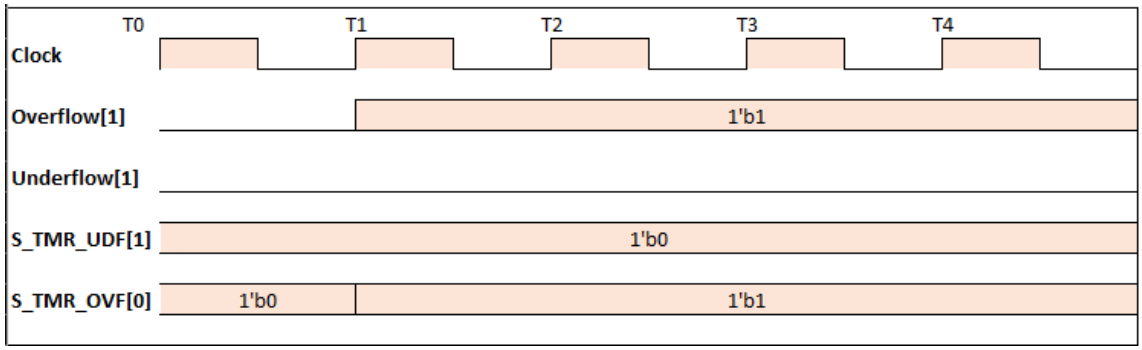

Figure 4-2: The Control logic timing chart when the Overflow flag is raised.

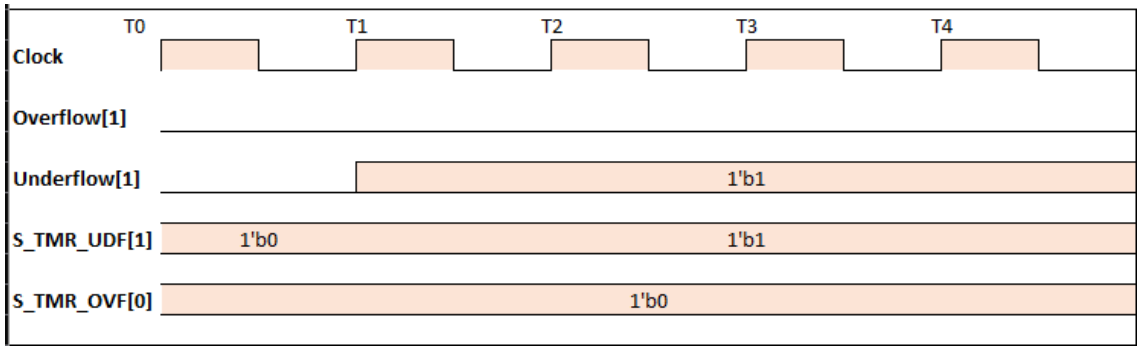

Figure 4-3: The Control logic timing chart when the Overflow flag is raised.

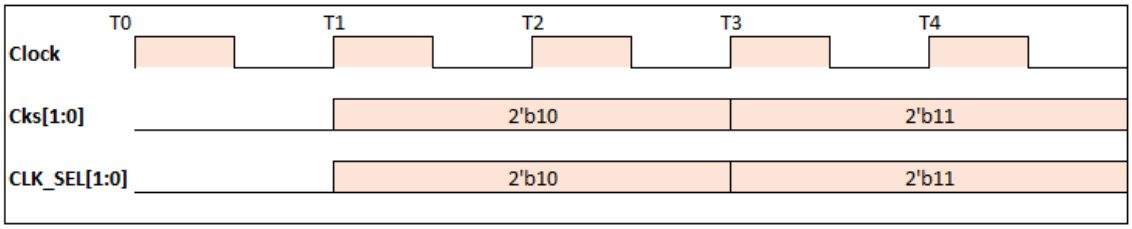

Figure 4-4: The Control logic output signal when Cks[1:0] is sent.

5. Clock select

5.1 Block diagram

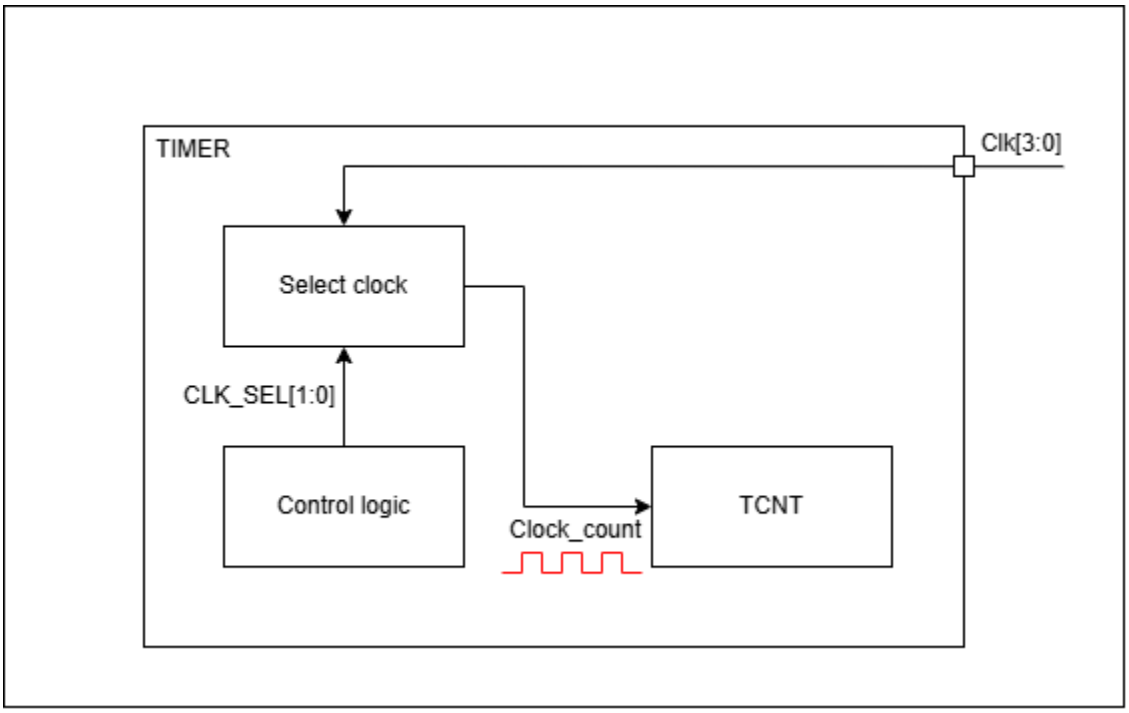

Figure 5-1: The Clock select block diagram.

5.2 Input/Output pins

Pin name	Bit width	I/O	Function
Clk[3:0]	4 bits	Input	The clock source for the counter timer. Each clock has a different frequency.
Clock_count	1 bit	Output	Clock pulse selected for the TCNT.

5.3 Functional/Protocol

The control logic receives the desired clock frequency from bit 1 and bit 0 of the TCR register. The select signal CLK_SEL[1:0] sent from the Control logic will inform the Select clock block which frequency is appropriated. Output signal from the mux have to go through a Rising edge detector then the Clock_count signal will be sent to the Timer Counter for flip-flop usage.

5.4 Design circuit

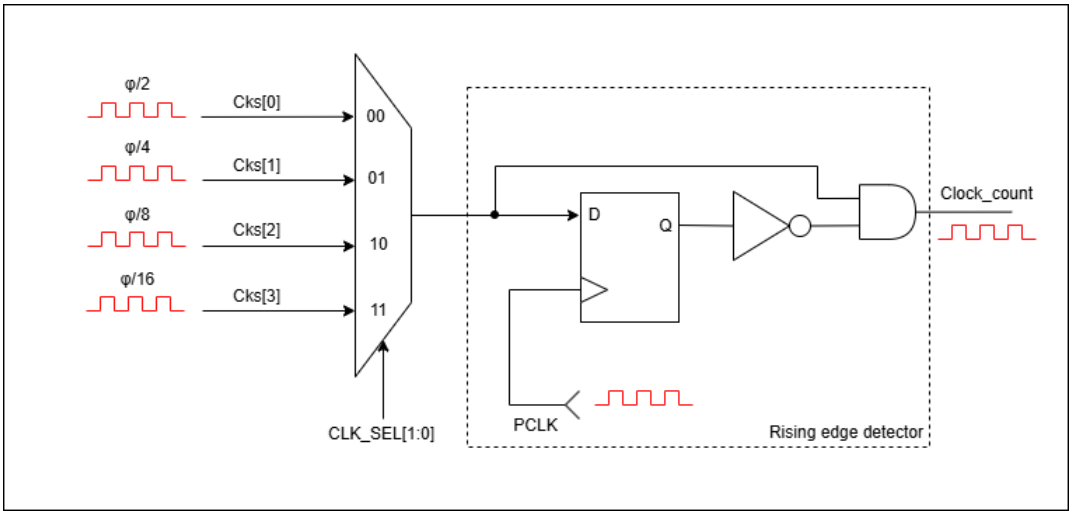

Figure 5-2: The Clock select circuit diagram.

5.5 Timing chart

The timing chart below shows when the CLK_SEL signal was sent from the Control logic, leading to the output signal Clock_count.

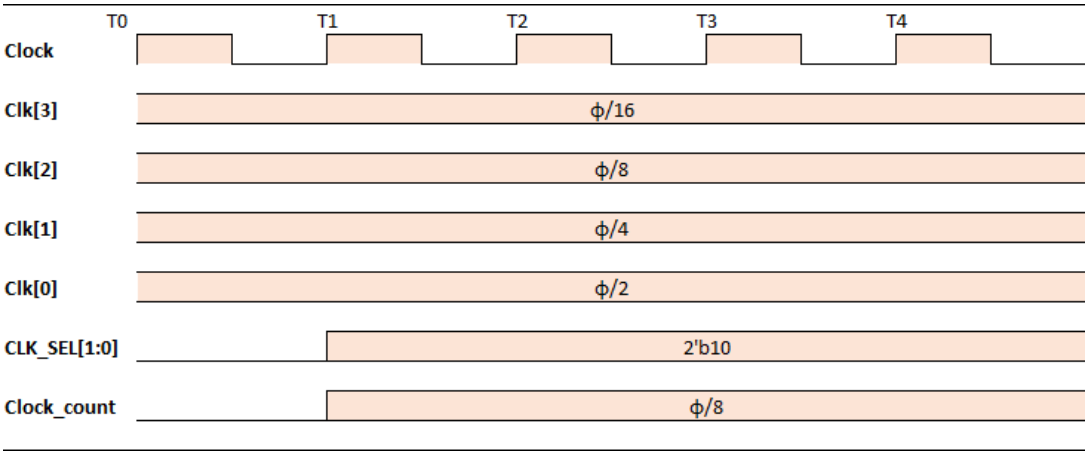

Figure 5-3: Timing chart of the Clock selected when CLK_SEL data is 2’b10.

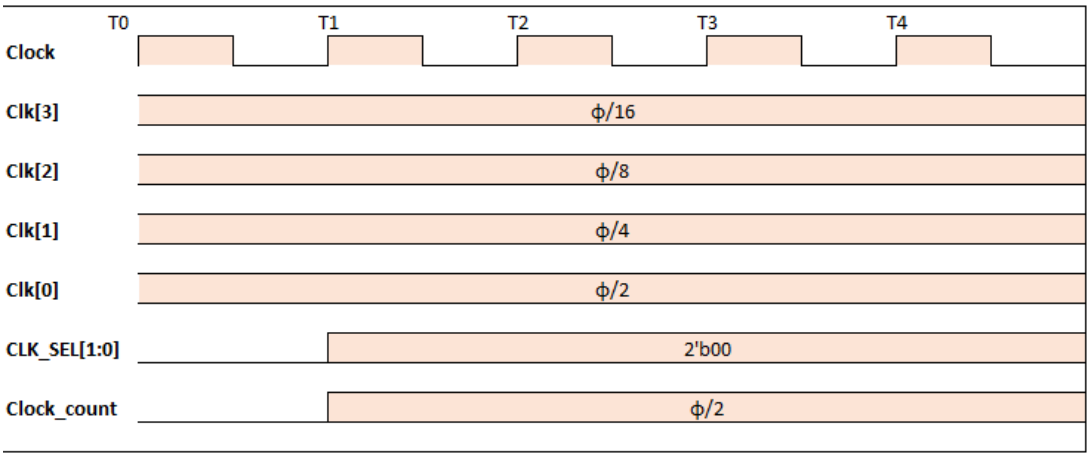

Figure 5-4: Timing chart of the Clock selected when CLK_SEL data is 2’b00.

6. Overflosw/Underflow comparison

6.1 Input/Outputs pin

Pin name	Bit width	I/O	Function
Count[7:0]	4 bits	Input	The current counting value from the TCNT, arranges from 8'h00 to 8'hFF.
Overflow[1]	1 bit	Output	Output signal sent to the Control logic when the Overflow happens.
Underfow[1]	1 bit	Output	Output signal sent to the Control logic when the Underflow happens

6.2 Block diagram

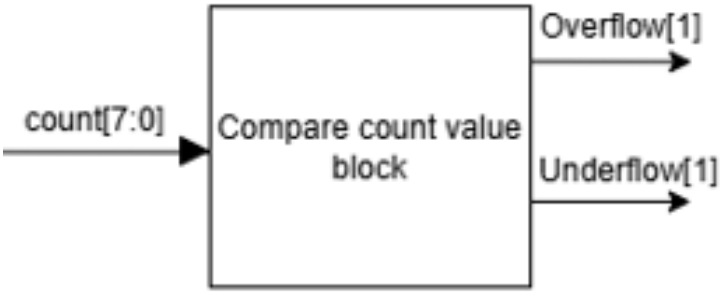

Figure 6-1: Compare count value block diagram.

6.3 Functional/Protocol

The compare count value block receives the count[7:0] signal from the TCNT and sends the status signal to the Control logic if either Overflow or Underflow happens during the counting section.

6.4 Timing chart

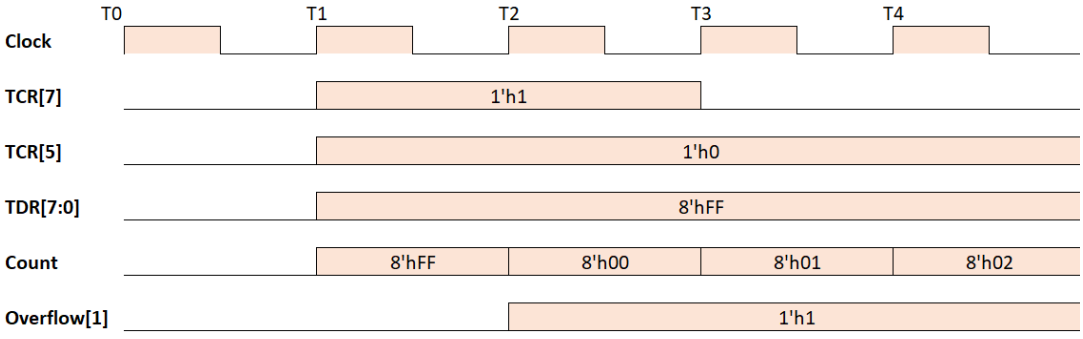

Figure 6-2: TCNT timing chart when the Compare block raised the Overflow flag.

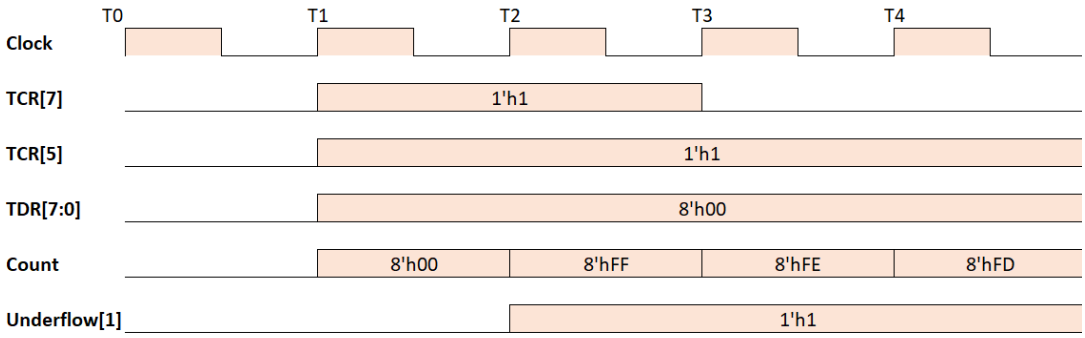

Figure 6-3: TCNT timing chart when the Compare block raised the Underflow flag.