ECE 100 (Spring 2021) - Final

(Format: 7 questions, 3 hours)

Name: _____

Student ID: _____

Score: _____ out of 100

Instructions:

1. Register for the Final exam (if you are seeing this, you are already registered)
2. Once you register for the Final exam, you will have 3 hours to complete the final.
3. Please use blank paper (or tablet) for your solutions. Clearly label the page # on each page and make it clear which Problem you are working on. Remember to box your answers to make it easier for us to grade.
4. After the final, you have 15 minutes to submit and upload your Final to CCLE (under "Final → Final Exam Submission").
5. Please fill out this 'End-of-Final' survey to acknowledge that you have completed the Final and submitted your answer sheet to CCLE: https://forms.gle/ArPhmsXJpdpo6swS8
6. Note the total points for this exam is 105, but 5 points will be bonus points. We will normalize to 30% of your grade.
7. If you do extremely well (>80%) you will receive a minimum grade of A^- no matter what your quarter grade is.
8. If you have submitted your course evaluation, please say so explicitly at the top of your exam (Bruin honor), you will get an additional 1 point bonus.
9. There are 16 pages in this exam. Please tell us how many pages you have in your answer PDF file on the first page. Number all your pages and make sure they are ordered and scanned legibly.

Rules:

- The final is a closed book. No computers, cell phones, etc.
- 1-page cheat sheet
- Scientific calculator allowed.
- Box all of your answers & show your work. Neat work will help us give you the benefit of doubt.
- **If you have questions on the exam, please DO NOT post on Piazza. Email instructor(s) directly.**

Final Exam Start Time:

Wednesday, June 9th @ 6:00am PDT

Note: Once you register for the Final, you will have 3h 15m to complete & upload your results. (3 hours to take the exam, 15 minutes to upload).

Final Exam End Time:

Thursday, June 10th @ 5:59am PDT (answer sheet must be submitted by this time)

No late submissions

<u>Problem 1: Course Fundamentals</u> (20 points - 2 points per question)
Answer the following ten questions, which test your conceptual understanding of what we have learned in class.

(a) Ohm's law relates the current, I, through a resistor, R, with the voltage across the resistor. What is the power dissipated through the resistor in terms of I & R?

(b) In the SI system of units, we have base quantities such as length (L), mass (kg) and time (s) – there are seven base quantities. Which of the following is the electrical base quantity? *(circle one)*

(i) Volts
(ii) Coulombs
(iii) Amperes
(iv) Hertz

(c) We introduced the concept of impedance ($Z = R + jX$), which is a complex quantity. What is the analog of Ohm's law using complex impedance?

(d) What do we mean by phasors? Consider a voltage phasor, $\mathbf{V}$, (phase= $0°$) applied to an impedance Z, (Z = R + jX). What is the current, $\mathbf{I}$, in Phasor form? What is the power, $\mathbf{P}$, expended by the voltage source? What is the meaning of the imaginary component of the power?

(e) Electrical engineering has perhaps one of the more abstract formulations of any branch of engineering. We can't see voltage but we can feel it when we get an electric shock! Trust me, it's very real. A commonly used mechanical analogy is water flow in a pipe. Using this analogy, what are the analogues of voltage, current, resistance and capacitance. Here is the difficult one – is there an analogue of inductance? If so, what is it?

(f) The continuity equation in most fields of engineering states that if there is no source of matter, the mass flux entering a system must equal the mass flux leaving the system. What is the electrical analog of the continuity equation?

(g) Similarly, energy conservation is a thermodynamic requirement. What electrical engineering law reflects energy conservation?

(h) Why are resistors, capacitors, and inductors linear components, but a diode or transistor is not?

(i) Way back Charles Babbage proposed computation based on mechanical computers – a complex machine with all kinds of gears and such. They did not make a big impact. What distinguishes electronic computers that mechanical computers did not possess.

(j) When you shine light on a semiconductor you can increase the conductivity of the semiconductor a 1000-fold through the generation of free carriers by the light. This effect is used in stores to indicate that someone has entered the store. Draw a simple circuit to do this function.

<u>Problem 2: Zero- order circuits</u> (10 points)
Consider a non-ideal voltage source, V, with an internal resistance, R_{int}.

(a) What is the schematic representation of this voltage source?

(b) If you do a source transformation to a current source what would the circuit representation be? What would the value of the current source be?

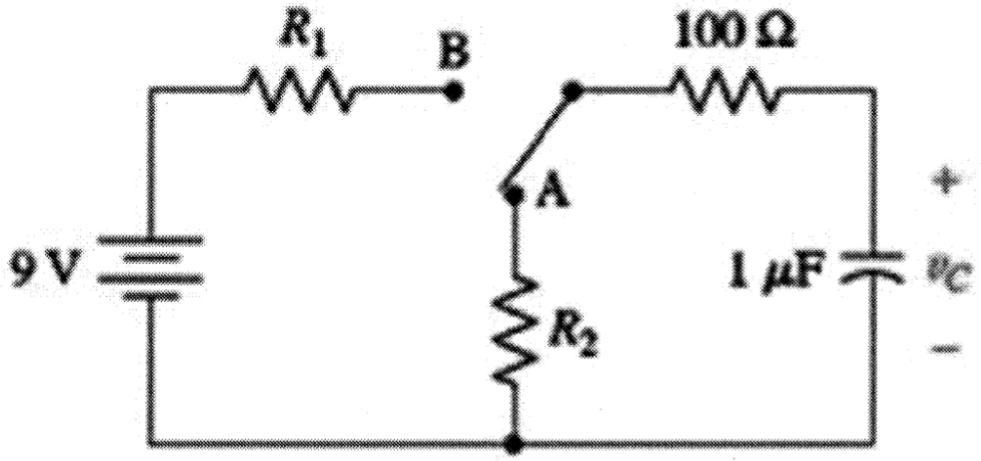
(c) Now reconsider the non-ideal voltage source and let it drive a load resistor R_L. You will use a zero-order differential equation (which is really a linear equation) to solve this circuit. What is the power dissipated in the load resistor, R_L?

(d) At what value of R_L is the power dissipated in the load maximum? (Express in terms of R_{int}).

(e) Is this true when you use the equivalent current source?

<u>Problem 3: First-order circuits</u> (10 points)

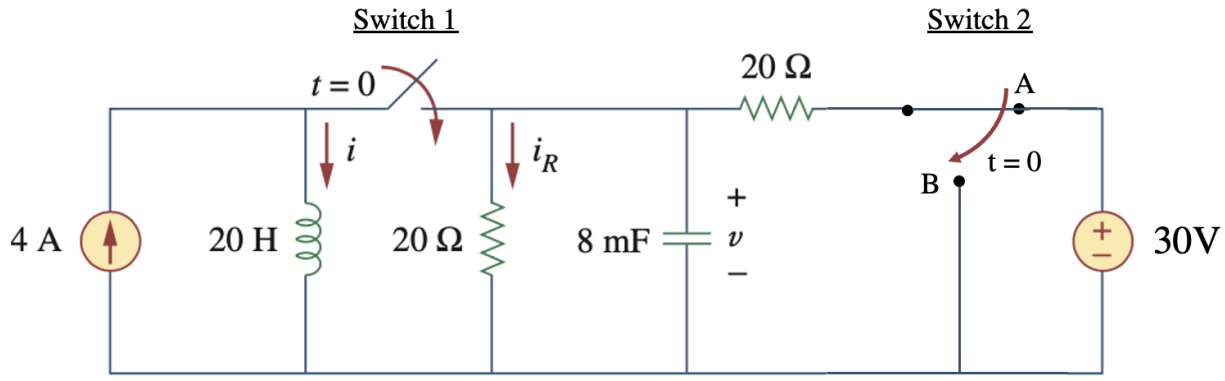
The switch has been in position A for a long time. At t=0ms, the switch is moved to position B, and at t=1ms, the switch is moved back to position A. Determine the values of R_1 and R_2 such that $V_c(t = 1ms) = 8V$ and $V_c(t = 2ms) = 1V$. Why is this a first order circuit?



Hint: First consider the circuit from $0 < t \leq 1ms$ *and then consider the circuit for* $t > 1ms$.

Problem 4: 2nd-order circuits (15 points)

Consider the circuit below. Note that there are two switches in this circuit. At t=0, Switch 1 is closed. For Switch 2, it is initially connected to Point A. At t=0, Switch 2 is moved from Point A to Point B.



(a) What characterizes 2nd order circuits? Why is the above circuit a 2nd order circuit?

(b) Draw the equivalent circuits for (i) $t < 0$and (ii)$t \geq 0$.

(c) Using KCL, write the second order differential equation for the circuit above ($t \geq 0$) in terms of current variable, i.

Recall: $\frac{d^2x(t)}{dt^2} + 2\zeta\omega_o\frac{dx(t)}{dt} + \omega_o^{\ 2} = f(t)$

(d) Solve for the initial conditions of the inductor and capacitor:
$i(t = 0^+)$, $v(t = 0^+)$.

(e) Solve for the damping factor (ζ) and the resonant frequency (ω_o).

(f) Is this system underdamped, overdamped, or critically damped?

(g) Solve for the characteristic roots: s_1 and s_2.

(h) Solve for $i(t)$.

(i) Solve for the current across the resistor, $i_R(t)$.

Hint: remember that the voltage across the inductor, capacitor, and resistor are the same voltage ($v_L = v_C = v_R = v$).

(j) Quickly sketch the voltage across capacitor as a function of time, $v(t)$.

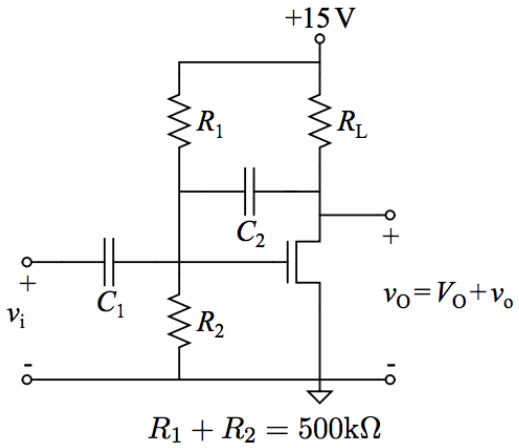
Problem 5: MOSFET amplifier (15 points)

Consider an NMOS FET used as an amplifier as shown in figure below. The capacitor C_1 couples the incremental input voltage v_i to the gate. Because it is an open circuit for DC, v_i does not affect V_{GS}, the operating point value of the gate-to source voltage. The FET is described by

$$i_D = 0 \text{ for } v_{GS} < V_T$$

$$i_D = K(v_{GS} - V_T)^2 \text{ for } v_{GS} > V_T \text{ and } v_{DS} > (v_{GS} - V_T)$$

$$K = 0.2\ \frac{mA}{V^2},\ V_T = 2\ V$$



(a) Determine V_{GS} and R_L such that the operating (quiescent) point of the amplifier is: V_O = 7 V, I_D = 0.2 mA

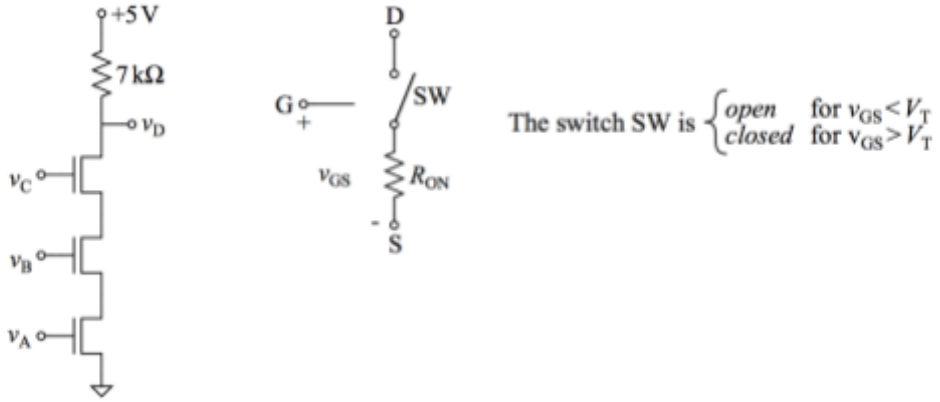
(b) Determine the transconductance g_m of the FET at the operating point defined in part (a).

(c) Given that $R_1 + R_2 = 500k\Omega$, determine R_1 and R_2 such that the desired DC voltage, V_{GS} is established.

(d) Using the small-signal model for the FET, sketch and label a complete small-signal equivalent model of the original circuit.

<u>Problem 6: MOS logic</u> (15 points)

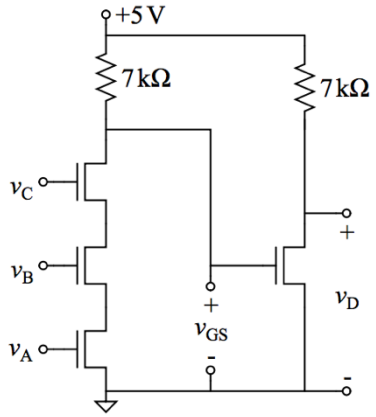
Consider the circuit shown below with three NMOS transistors. Assume that a logical one corresponds to voltage, $v > 4$ volts and a logical zero corresponds to $v < 1$ volt. The switch-resistor model for the FET is shown alongside.



(a) Write a logic expression or describe the logic function implemented by the above circuit. You may consider using a Boolean expression (Output node is v_D).

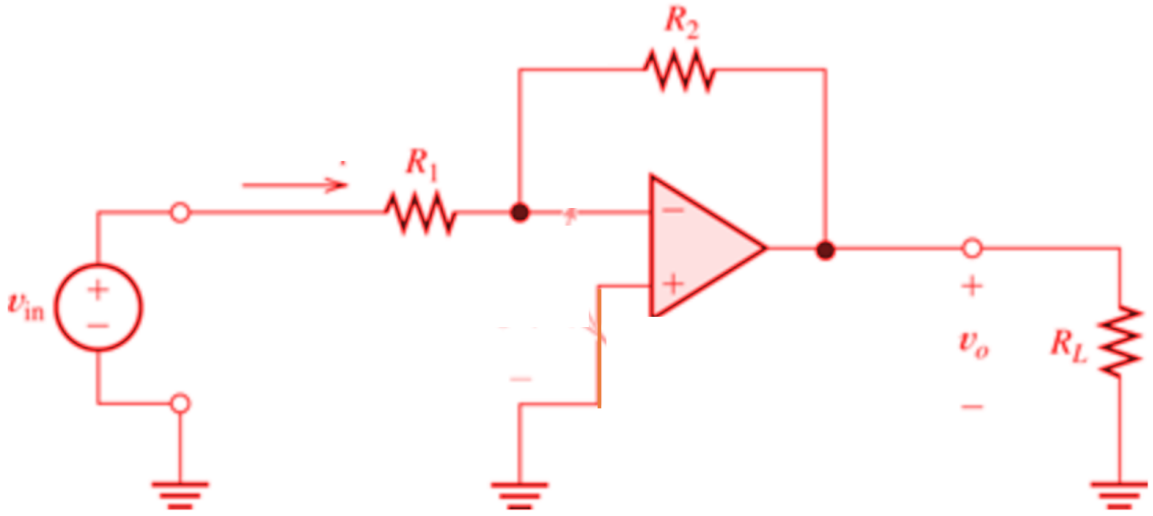
(b) Using a switch-resistor model (R_{ON} = 1kΩ, V_T = 1V) for each FET, determine the output voltage v_D when $v_A = v_B = v_C = 5V$.

(c) The output of the above circuit is connected to a FET inverter as shown below. Will this implement an ‘AND’ logic operation? If not, why? (R_{ON}=1kΩ, V_T=1V)



Problem 7: Operational Amplifiers (20 points)

Consider the op-amp circuit shown in the schematic shown below.



(a) Analyze the circuit shown and derive the output voltage in terms of the input voltage. Indicate where the virtual short (or virtual ground). What are the assumptions on the op-amp Voltage gain, A_V? What should be the relationship between R_1, R_2, and R_L be to get a voltage gain A_V=-5. What are the constraints on R_L?

(b) How would you convert the circuit in (a) to an 'integrator'? (draw the new circuit)

You may consider swapping R_1 or R_2 for a different component.

(c) How would you convert the circuit in (a) to a ‘differentiator’? (draw the new circuit)
You may consider swapping R_1 or R_2 for a different component.

(d) How would you modify the circuit in (a) to do a summation of three input voltages? (draw the new circuit)

(e) Explain qualitatively (with a block diagram) how you would build a PID controller with Op-Amps.
Hint: “PID” = proportional-integral-derivative controller