**ECE 100 (Spring 2021) - Homework #7**

**<u>Due Date:</u>** Sunday, May 16th @ 11:59pm PDT
**Recommended Readings:** 6.2-6.5, 9.1-9.7, 11.1-11.2

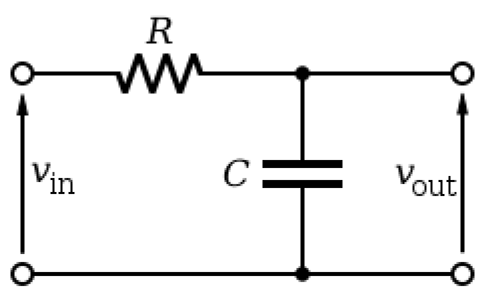
***Problems highlighted in blue are optional but included for extra practice***

**Required problems: 1, 2, 3, 5, 10, 13, 14, 16, 19**

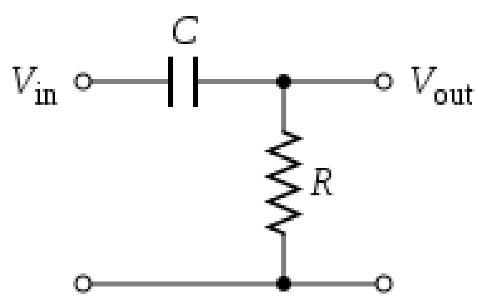
**<u>Problem 1 (10 points)</u>**

(a) Draw the expected frequency response of each of the following: *(i) low-pass, (ii) high-pass, (iii) band-pass, and (iv) band-stop filters.*

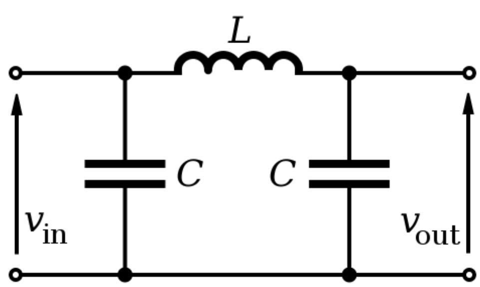
*For (b)-(g), indicate whether the circuit is a low-pass, high-pass, band-pass, or band-reject (also known as band-stop) filter.*



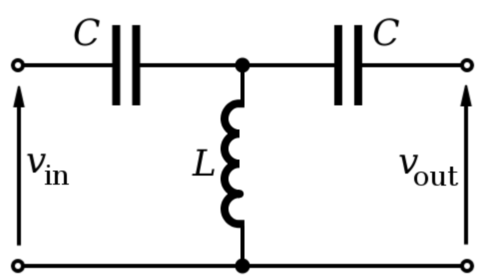

(b)




(c)




(d)

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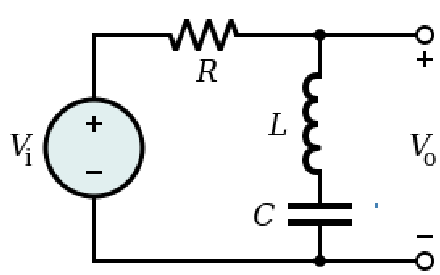
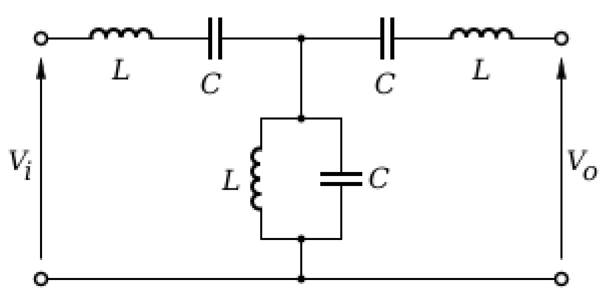


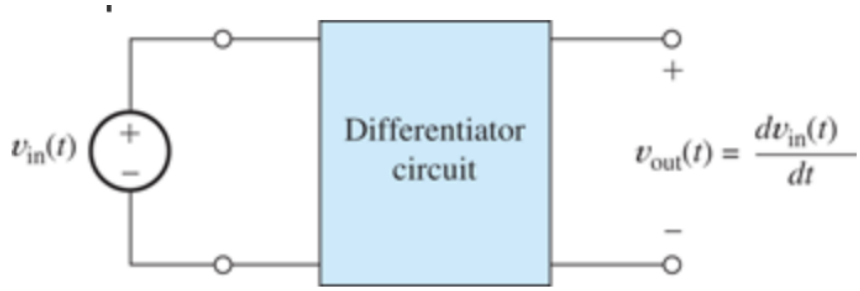

(f)




(g)

## Problem 2 (10 points)

**P6.20.** Suppose we have a circuit for which the output voltage is the time derivative of the input voltage, as illustrated in **Figure P6.20**. For an input voltage given by $v_{\text{in}}(t) = V_{\max}\cos(2\pi f t)$, find an expression for the output voltage as a function of time. Then, find an expression for the transfer function of the differentiator. Plot the magnitude and phase of the transfer function versus frequency.

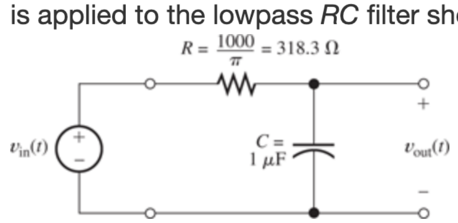



## Problem 3 (10 points)

***P6.25.** An input signal given by

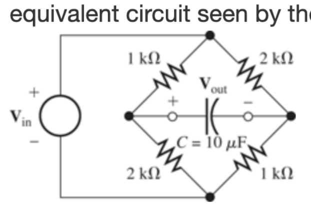
$$v_{\text{in}}(t) = 5\cos(500\pi t) + 5\cos(1000\pi t) + 5\cos(2000\pi t)$$

is applied to the lowpass *RC* filter shown in **Figure P6.25**. Find an expression for the output signal.



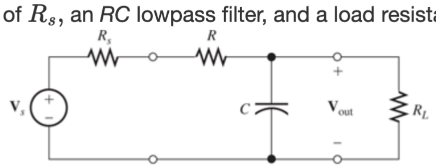

## *Problem 4 (optional)*

***P6.30.** Sketch the magnitude of the transfer function $H(f) = \mathbf{V}_{\text{out}}/\mathbf{V}_{\text{in}}$ to scale versus frequency for the circuit shown in **Figure P6.30**. What is the value of the half-power frequency? [*Hint:* Start by finding the Thévenin equivalent circuit seen by the capacitance.]

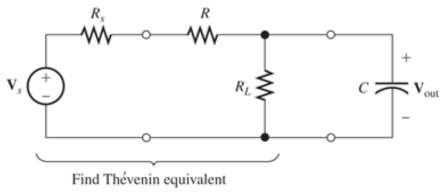


## Problem 5 (20 points)

**P6.32.** Consider the circuit shown in **Figure P6.32(a)**. This circuit consists of a source having an internal resistance of $R_s$, an *RC* lowpass filter, and a load resistance $R_L$.



(a)



(b)

a. Show that the transfer function of this circuit is given by

$$H(f) = \frac{\mathbf{V}_{out}}{\mathbf{V}_s} = \frac{R_L}{R_s + R + R_L} \times \frac{1}{1 + j(f/f_B)}$$

in which the half-power frequency $f_B$ is given by

$$f_B = \frac{1}{2\pi R_t C} \quad \text{where} \quad R_t = \frac{R_L\ (R_s + R)}{R_L + R_s + R}$$

Notice that $R_t$ is the parallel combination of $R_L$ and $(R_s + R)$. [*Hint:* One way to make this problem easier is to rearrange the circuit as shown in **Figure P6.32(b)** and then to find the Thévenin equivalent for the source and resistances.]

b. Given that $C = 0.2\ \mu\text{F},\ R_s = 2\ \text{k}\Omega,\ R = 47\ \text{k}\Omega$, and $R_L = 1\ \text{k}\Omega$, sketch (or use MATLAB to plot) the magnitude of *H*(*f*) to scale versus $f/f_B$ from 0 to 3.

## Problem 6 (optional)

***P6.46.** Two first-order lowpass filters are in cascade as shown in **Figure P6.46**. The transfer functions are

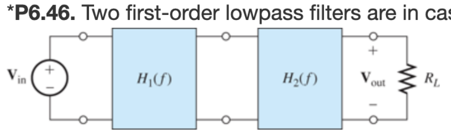



**Figure P6.46**

$$H_1(f) = H_2(f) = \frac{1}{1 + j(f/f_B)}$$

a. Write an expression for the overall transfer function.
b. Find an expression for the half-power frequency for the overall transfer function in terms of $f_B$.

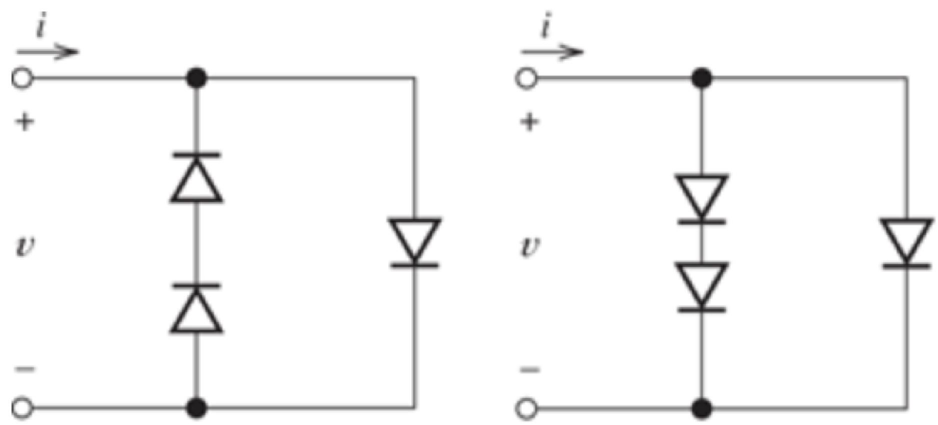
[Comment: This filter cannot be implemented by cascading two simple *RC* lowpass filters like the one shown in **Figure 6.7** on page **296** because the transfer function of the first circuit is changed when the second is connected. Instead, a buffer amplifier, such as the voltage follower discussed in **Section 14.3**, must be inserted between the *RC* filters.]

## Problem 7 (optional)

**P6.67.** Suppose we need a first-order highpass filter (such as **Figure 6.19** on page **309**) to attenuate a 60-Hz input component by 60 dB. What value is required for the break frequency of the filter? By how many dB is the 600-Hz component attenuated by this filter? If $R = 5\ \mathrm{k}\Omega$, what is the value of *C*?

## Problem 8 (optional)

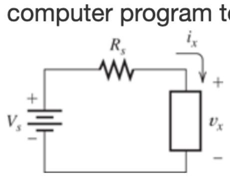
Sketch i vs v for the following circuits. Assume voltages of 0.6V for all diodes when current flows in the forward direction.




(a) (b)

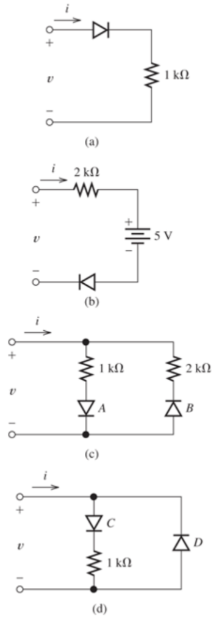
## Problem 9 (optional)

***P9.16.** The nonlinear circuit element shown in **Figure P9.16** has $i_x = [\exp(v_x) - 1]/10$. Also, we have $V_s = 3\ \mathrm{V}$ and $R_s = 1\ \Omega$. Use graphical load-line techniques to solve for $i_x$ and $v_x$. (You may prefer to use a computer program to plot the characteristic and the load line.)



## Problem 10 (10 points)

**P9.39.** Sketch *i* versus *v* to scale for each of the circuits shown in **Figure P9.39**. Assume that the diodes are ideal and allow *v* to range from $-10$ V to $+10$ V.




## Problem 11 (optional)

**P9.49.** Draw the circuit diagram of a half-wave rectifier for producing a nearly steady dc voltage from an ac source. Draw two different full-wave circuits.

## Problem 12 (optional)

**P9.52.** Consider the half-wave rectifier shown in **Figure 9.26** on page **477**. The ac source has an rms value of 20 V and a frequency of 60 Hz. The diodes are ideal, and the capacitance is very large, so the ripple voltage $V_r$ is very small. The load is a $100\text{-}\Omega$ resistance. Determine the PIV across the diode and the charge that passes through the diode per cycle.

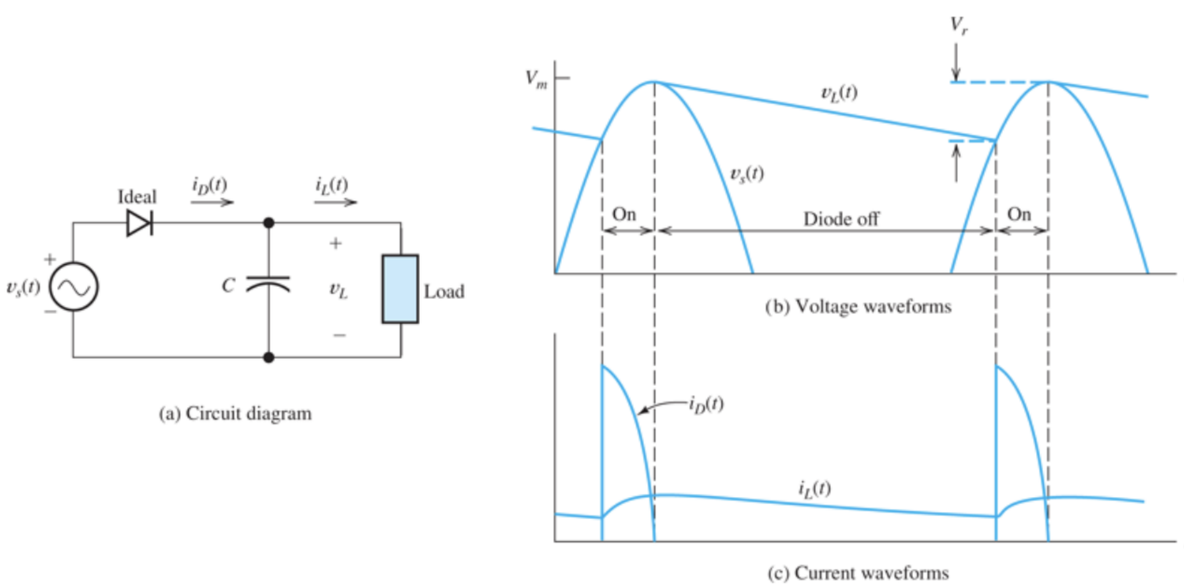



**Figure 9.26**

Half-wave rectifier with smoothing capacitor.

## Problem 13 (10 points)

***P9.54.** Design a half-wave rectifier power supply to deliver an average voltage of 9 V with a peak-to-peak ripple of 2 V to a load. The average load current is 100 mA. Assume that ideal diodes and 60-Hz ac voltage sources of any amplitudes needed are available. Draw the circuit diagram for your design. Specify the values of all components used.

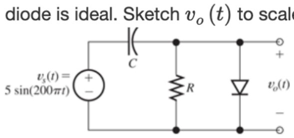
**P9.55.** Repeat Problem P9.54 with a full-wave bridge rectifier.

**P9.56.** Repeat Problem P9.54 with two diodes and out-of-phase voltage sources to form a full-wave rectifier.

**P9.57.** Repeat Problem P9.54, assuming that the diodes have forward drops of 0.8 V.

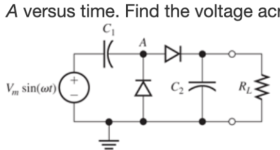
## Problem 14 (10 points)

**P9.69.** Consider the circuit shown in Figure P9.69, in which the *RC* time constant is very long compared with the period of the input and in which the diode is ideal. Sketch $v_o(t)$ to scale versus time.



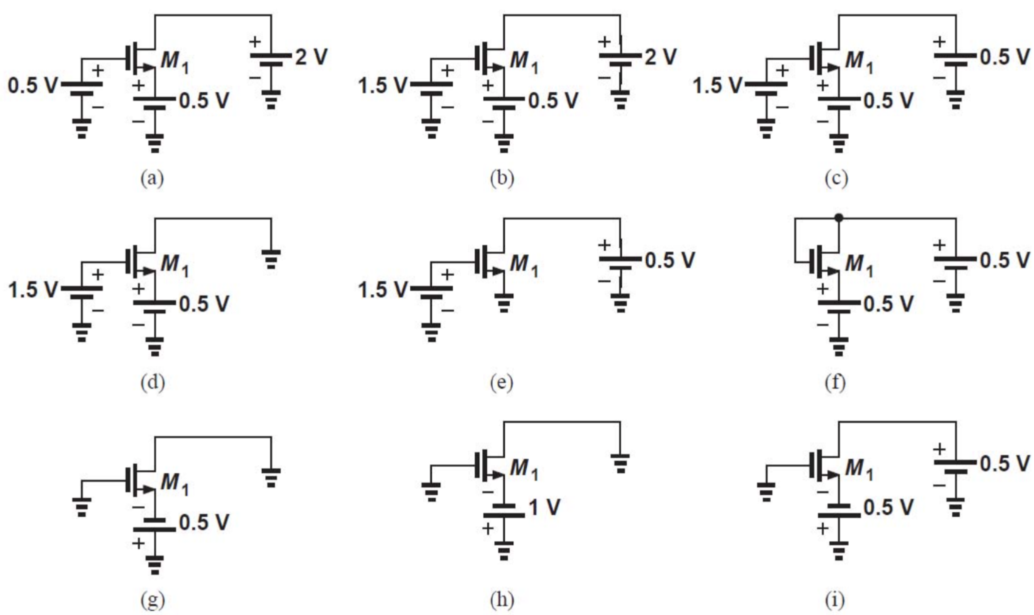

## *Problem 15 (optional)*

**P9.71. Voltage-doubler circuit.** Consider the circuit of Figure P9.71. The capacitors are very large, so they discharge only a very small amount per cycle. (Thus, no ac voltage appears across the capacitors, and the ac input plus the dc voltage of $C_1$ must appear at point *A*.) Sketch the voltage at point *A* versus time. Find the voltage across the load. Why is this called a voltage doubler? What is the PIV across each diode?



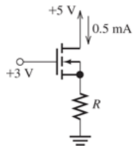

## Problem 16 (10 points)

**MOSFET as a Resistor**: If the threshold is equal to 0.7 V, for each circuit determine whether the device is off or acts as a resistor or neither:



## Problem 17 (optional)

**P11.14.**Given that the enhancement transistor shown in **Figure P11.14** has $V_{to} = 1\ \mathrm{V}$ and $K = 0.5\ \mathrm{mA/V^2}$, find the value of the resistance *R*.




## Problem 18 (optional)

***P11.19.** Consider the circuit shown in **Figure 11.10** on page **567**. The transistor characteristics are shown in **Figure 11.11**. Suppose that $V_{GG}$ is changed to 0 V. Determine the values of $V_{DSQ}$, $V_{DS\min}$, and $V_{DS\max}$. Find the gain of the amplifier.

## Problem 19 (10 points)

**P11.20.** Consider the amplifier shown in **Figure P11.20**.

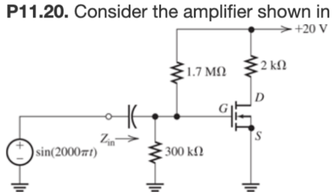



**Figure P11.20**

a. Find $v_{GS}(t)$, assuming that the coupling capacitor is a short circuit for the ac signal and an open circuit for dc. [*Hint:* Apply the superposition principle for the ac and dc sources.]
b. If the FET has $V_{to} = 1\ \mathrm{V}$ and $K =$ sketch its drain characteristics to scale for $v_{GS} = 1, 2, 3,$ and 4 V.
c. Draw the load line for the amplifier on the characteristics.
d. Find the values of $V_{DSQ}$, $V_{DS\min}$, and $V_{DS\max}$.

## Problem 20 (optional)

**P11.22.** Use a load-line analysis of the circuit shown in **Figure P11.22** to determine the values of $V_{DSQ}$, $V_{DS\ \min}$, and $V_{DS\ \max}$. The characteristics of the FET are shown in **Figure 11.21** on page **576**. [*Hint:* First, replace the 15-V source and the resistances by their Thévenin equivalent circuit.]