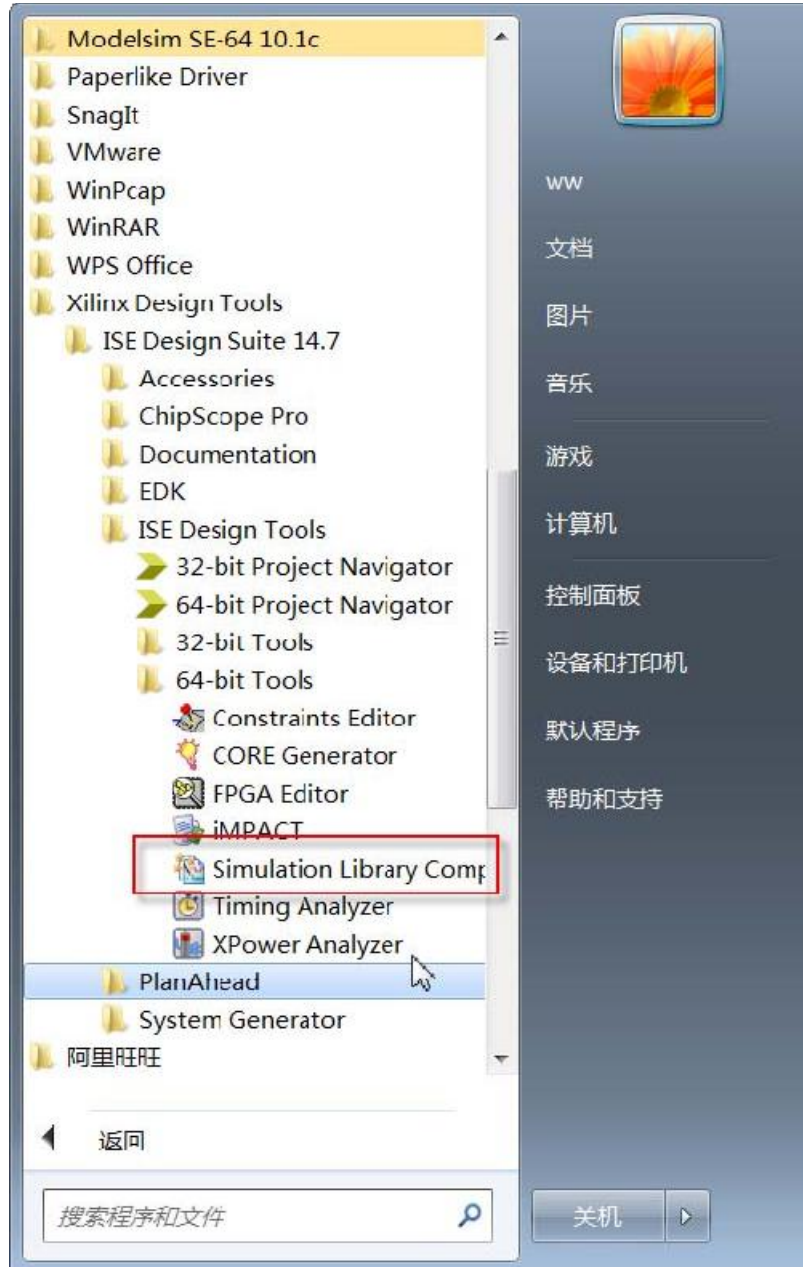


## ISE association Modelsim settings

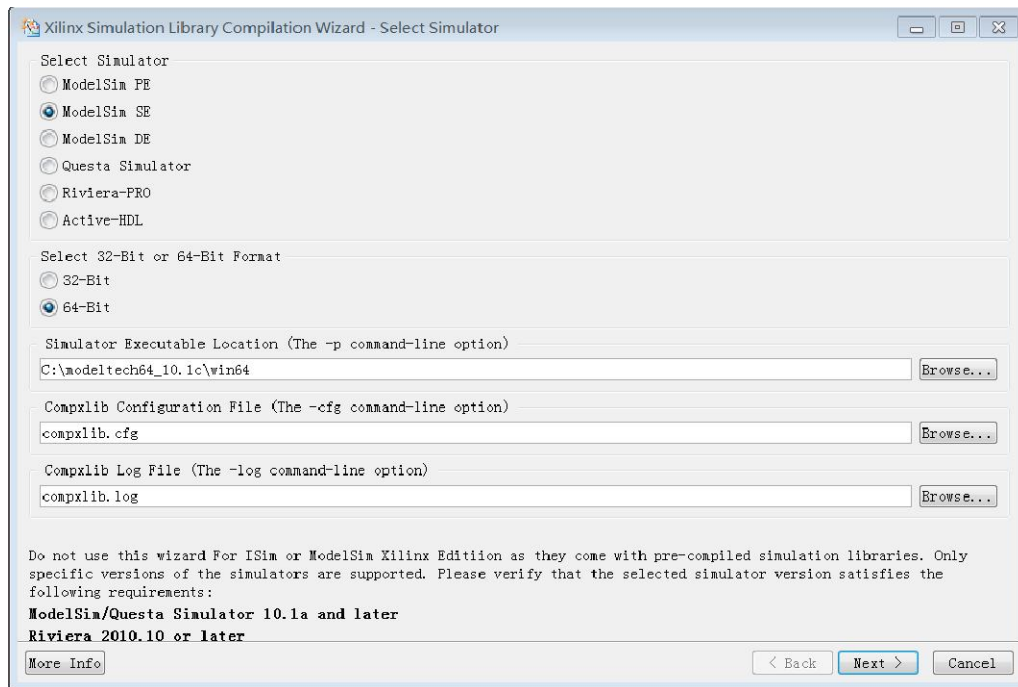
1. First generate the ISE simulation library file. In the Start menu, find the "Xilinx Design Tools-> ISE Design Suite 14.7->ISE Design Tools->64-bit Tools->Simulation Library Complication Wizard" option. Click to open



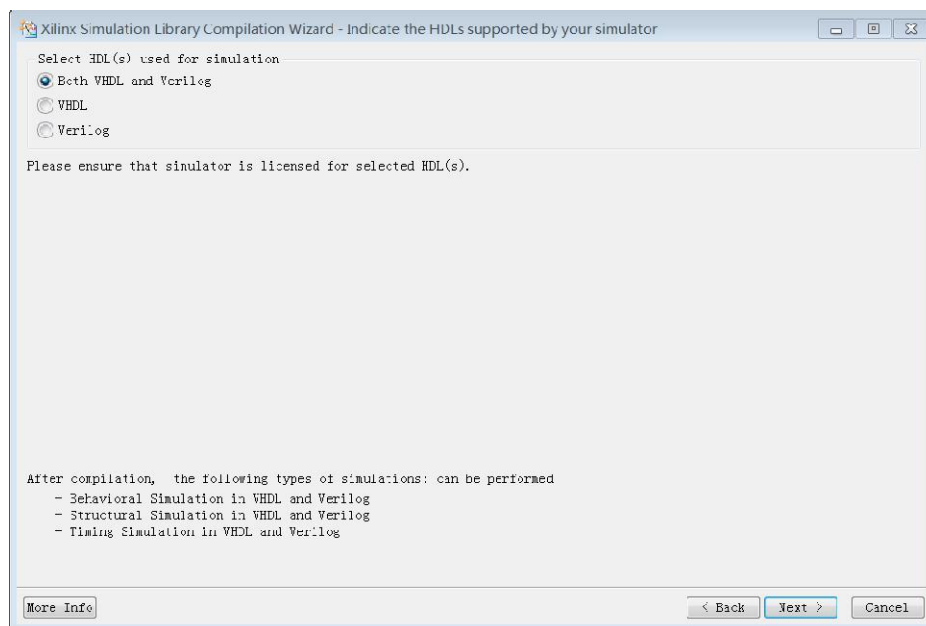
2. Select the Modelsim version as shown below, and we choose Modelsim SE here. Fill in the text of Modelsim.exe under "Simulator Executable Location"

3. Folder, click "Browse..." button, add, our Modelsim SE

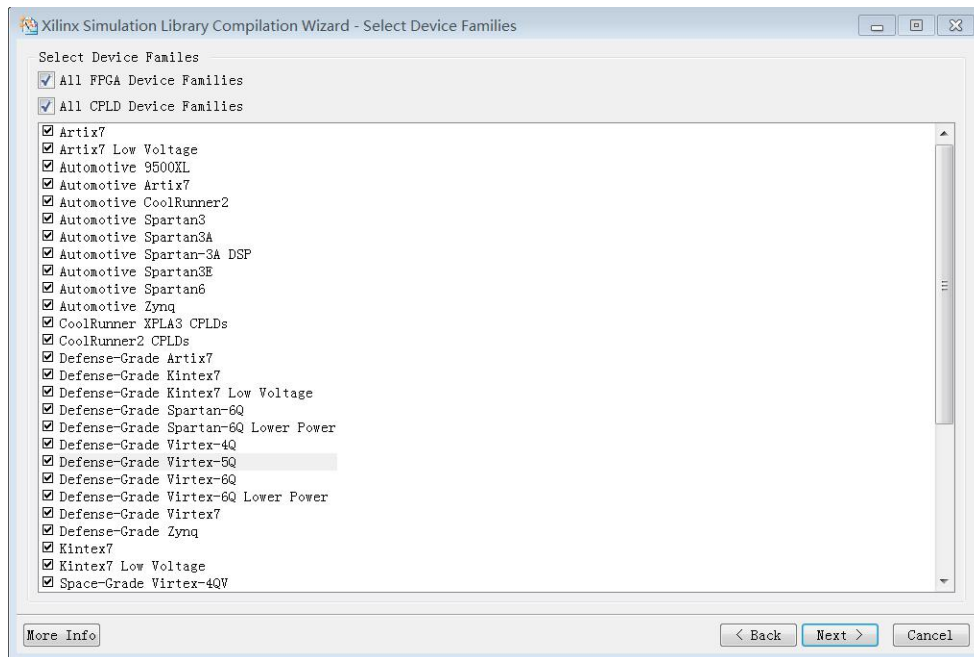
The path is "C:\modeltech64\_10.1C\win64



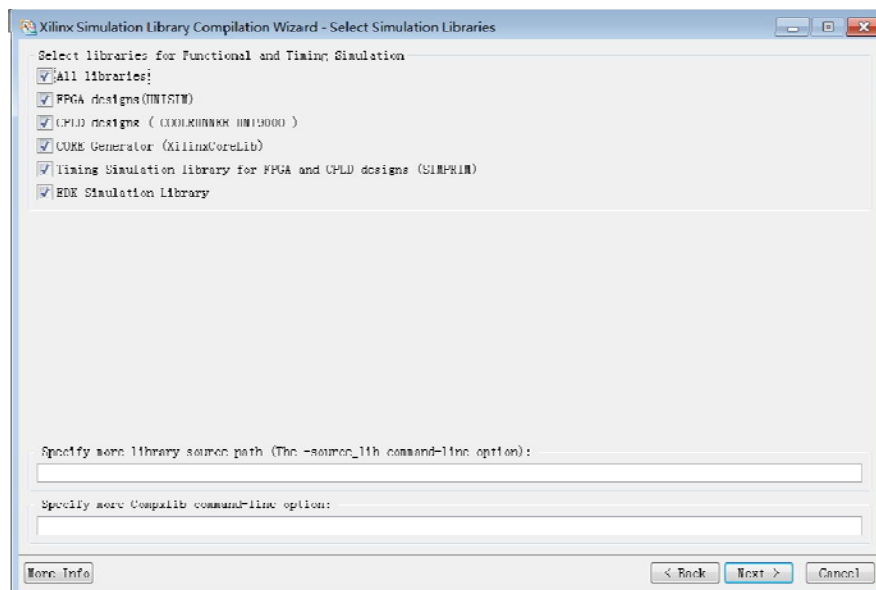
3. Select the language you want to compile as shown below. Generally we use the default option "Both VHDL and Verilog" and click Next.



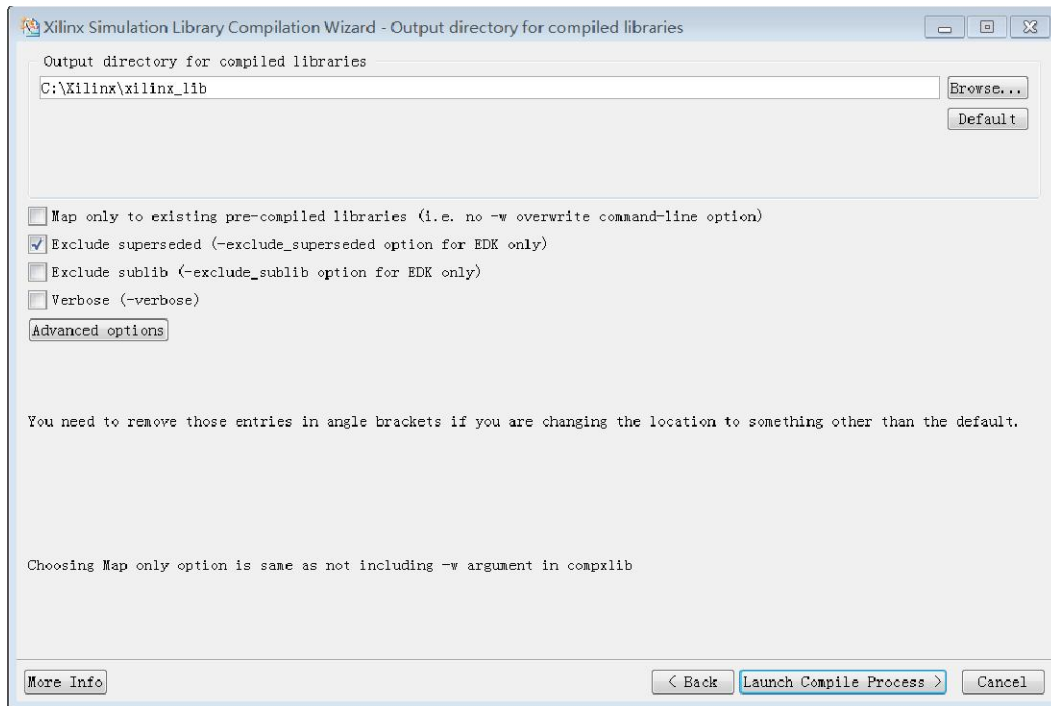
4. Select the Xilinx FPGA and CPLD device libraries that need to be compiled as shown below. The default is checked. Click "Next"



5. As shown in the figure below, this step is by default, all selected. The following two lines can be left blank, click "Next".

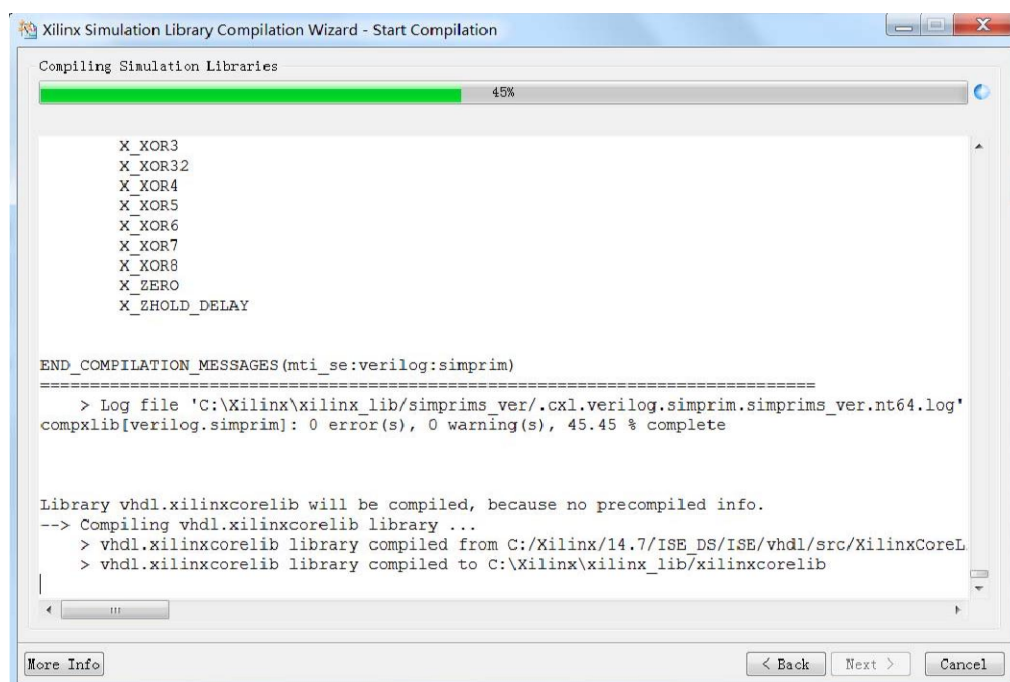


6. Fill in the path of the output compiled library under "Output directory for compiled libraries". Here we enter "C:\Xilinx\Xilinx\_lib". Note that we need to create a new folder for Xilinx\_lib in the C:\Xilinx directory. . Other options are also available by default, then click on "Launch Compiled Process"



7. Here, the key reminder: the compilation progress time is longer, depending on your computer configuration, my computer

It takes about 30 minutes, especially if the compilation progress will stay at 0% for a long time. This is normal. Please be patient.

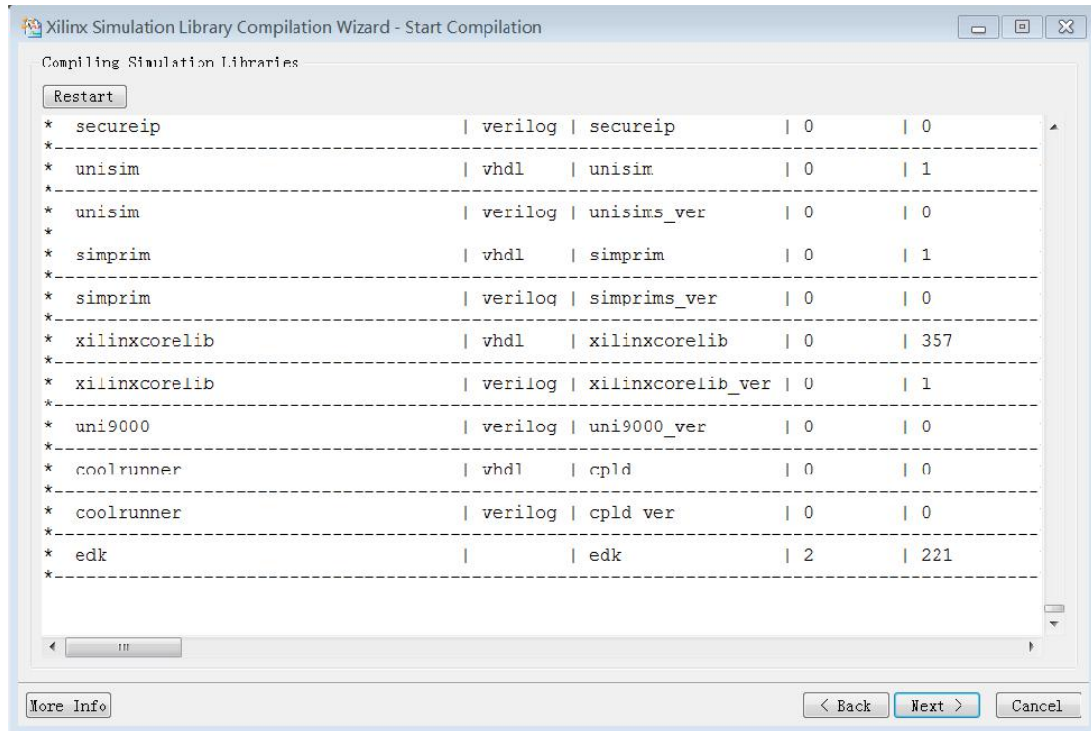


8. After 100%, it will jump to the interface as shown below, here report the error during compilation. And warning, warning can be ignored, error must be looked at, if there is a

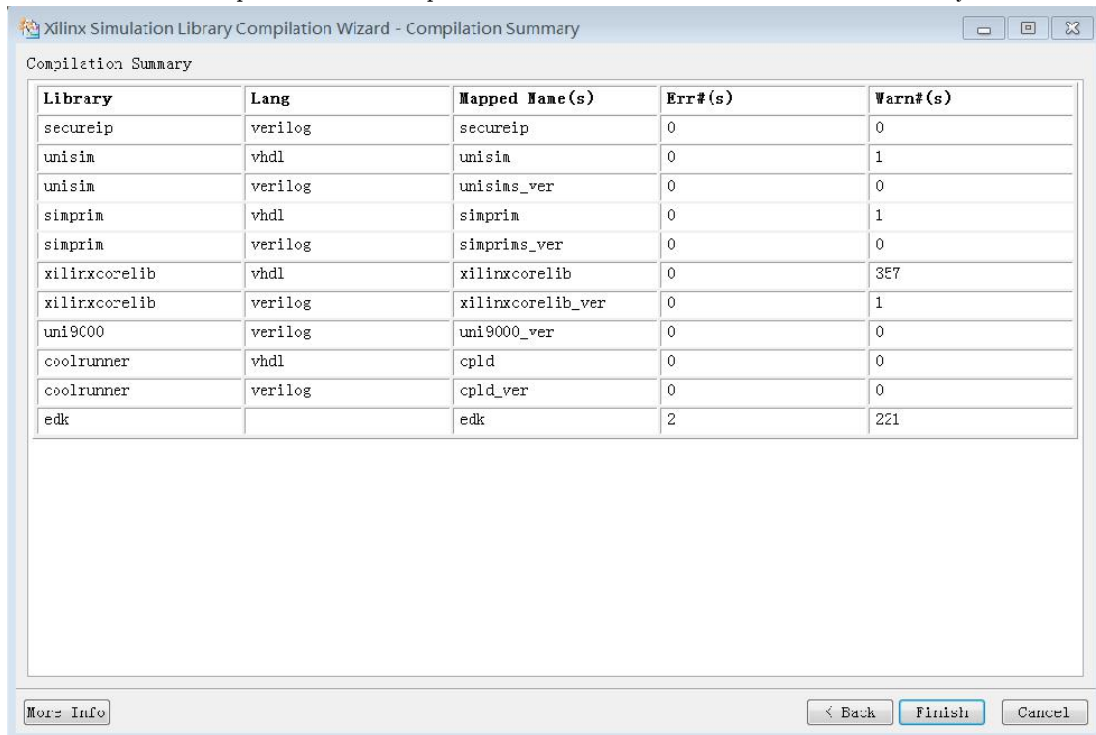
better return

See if the relevant path has Chinese or spaces, and the version is correct. I compiled edk here.

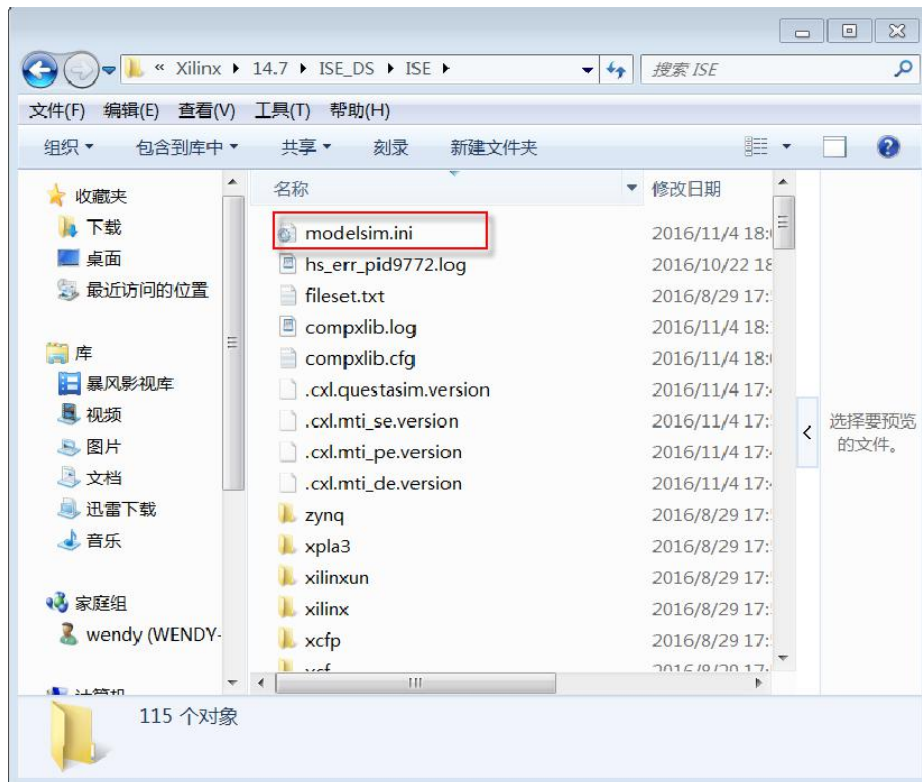
Error, can be ignored, we can not use it in the development process. Click "Next" to continue



9. The final compilation report is shown in the figure below. Click "Finish" to complete the compilation of the entire device library.



10. Now you will see a Modelsim.ini file in the ISE installation directory.



We open Modelsim.ini and copy the contents of the shadows (in the modelsim.ini file)  
 Line 47 starts from the top line of "[vcom]", that is, the content of the 308th action, all selected and copied)  
 The picture below starts at line 47:

```
modelsim.ini - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

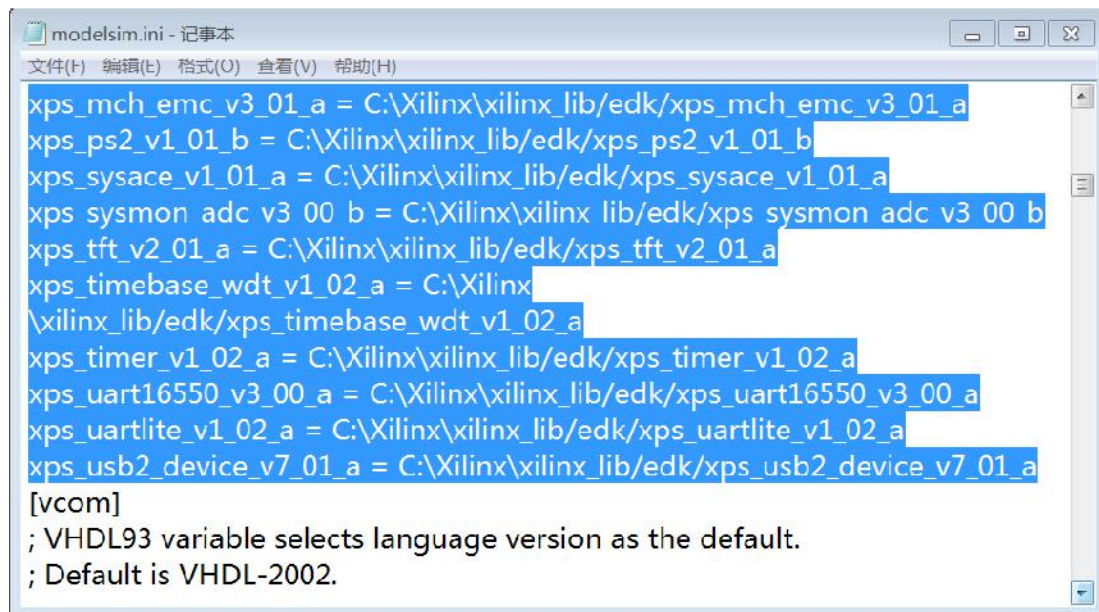
; same packages).
; A design should not reference VITAL from both the ieee library and the
; vital2000 library because the vital packages are effectively different.
; A design that references both the ieee and vital2000 libraries must have
; both logical names ieee and vital2000 mapped to the same library, either of
; these:
; $MODEL_TECH/./ieee
; $MODEL_TECH/./vital2000

;vhdl_psl_checkers = $MODEL_TECH/./vhdl_psl_checkers // Source files only for this release
;verilog_psl_checkers = $MODEL_TECH/./verilog_psl_checkers // Source files only for this release
;mvvc_lib = $MODEL_TECH/./mvvc_lib

secureip = C:\Xilinx\Xilinx_lib\secureip
unisim = C:\Xilinx\Xilinx_lib\unisim
unimacro = C:\Xilinx\Xilinx_lib\unimacro
unisims_ver = C:\Xilinx\Xilinx_lib\unisims_ver
unimacro_ver = C:\Xilinx\Xilinx_lib\unimacro_ver
simprim = C:\Xilinx\Xilinx_lib\simprim
simprims_ver = C:\Xilinx\Xilinx_lib\simprims_ver
xilinxcorelib = C:\Xilinx\Xilinx_lib\xilinxcorelib
xilinxcorelib_ver = C:\Xilinx\Xilinx_lib\xilinxcorelib_ver
uni9000_ver = C:\Xilinx\Xilinx_lib\uni9000_ver
cpld = C:\Xilinx\Xilinx_lib\cpld
cpld_ver = C:\Xilinx\Xilinx_lib\cpld_ver
cdk = C:\Xilinx\Xilinx_lib\cdk
```

The following picture shows the behavior to 308



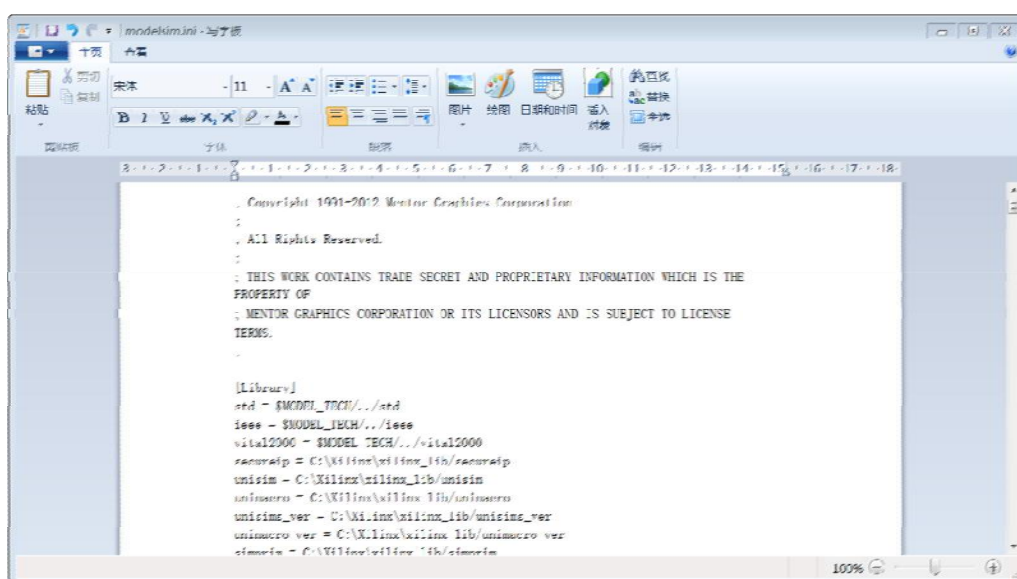


```
modelsim.ini - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

xps_mch_emc_v3_01_a = C:\Xilinx\Xilinx Lib\edk\xps_mch_emc_v3_01_a
xps_ps2_v1_01_b = C:\Xilinx\Xilinx Lib\edk\xps_ps2_v1_01_b
xps_sysace_v1_01_a = C:\Xilinx\Xilinx Lib\edk\xps_sysace_v1_01_a
xps_sysmon_adc_v3_00_b = C:\Xilinx\Xilinx Lib\edk\xps_sysmon_adc_v3_00_b
xps_tft_v2_01_a = C:\Xilinx\Xilinx Lib\edk\xps_tft_v2_01_a
xps_timebase_wdt_v1_02_a = C:\Xilinx\Xilinx Lib\edk\xps_timebase_wdt_v1_02_a
xps_timer_v1_02_a = C:\Xilinx\Xilinx Lib\edk\xps_timer_v1_02_a
xps_uart16550_v3_00_a = C:\Xilinx\Xilinx Lib\edk\xps_uart16550_v3_00_a
xps_uartlite_v1_02_a = C:\Xilinx\Xilinx Lib\edk\xps_uartlite_v1_02_a
xps_usb2_device_v7_01_a = C:\Xilinx\Xilinx Lib\edk\xps_usb2_device_v7_01_a
[vcom]
; VHDL93 variable selects language version as the default.
; Default is VHDL-2002.
```

11. Under Modelsim's installation directory, ie "C:\modeltech\_10.1c", look for

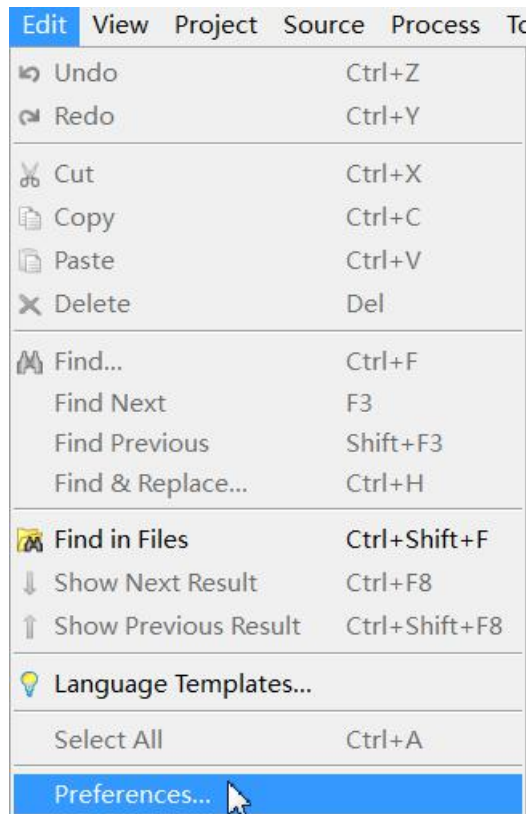
Open after "modelsim.ini" (note: first change the properties of this file under Modelsim - remove the read-only attribute). At the end of line 12, enter a line feed, and then paste the previously copied content as shown. Don't delete the original content.



```
modelsim.ini - 记事本
Copyright 1991-2002 Mentor Graphics Corporation
All Rights Reserved.
THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH IS THE
PROPERTY OF
MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS SUBJECT TO LICENSE
TERMS.

[Library]
std - $MODEL_TECH/./std
ieee - $MODEL_TECH/./ieee
vital2000 - $MODEL_TECH/./vital2000
sawarpip - C:\Xilinx\Xilinx Lib\sawarpip
unisim - C:\Xilinx\Xilinx Lib\unisim
unimacro - C:\Xilinx\Xilinx Lib\unimacro
unimever - C:\Xilinx\Xilinx Lib\unimever
unimacro ver - C:\Xilinx\Xilinx Lib\unimacro ver
simprim - C:\Xilinx\Xilinx Lib\simprim
```

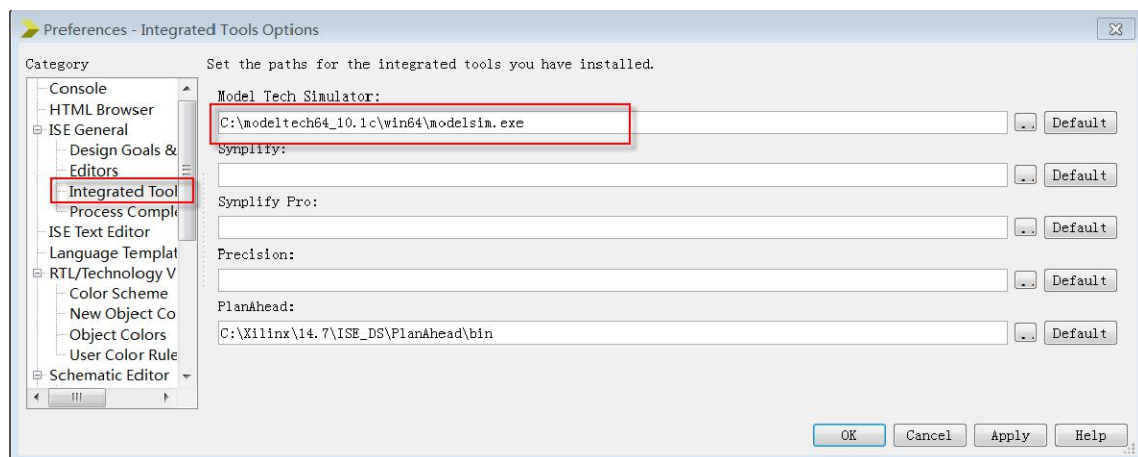
12. Open ISE14.7, then look for it on the ISE menu and click to open the Preferences window.



13. Under "Category" on the left, select "ISE General"->"Integrated"

Tools. In the Integrated Tools settings, enter the file path of Modelsim.exe under "Model Tech Simulator" on the right. Our path here is "C:\modeltech64\_10.1c\win64\modelsim.exe" as shown.

After completing the settings, click "OK"



At this point, the software installation is complete.