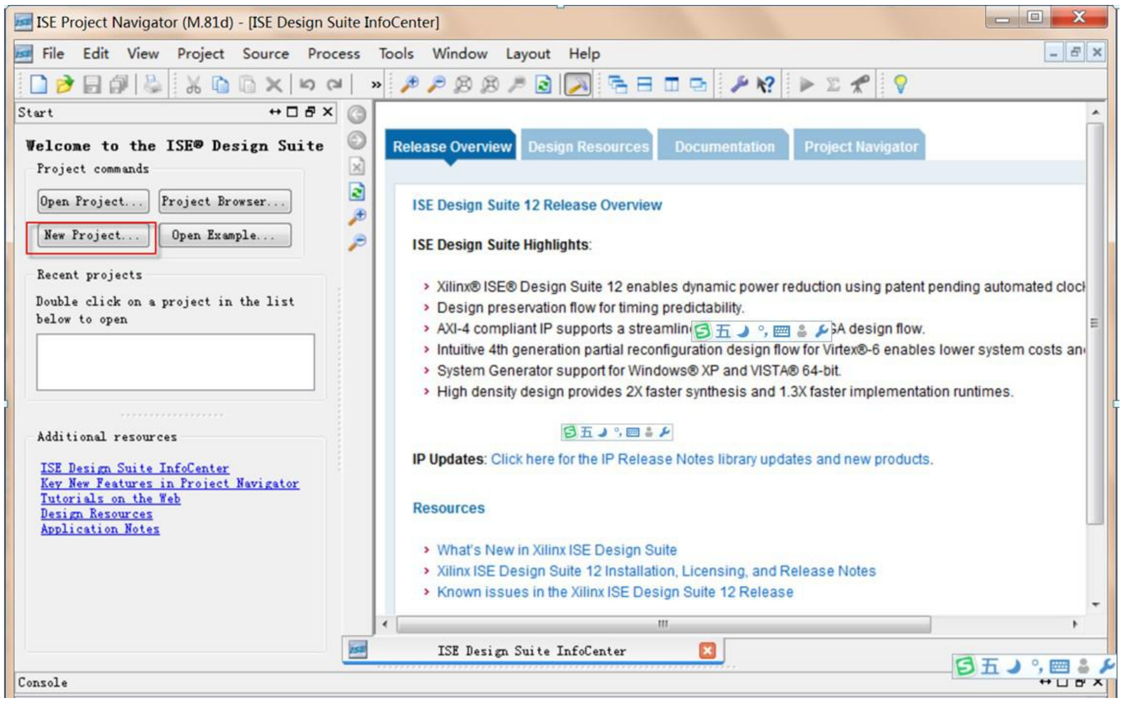
ISE establishes detailed engineering steps

The FPGA design flow includes circuit design input, functional simulation, design synthesis, post-synthesis simulation, design implementation, add constraints, post-route simulation and download, and debug. In general FPGA logic design, only the ISE design tool is needed. The following is an example of the simplest "LED street light", which explains the use of the ISE design tool and introduces the basic process of FPGA design based on ISE:

Step 1. Create a new project
Double-click the shortcut icon for the ISE desktop:

Or Start → All Programs → Open in Xilinx ISE Design Suite 12.4 → ISE Design Tools

Project Navigator. Open the following interface


ISE Project Navigator (M.81d) - [ISE Design Suite InfoCenter]
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Additional resources
ISE Design Suite InfoCenter
Key New Features in Project Navigator
Tutorials on the Web
Design Resources
Application Notes
Release Overview
Design Resources
Documentation
Project Navigator
ISE Design Suite InfoCenter
Console

Double click on a project in the list below to open

ISE Design Suite 12 Release Overview

ISE Design Suite Highlights:

- Xilinx® ISE® Design Suite 12 enables dynamic power reduction using patent pending automated cloc
- Design preservation flow for timing predictability.
- AXI-4 compliant IP supports a streamlin 3A design flow.
- Intuitive 4th generation partial reconfiguration design flow for Virtex®-6 enables lower system costs an
- System Generator support for Windows® XP and VISTA® 64-bit.
- High density design provides 2X faster synthesis and 1.3X faster implementation runtimes.

IP Updates: Click here for the IP Release Notes library updates and new products.

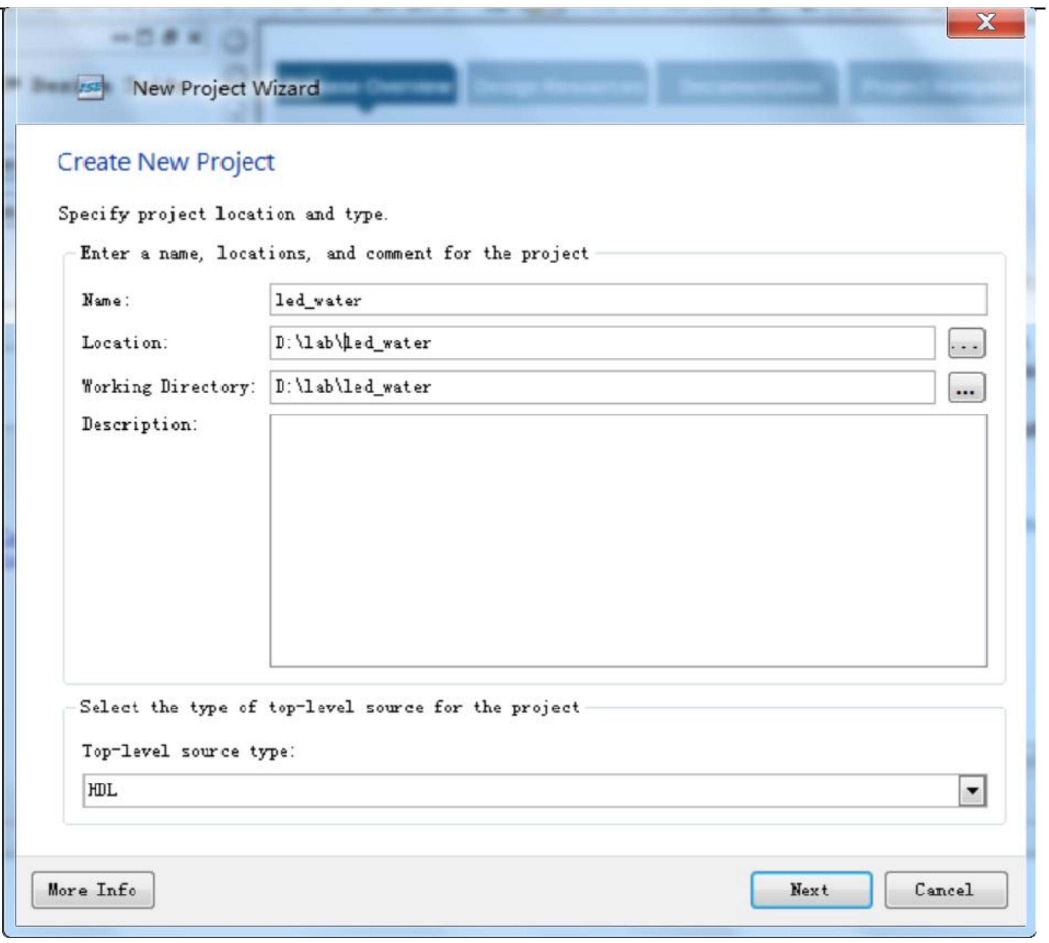
Resources

- What's New in Xilinx ISE Design Suite
- Xilinx ISE Design Suite 12 Installation, Licensing, and Release Notes
- Known issues in the Xilinx ISE Design Suite 12 Release

We need to create a new project, so click on New Project. If it is already built before

Cheng, then we can choose Open Project. At the same time, the most recently used items are listed below, and we can also open them by double-clicking.

You can see the new project wizard shown below.


New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: led_water

Location: D:\lab\led_water

Working Directory: D:\lab\led_water

Description:

Select the type of top-level source for the project

Top-level source type: HDL

Then enter the project name in Name and the software wil l be in both Location and working

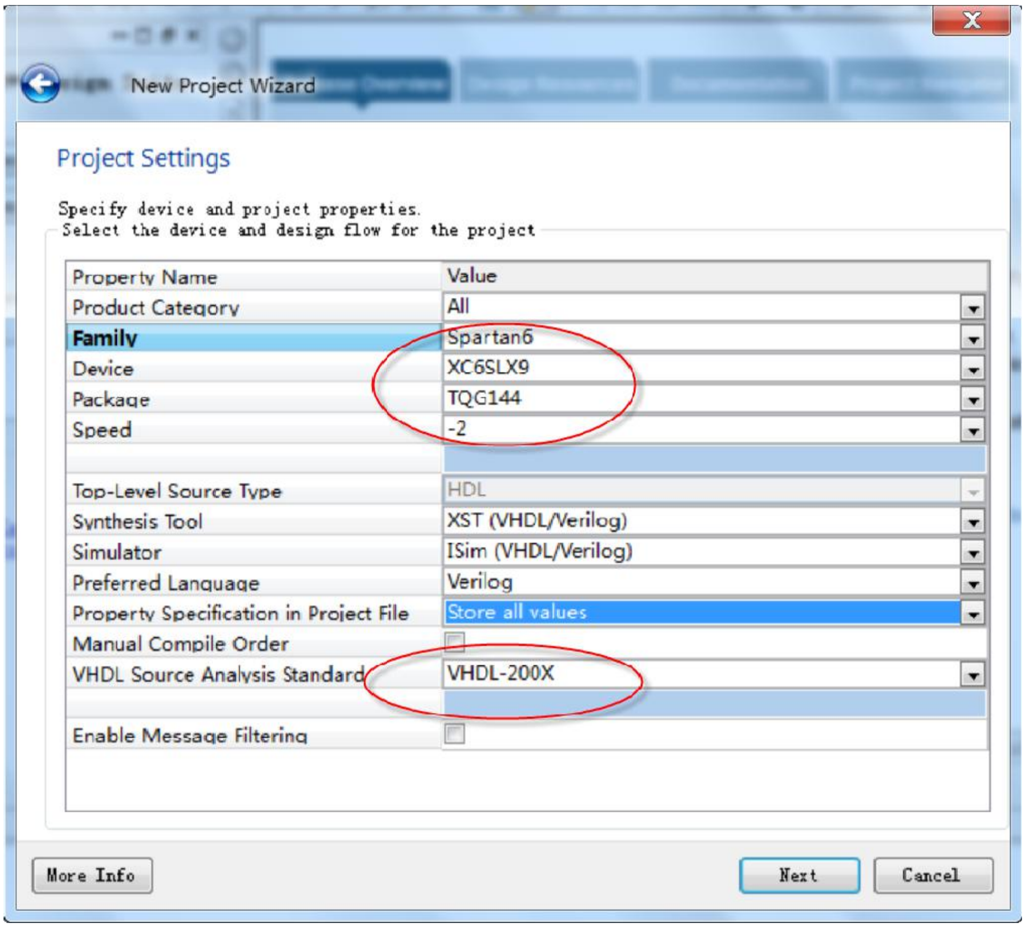
Create a new folder in the Directory with the same name as the project to hold al l the fi les for the project. In Select the path where our project is stored in Location. Because we are using

Veri log HDL language, hence Source Type Type we choose

HDL, here we use the Veri log module as the top-level input, so choose HDL. Enter the project name

Led_water, the fol lowing dialog box appears after you choose to store it under D: \ LAB. Cl ick Next.

Step 2. Engineering pre-set



Project Settings

Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Product Category	All
Family	Spartan6
Device	XC6SLX9
Package	TQG144
Speed	-2
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	☐
VHDL Source Analysis Standard	VHDL-200X
Enable Message Filtering	☐

In this step, the main settings of the FPGA device model, speed grade, synthesis tools and simulation tools are selected.

Choice, the rest of the general default can be. There are ALL and civilian grades in the Product Category.

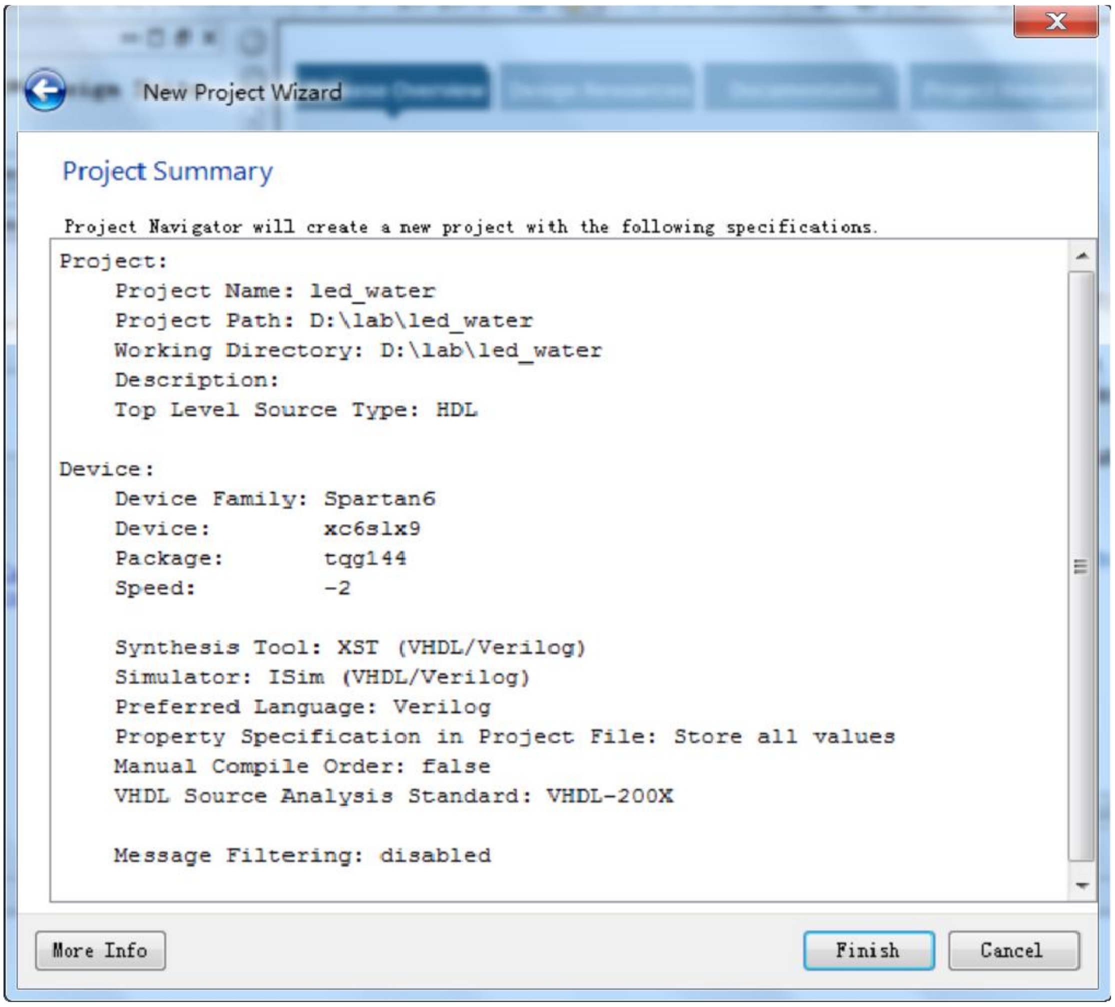
General Purpose, Industrial Grade Automotive, Military Grade Military / HiReliability, Aviation Anti-radiation

Shooting Radiation Tolerant Five options, here choose the default ALL. Chip model selection spartan6 XC6SLX9 for development board, package TQG144, speed grade -2

If you are using other boards, please choose according to the actual situation.

The comprehensive tool selects the XST that comes with ISE. Here, the comprehensive tool and simulation tool can choose the third. Side tools such as the commonly used SynplifyPro and Modelsim.

The choice of Verilog standard, ISE default is VHDL-93, it can also be changed to VHDL-200X, English VHDL-200X standard coverage is wider than VHDL-93, some keywords of VHDL-200X are not recognized in VHDL-93. Click Next.



Project Summary

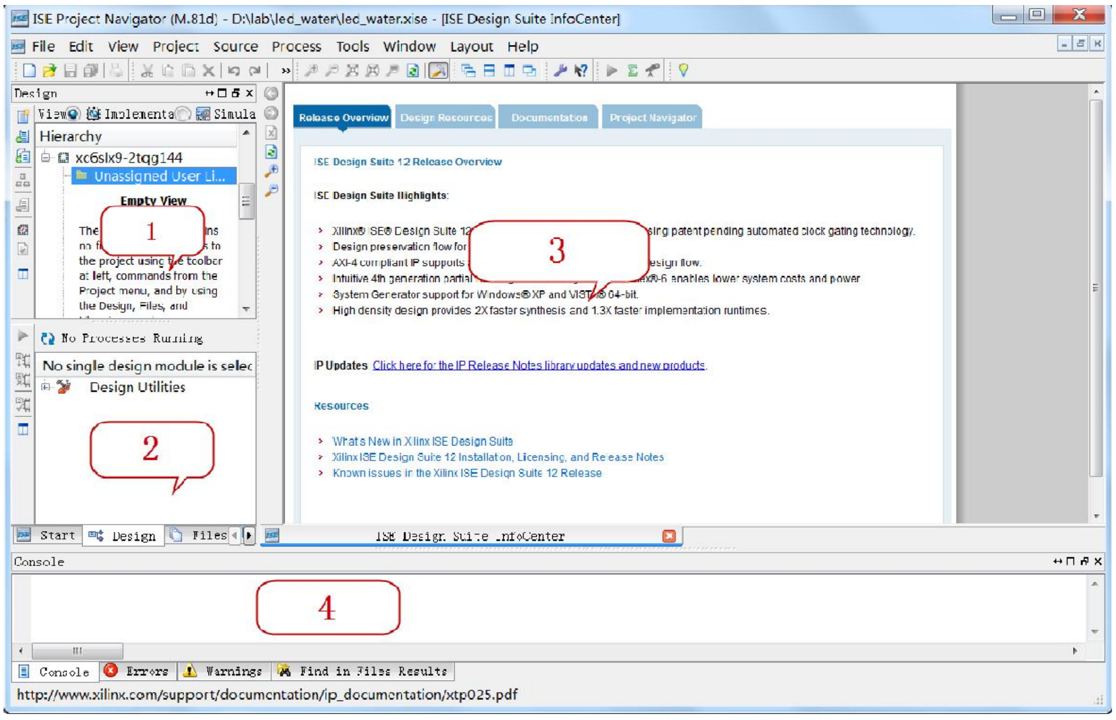
Project Navigator will create a new project with the following specifications.

```
Project:
    Project Name: led_water
    Project Path: D:\lab\led_water
    Working Directory: D:\lab\led_water
    Description:
    Top Level Source Type: HDL

Device:
    Device Family: Spartan6
    Device:        xc6slx9
    Package:       tqg144
    Speed:         -2

    Synthesis Tool: XST (VHDL/Verilog)
    Simulator: ISim (VHDL/Verilog)
    Preferred Language: Verilog
    Property Specification in Project File: Store all values
    Manual Compile Order: false
    VHDL Source Analysis Standard: VHDL-200X

    Message Filtering: disabled
```

This window will display the summary of the new project. After checking, click Finish to complete the project creation.

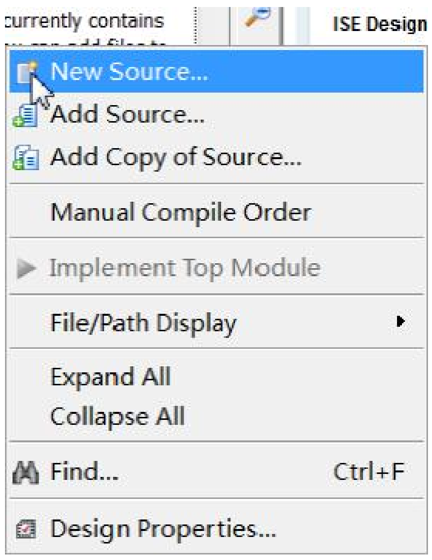
Step 3. Add new HDL source files

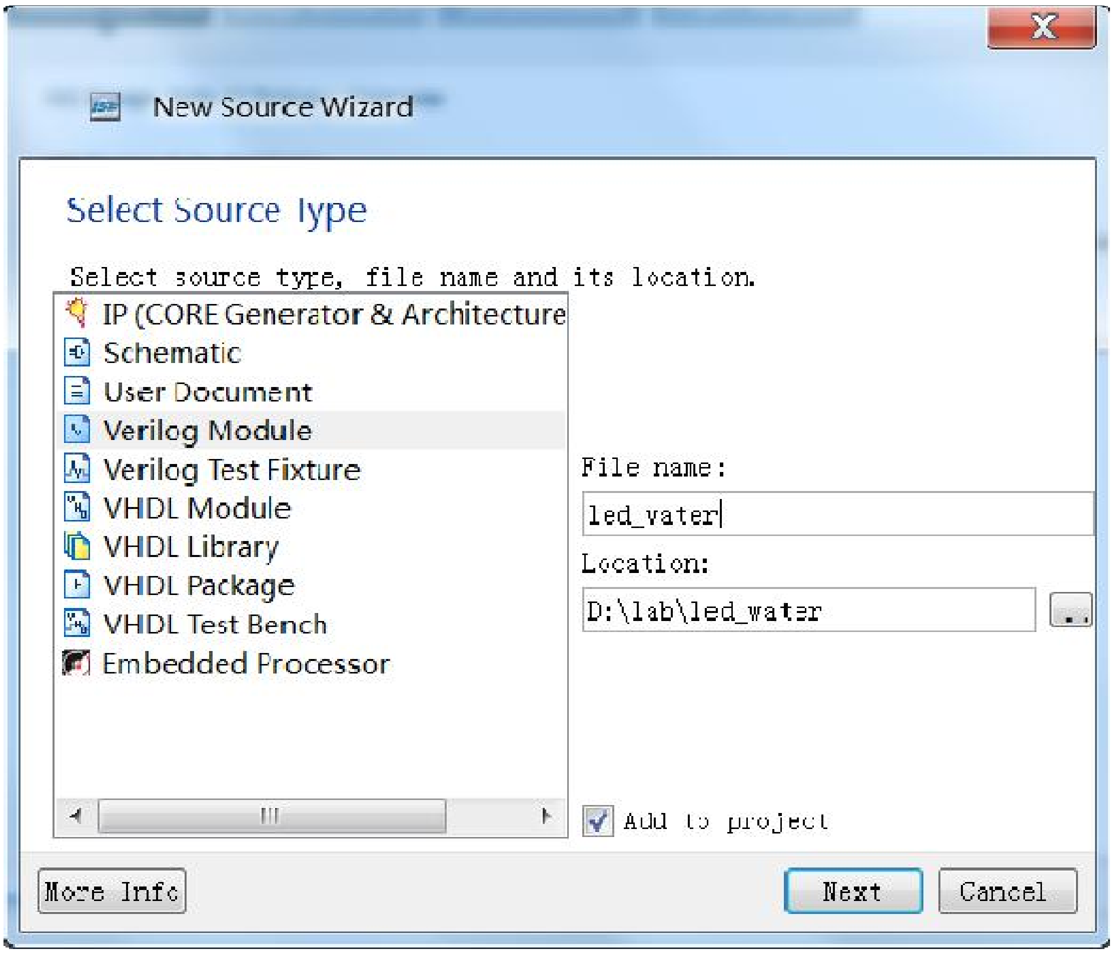
The newly created project interface appears after the previous step is completed.


ISE Project Navigator (M.81d) - D:\lab\led_water\led_water.xise - [ISE Design Suite InfoCenter]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
xc6slx9-2tqg144
Unassigned User Li...
Empty View
1
2
3
4
No Processes Running
No single design module is selec
Design Utilities
Release Overview
Design Resources
Documentation
Project Navigator
ISE Design Suite 12 Release Overview
ISE Design Suite Highlights:
IP Updates Click here for the IP Release Notes library updates and new products.
Resources
Start
Design
Files
ISE Design Suite InfoCenter
Console
Errors
Warnings
Find in Files Results
http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

region 1 Used to manage various files included in the project; area 2 Used to control the progress of the project, integrated / Compile, place and route, generate bit Files, etc .; area 3 Is the code display area; area 4 Information is displayed Display area and console, used to display various detailed information during the operation, Tcl Command input, etc.

In the area above 1 Right-click, New verilog File if the user already has Verilog Source program, you can also right-click to add directly Verilog file. We choose new New Source .




New Source Wizard

Select Source Type

Select source type, file name and its location.

File name: led_water

Location: D:\lab\led_water

[✓] Add to project

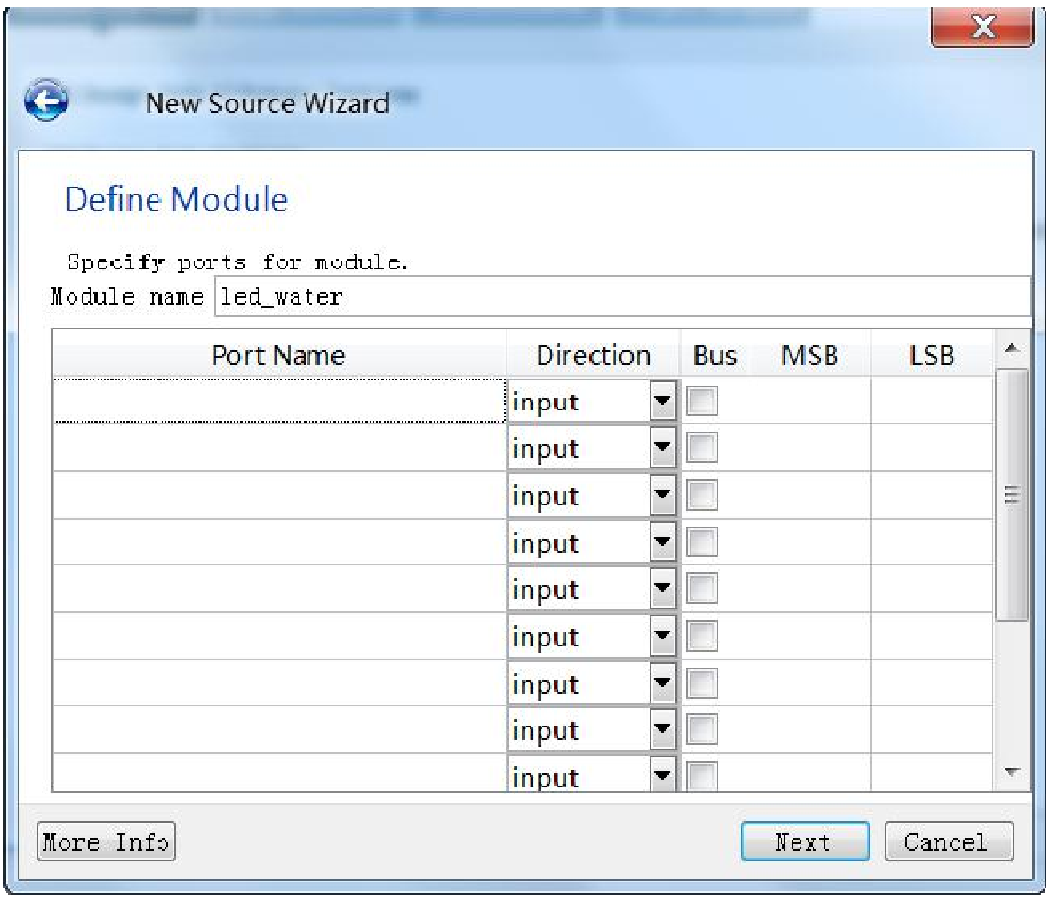
You can see the files that can be created IPcore , Schematic, Verilog , VHDL , Chipscope Wait

Wait, we are using Verilog Language, so choose Verilog Module ,in File name Lose

File name led_water , Click Next .

Next is to define the input and output interface of the module, as shown below. We generally work directly in a text editor

Enter, click here directly Next .



New Source Wizard

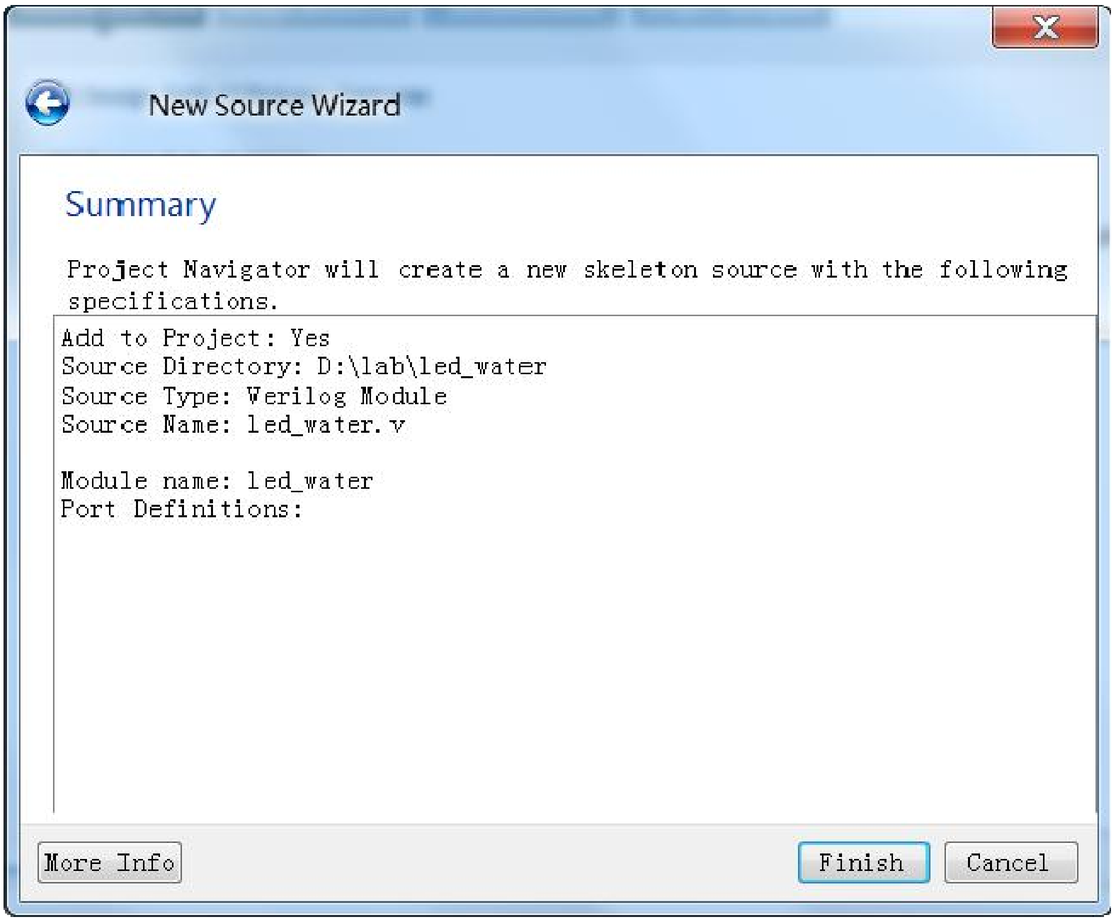
Define Module

Specify ports for module.

Module name led_water

Port Name	Direction	Bus	MSB	LSB
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		

Click on the image below Finish , We have finished creating a new one Verilog Source file work.



Summary

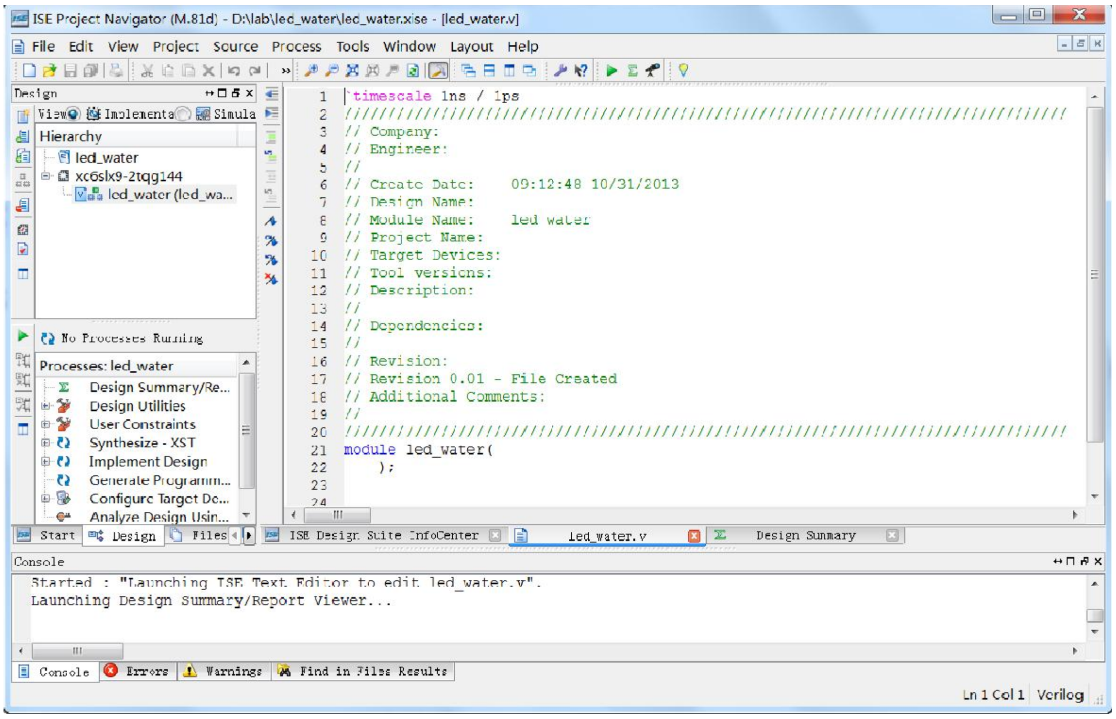
Project Navigator will create a new skeleton source with the following specifications.

```
Add to Project: Yes
Source Directory: D:\lab\led_water
Source Type: Verilog Module
Source Name: led_water.v

Module name: led_water
Port Definitions:
```

First 4 Step. Write code

The newly created file has been opened at this time. In the code area, we see the module header comment and the module name. under

In one step, we need to write relevant code in the code area to achieve control led Function.



```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    09:12:48 10/31/2013
// Design Name:
// Module Name:    led_water
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module led_water(
    );
```

```
Started : "Launching ISE Text Editor to edit led_water.v".
Launching Design Summary/Report Viewer...
```

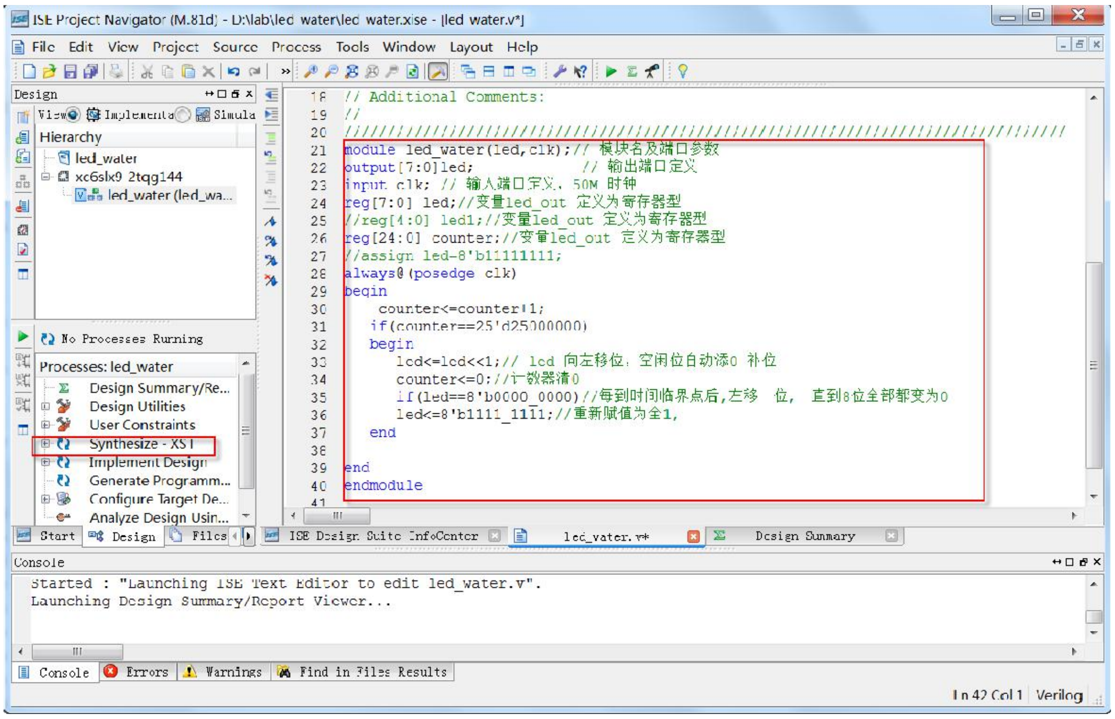
Enter the corresponding function code, as shown below. Double click Synthesize - XST Perform a comprehensive compilation and check

Check for errors in code writing

```
module led_water (led, clk); // Module name and port parameters   end
output [7: 0] led;                                // output port definition
input clk; // input port definition, 50M clock
reg [7: 0] led; // The variable led_out is defined as a registered type    Device
// reg [4: 0] led1; // The variable led_out is defined as a register type
reg [24: 0] counter; // The variable led_out is defined as a register type
// assign led = 8'b11111111;
always @ (posedge clk)
begin
    counter <= counter + 1;
   if (counter == 25'd25000000)
   begin
          led <= led << 1; // led is shifted to the left, and the free bits are automatically added with 0 complement bits
          counter <= 0; // Counter cleared to 0
          if (led == 8'b0000_0000) // When the time critical point is reached, shift to the left one bit, until all 8 bits One
```

Charge fog 0

```
            led <= 8'b1111_1111; // The new assignment weight value is all 1,
    end

end
endmodule
```

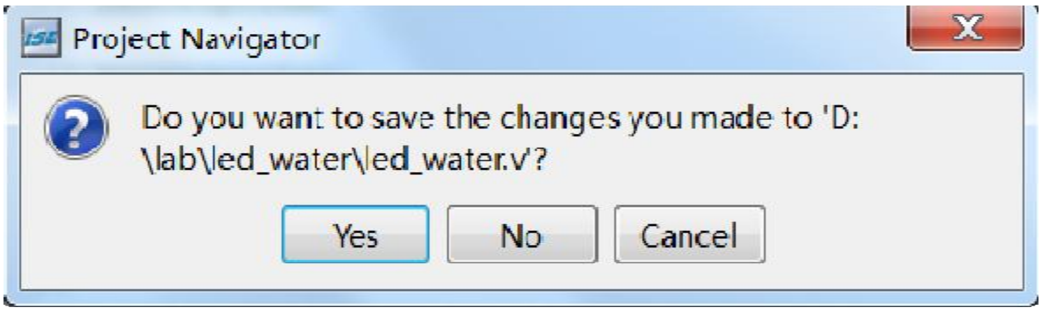


ISE Project Navigator (M.81d) - D:\lab\led water\led water.xise - [led water.v*]

```
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////
module led_water(led,clk);// 模块名及端口参数
output[7:0]led;             // 输出端口定义
input clk; // 输入端口定义, 50M 时钟
reg[7:0] led;//变量led_out 定义为寄存器型
//reg[4:0] led1;//变量led_out 定义为寄存器型
reg[24:0] counter;//变量led_out 定义为寄存器型
//assign led-8'b11111111;
always@(posedge clk)
begin
    counter<=counter+1;
   if(counter==25'd25000000)
   begin
      led<=led<<1;// led 向左移位, 空闲位自动添0 补位
      counter<=0;//计数器清0
      if(led==8'b0000_0000)//每到时间临界点后,左移  位,  直到8位全部都变为0
      led<=8'b1111_1111;//重新赋值为全1,
   end

end
endmodule
```

```
Started : "Launching ISE Text Editor to edit led_water.v".
Launching Design Summary/Report Viewer...
```

Prompt whether to save, obviously, Yes



Project Navigator

Do you want to save the changes you made to 'D:\lab\led_water\led_water.v'?

After the compilation is complete, a green check mark or a yellow exclamation mark will appear behind the blue double arrow in front. If compiled

An error occurred during the process, which will stop halfway and display a red cross.

Green checkmark: It means that there are no warnings or errors during the comprehensive compilation process.

Yellow exclamation mark: it indicates that an alarm is generated during the comprehensive compilation process, you need to pay attention to whether th

Warning.

The red cross indicates that an error occurred during the comprehensive compilation process and the compilation is terminated.

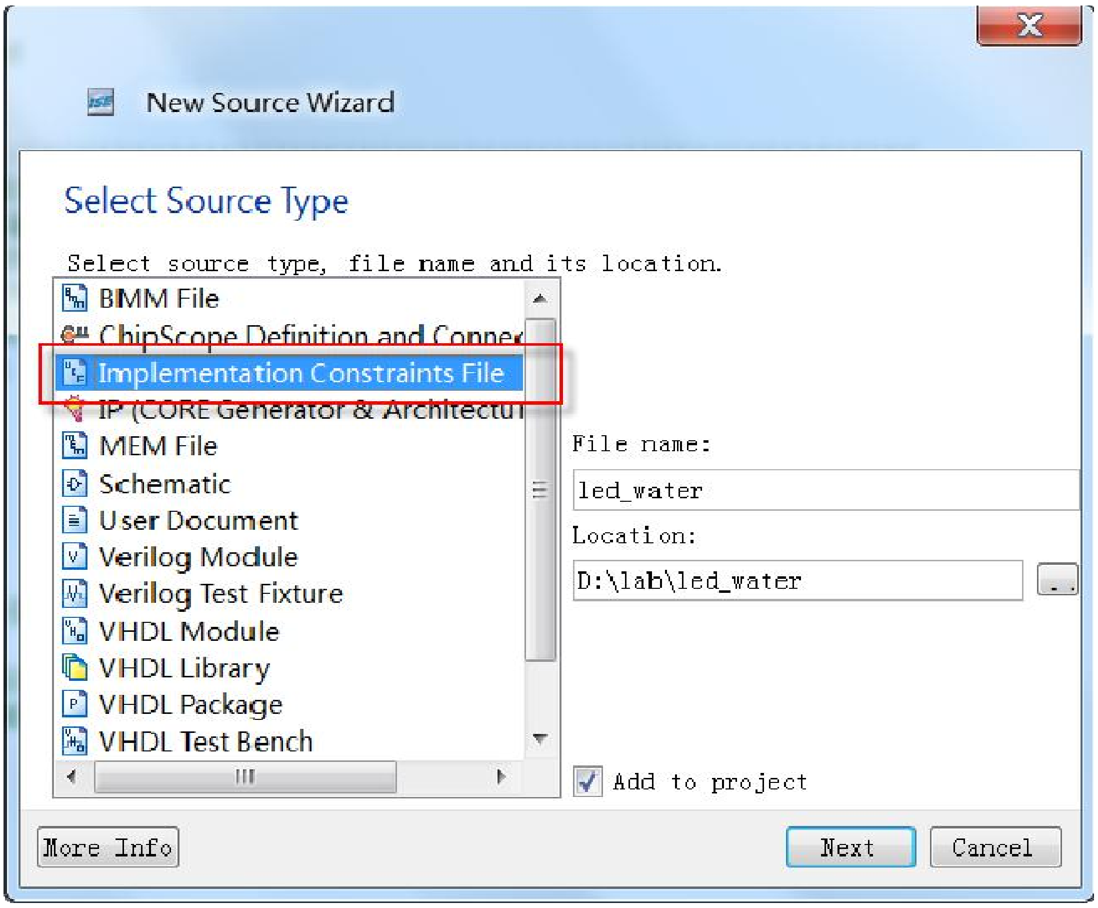
First 5 Step. Create a new pin constraint file UCF

In this step, we need to create a new pin constraint file UCF To establish correspondence between codes and circuit boards

relationship. Refer to section 3 Step, or add a new file, we choose Implementation Constraints File ,

File name Input led_water (Same name as the top-level module). Click next –> Finish Complete the binding

New creation.


New Source Wizard

Select Source Type

Select source type, file name and its location.

- BMM File
- ChipScope Definition and Connec
- Implementation Constraints File
- IP (CORE Generator & Architectu
- MEM File
- Schematic
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench

File name: led_water

Location: D:\lab\led_water

✓ Add to project

Click on the pop-up window to confirm the information is correct Finish . The software will automatically open the constraint file for editing

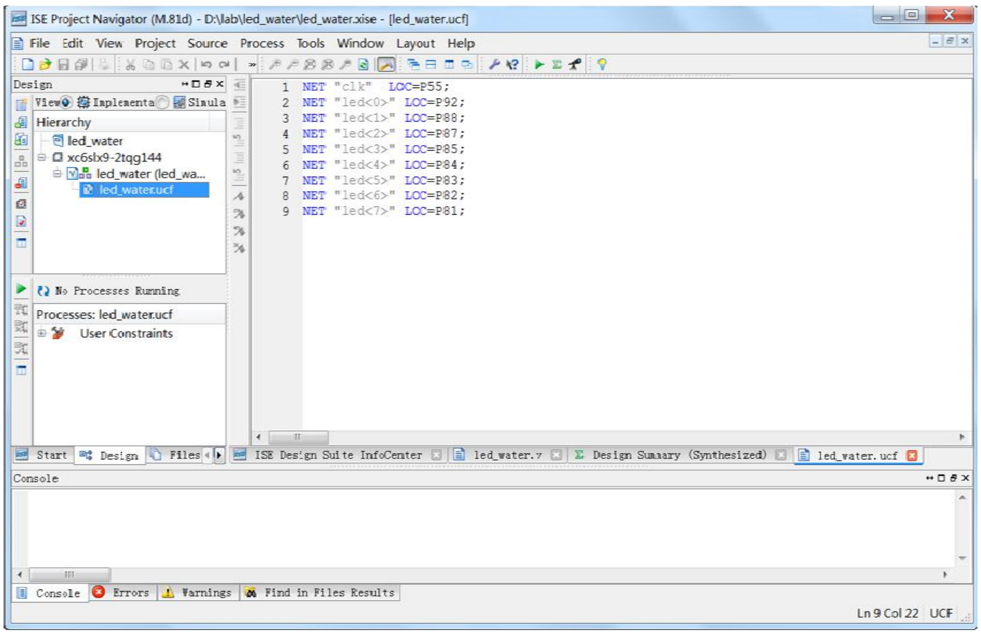
Window, enter the following code and click save. Note that this part needs to be compared with the pin assignment table of the development board, one by one

distribution.

```
NET "clk" LOC = P55;
NET "led <0>" LOC = P92;
NET "led <1>" LOC = P88;
NET "led <2>" LOC = P87;
NET "led <3>" LOC = P85;
NET "led <4>" LOC = P84;
NET "led <5>" LOC = P83;
NET "led <6>" LOC = P82;
NET "led <7>" LOC = P81;
```

Constraint files can also be selected by selecting User Constraints → I / O Pin Planning

start up PlanAhead To add the generation through the graphical interface.

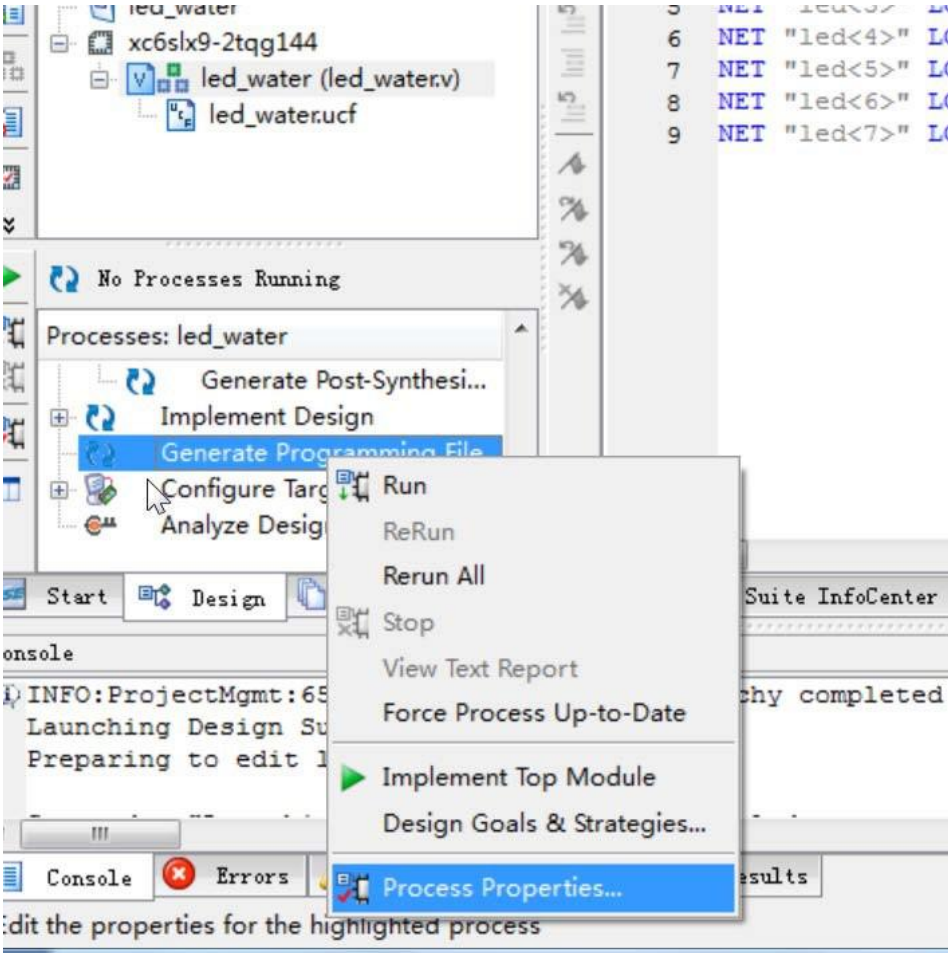

ISE Project Navigator (M.81d) - D:\lab\led_water\led_water.xise - [led_water.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
led_water
xc6slx9-2tqg144
led_water (led_wa...
led_water.ucf
No Processes Running
Processes: led_water.ucf
User Constraints
Start Design Files
ISE Design Suite InfoCenter
led_water.v
Design Summary (Synthesized)
led_water.ucf
Console
Console Errors Warnings Find in Files Results
Ln 9 Col 22 UCF

```
NET "clk"  LOC=P55;
NET "led<0>" LOC=P92;
NET "led<1>" LOC=P88;
NET "led<2>" LOC=P87;
NET "led<3>" LOC=P85;
NET "led<4>" LOC=P84;
NET "led<5>" LOC=P83;
NET "led<6>" LOC=P82;
NET "led<7>" LOC=P81;
```

First 6 Step. Property settings

After the constraint file is added, the attribute setting is required. in Generate Programming File on

Click the right mouse button and select Process Properties Option to set properties.

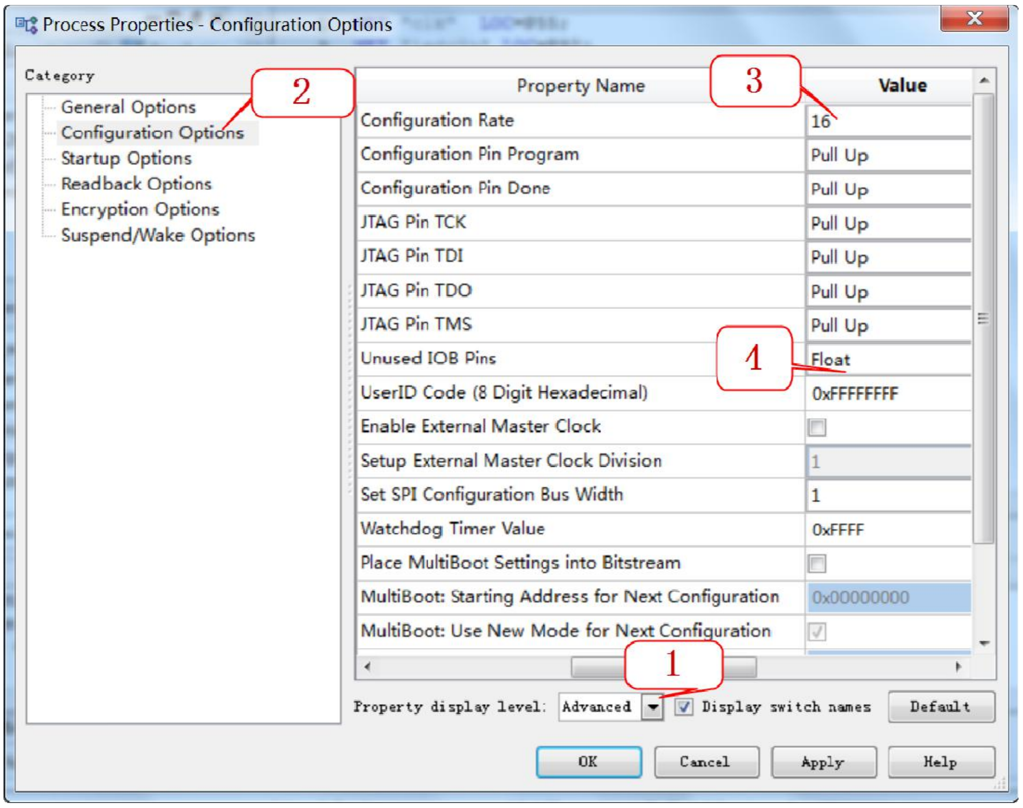


```
NET "led<4>" L
NET "led<5>" L
NET "led<6>" L
NET "led<7>" L
```

```
INFO:ProjectMgmt:65                                  hy completed
Launching Design Su
Preparing to edit l
```

Edit the properties for the highlighted process

The property setting interface is as follows,


Process Properties - Configuration Options

Category

- General Options
- Configuration Options
- Startup Options
- Readback Options
- Encryption Options
- Suspend/Wake Options

Property Name	Value
Configuration Rate	16
Configuration Pin Program	Pull Up
Configuration Pin Done	Pull Up
JTAG Pin TCK	Pull Up
JTAG Pin TDI	Pull Up
JTAG Pin TDO	Pull Up
JTAG Pin TMS	Pull Up
Unused IOB Pins	Float
UserID Code (8 Digit Hexadecimal)	0xFFFFFFFF
Enable External Master Clock	☐
Setup External Master Clock Division	1
Set SPI Configuration Bus Width	1
Watchdog Timer Value	0xFFFF
Place MultiBoot Settings into Bitstream	☐
MultiBoot: Starting Address for Next Configuration	0x00000000
MultiBoot: Use New Mode for Next Configuration	✓

Property display level: Advanced

✓ Display switch names

(1) First choose Advanced Mode, so look at it to see more configuration items.

(2) Then we choose Configuration Option , We choose the default value for other content

So.

(3) Configuration rate Is the configuration SPI load FPGA When mirroring CCLK Clock frequency

Rate, the default is 2MHz ,

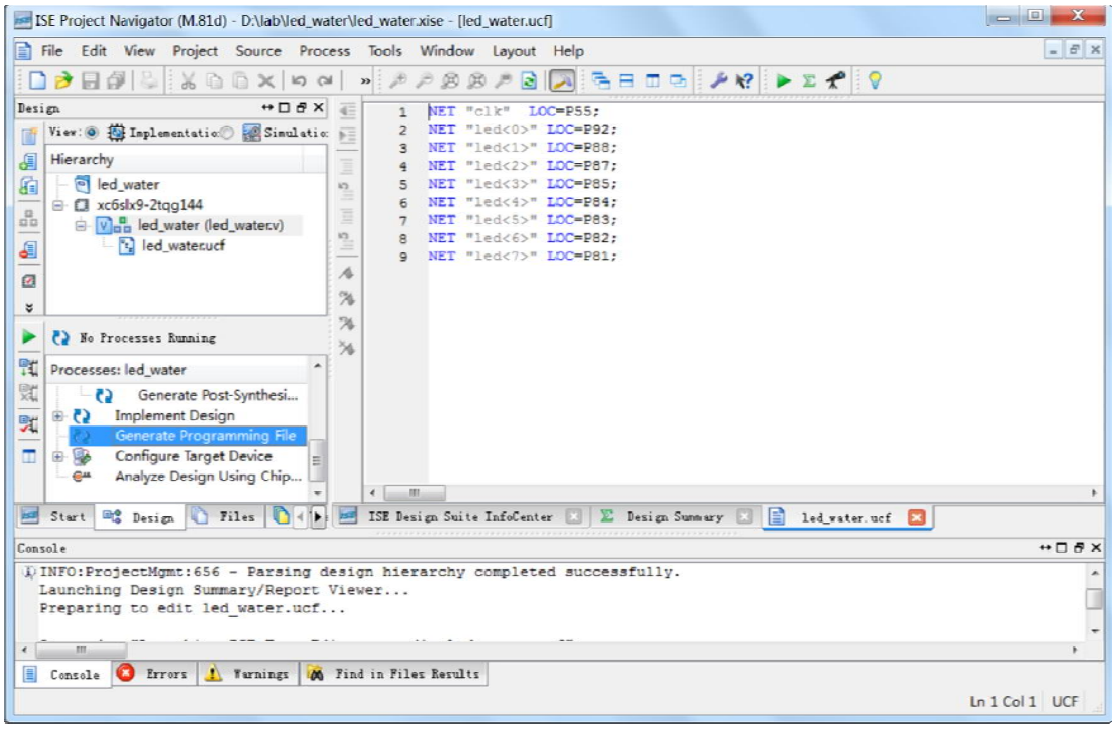
We generally choose 16MHz , So that the loading speed will be faster.

(4) select SPI Flash Bit width, you can choose 1/2/4 ,select 1 .

Click after configuring as shown OK , That is configured to generate bit Mode. Double click Generate

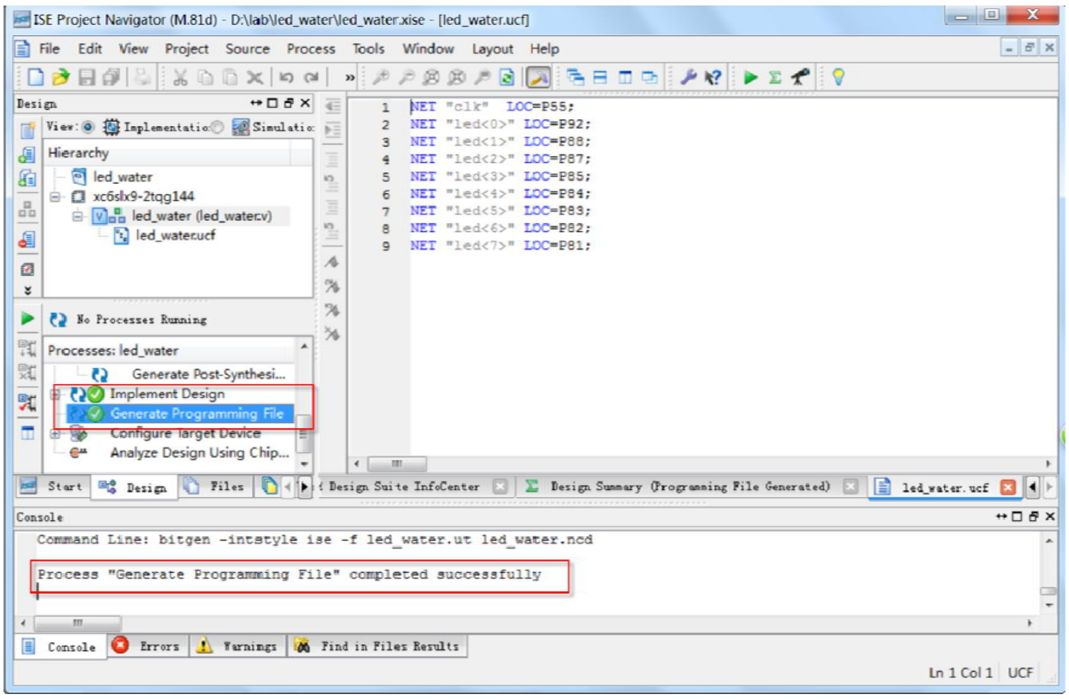
Programming File Let the software complete functions such as place and route, and regenerate the ones defined by the new bit Text

Pieces.


ISE Project Navigator (M.81d) - D:\lab\led_water\led_water.xise - [led_water.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
led_water
xc6slx9-2tqg144
led_water (led_water.v)
led_water.ucf
No Processes Running
Processes: led_water
Generate Post-Synthesi...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Chip...
Start Design Files
ISE Design Suite InfoCenter
Design Summary
led_water.ucf
Console
Console Errors Warnings Find in Files Results
Ln 1 Col 1 UCF

```
NET "clk"  LOC=P55;
NET "led<0>" LOC=P92;
NET "led<1>" LOC=P88;
NET "led<2>" LOC=P87;
NET "led<3>" LOC=P85;
NET "led<4>" LOC=P84;
NET "led<5>" LOC=P83;
NET "led<6>" LOC=P82;
NET "led<7>" LOC=P81;
```

```
INFO:ProjectMgmt:656 - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
Preparing to edit led_water.ucf...
```


ISE Project Navigator (M.81d) - D:\lab\led_water\led_water.xise - [led_water.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
led_water
xc6slx9-2tqg144
led_water (led_water.v)
led_water.ucf
No Processes Running
Processes: led_water
Generate Post-Synthesi...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Chip...
Start Design Files
Design Suite InfoCenter
Design Summary (Programming File Generated)
led_water.ucf
Console
Console Errors Warnings Find in Files Results
Ln 1 Col 1 UCF

```
NET "clk"  LOC=P55;
NET "led<0>" LOC=P92;
NET "led<1>" LOC=P88;
NET "led<2>" LOC=P87;
NET "led<3>" LOC=P85;
NET "led<4>" LOC=P84;
NET "led<5>" LOC=P83;
NET "led<6>" LOC=P82;
NET "led<7>" LOC=P81;
```

```
Command Line: bitgen -intstyle ise -f led_water.ut led_water.ncd

Process "Generate Programming File" completed successfully
```