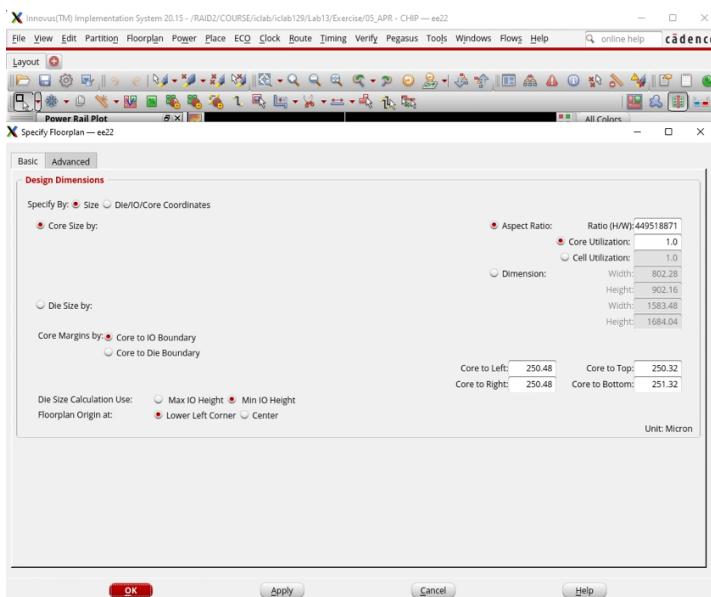


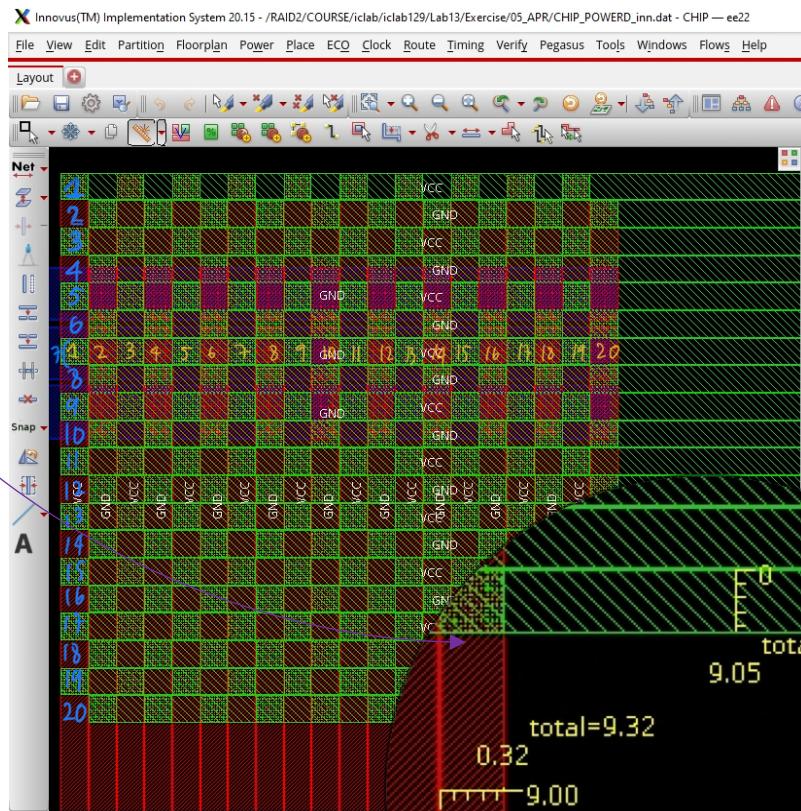
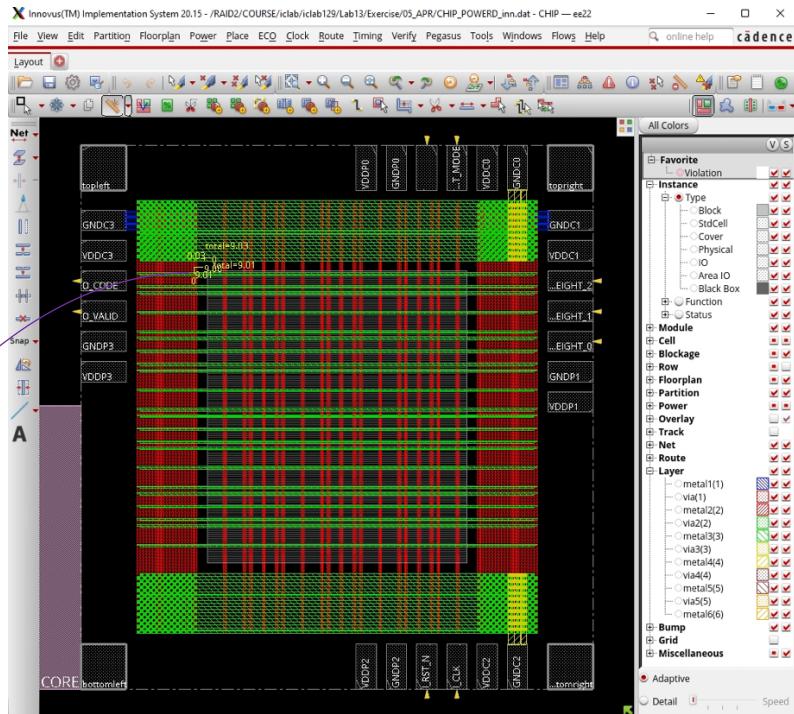
# APRII & IR Drop

## Lab13

### 1. Core to IO boundary:



## 2. Core Ring:



These screenshots showcase the core rings part of the power plan stage of the APR.

### 3. Post-Route setup time analysis:

```

ee22.ee.ncut.edu.tw (iclab129)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
9. ee22.ee 10. /home/m 12. 140.113 13. ee22.ee 14. ee25.ee 18. ee25.ee
Reconnect SSH-browser
(RAID2/COURSE/iclab/iclab129)
Start delay calculation (fullDC) (1 T). (MEM=2552.32)
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 8941.
Total number of fetched objects 8941
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8920, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=2590.48 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2590.48 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:43.4 real=0:00:04.0 totSessioncpu=0:06:48 mem=2590.5M)

timeDesign Summary

Setup views included:
av_func_mode_max

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 7.081 | 10.175 | 7.081 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 371 | 281 | 370 |
+-----+-----+-----+-----+-----+-----+-----+-----+
Real Total
DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
Lab01 | 0 (0) | 0.000 | 0 (0) |
Lab02 | 0 (0) | 0.000 | 0 (0) |
Lab03 | 0 (0) | 0.000 | 0 (0) |
Lab04 | 0 (0) | 0 | 0 (0) |
Lab05 | 0 (0) | 0 | 0 (0) |
Lab06 | 0 (0) | 0 | 0 (0) |
Lab07 | 0 (0) | 0 | 0 (0) |
Lab08 | 0 (0) | 0 | 0 (0) |
Lab09 | 0 (0) | 0 | 0 (0) |
Lab10 | 0 (0) | 0 | 0 (0) |
Lab12 | 0 (0) | 0 | 0 (0) |
Lab13 | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+-----+-----+-----+-----+
Density: 38.376%
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 21.57 sec
Total Real time: 25.0 sec
Total Memory Usage: 2567.75 Mbytes
Reset AAE Options
*** timeDesign #4 [finish] : cpu/real = 0:00:21.6/0:00:25.6 (0.8), totSession cpu/real = 0:06:48.5/
0:57:39.5 (0.1), mem = 2567.8M
innovos 6>

```

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The setup time analysis shows no TNS issues and no Violating paths.

As well as no DRV conditions have occurred.

### 4. Post-Route hold time analysis

```

ee22.ee.ncut.edu.tw (iclab129)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
9. ee22.ee 10. /home/m 12. 140.113 13. ee22.ee 14. ee25.ee 16. ee25.ee
Reconnect SSH-browser
(RAID2/COURSE/iclab/iclab129)
AAE_INFO: 1 threads acquired from CTE.
Start delay calculation (fullDC) (1 T). (MEM=2543.86)
Total number of fetched objects 8941
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8920, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2587.9 CPU=0:00:02.2 REAL=0:00:02.0)
End delay calculation (fullDC). (MEM=2587.9 CPU=0:00:02.4 REAL=0:00:02.0)
Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2587.9M)
Add other clocks and setuputeToAAEClockMapping during iteration 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2587.9M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2553.02)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8941.
Total number of fetched objects 8941
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8920, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2592.18 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2592.18 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:03.0 real=0:00:03.0 totSessioncpu=0:06:59 mem=2592.2M)

timeDesign Summary

Hold views included:
av_func_mode_min

+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 0.226 | 0.226 | 9.682 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 371 | 281 | 370 |
+-----+-----+-----+-----+-----+-----+-----+
Real Total
DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
Lab01 | 0 (0) | 0 | 0 (0) |
Lab02 | 0 (0) | 0 | 0 (0) |
Lab03 | 0 (0) | 0 | 0 (0) |
Lab04 | 0 (0) | 0 | 0 (0) |
Lab05 | 0 (0) | 0 | 0 (0) |
Lab06 | 0 (0) | 0 | 0 (0) |
Lab07 | 0 (0) | 0 | 0 (0) |
Lab08 | 0 (0) | 0 | 0 (0) |
Lab09 | 0 (0) | 0 | 0 (0) |
Lab10 | 0 (0) | 0 | 0 (0) |
Lab12 | 0 (0) | 0 | 0 (0) |
Lab13 | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+-----+-----+-----+
Density: 38.376%
Reported timing to dir timingReports
Total CPU time: 3.68 sec
Total Real time: 5.0 sec
Total Memory Usage: 2525.445312 Mbytes
Reset AAE Options
*** timeDesign #5 [finish] : cpu/real = 0:00:03.7/0:00:04.6 (0.8), totSession cpu/real = 0:06:59.4/
1:00:31.3 (0.1), mem = 2525.4M
innovos 6>

```

The Hold time analysis shows no DRV conditions have occurred.

## 5. DRC result:

Quick connect...

9. ee22.ee.nclu... 10. home/mob... 12. 14.10.113.225 13. ee22.ee.nclu... 14. ee22.ee.nclu...

VERIFICATION REPORT

File: /RAID/COURSE/EECLAB/clab129/

Name: Lab1

Sub-Area: 9 complete 0 Viols.

Sub-Area: {1075.200 241.920 1332.380 483.840} 10 of 30

VERIFICATION DRC ..... Sub-Area: 10 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {0.000 483.840 268.800 725.760} 11 of 30

VERIFICATION DRC ..... Sub-Area: 11 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {268.800 483.840 537.600 725.760} 12 of 30

VERIFICATION DRC ..... Sub-Area: 12 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {537.600 483.840 806.400 725.760} 13 of 30

VERIFICATION DRC ..... Sub-Area: 13 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {806.400 483.840 1075.200 725.760} 14 of 30

VERIFICATION DRC ..... Sub-Area: 14 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {1075.200 483.840 1332.380 725.760} 15 of 30

VERIFICATION DRC ..... Sub-Area: 15 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {0.000 725.760 268.800 967.680} 16 of 30

VERIFICATION DRC ..... Sub-Area: 16 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {268.800 725.760 537.600 967.680} 17 of 30

VERIFICATION DRC ..... Sub-Area: 18 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {537.600 725.760 806.400 967.680} 18 of 30

VERIFICATION DRC ..... Sub-Area: 19 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {806.400 725.760 1075.200 967.680} 19 of 30

VERIFICATION DRC ..... Sub-Area: {1075.200 725.760 1332.380 967.680} 20 of 30

VERIFICATION DRC ..... Sub-Area: 20 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {0.000 967.680 268.800 1209.600} 21 of 30

VERIFICATION DRC ..... Sub-Area: 21 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {268.800 967.680 537.600 1209.600} 22 of 30

VERIFICATION DRC ..... Sub-Area: 22 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {537.600 967.680 806.400 1209.600} 23 of 30

VERIFICATION DRC ..... Sub-Area: 23 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {806.400 967.680 1075.200 1209.600} 24 of 30

VERIFICATION DRC ..... Sub-Area: 24 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {1075.200 967.680 1332.380 1209.600} 25 of 30

VERIFICATION DRC ..... Sub-Area: 25 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {0.000 1209.600 268.800 1434.280} 26 of 30

VERIFICATION DRC ..... Sub-Area: 26 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {268.800 1209.600 537.600 1434.280} 27 of 30

VERIFICATION DRC ..... Sub-Area: 27 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {537.600 1209.600 806.400 1434.280} 28 of 30

VERIFICATION DRC ..... Sub-Area: 28 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {806.400 1209.600 1075.200 1434.280} 29 of 30

VERIFICATION DRC ..... Sub-Area: 29 complete 0 Viols.

VERIFICATION DRC ..... Sub-Area: {1075.200 1209.600 1332.380 1434.280} 30 of 30

VERIFICATION DRC ..... Sub-Area: 30 complete 0 Viols.

Verification Complete : 0 Viols.

\*\*\* End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 2.00 MEM: 41.0M) \*\*\*

Remote monitoring

Follow terminal folder

The DRC verification results show that no DRC violations have occurred.

## 6. LVS result:

The screenshot shows a terminal window with several tabs open. The current tab displays Verilog simulation results and connectivity verification details.

```
VERIFY DRC ..... Sub-Area: {0.000 967.680 268.800 1209.600} 21 of 30
VERIFY DRC ..... Sub-Area: {268.800 967.680 537.600 1209.600} 22 of 30
VERIFY DRC ..... Sub-Area: {537.600 967.680 806.400 1209.600} 23 of 30
VERIFY DRC ..... Sub-Area: {806.400 967.680 1075.200 1209.600} 24 of 30
VERIFY DRC ..... Sub-Area: {1075.200 967.680 1332.380 1209.600} 25 of 30
VERIFY DRC ..... Sub-Area: {25 0} 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1209.600 268.800 1434.280} 26 of 30
VERIFY DRC ..... Sub-Area: {26 0} 0 Viols.
VERIFY DRC ..... Sub-Area: {268.800 1209.600 537.600 1434.280} 27 of 30
VERIFY DRC ..... Sub-Area: {537.600 1209.600 806.400 1434.280} 28 of 30
VERIFY DRC ..... Sub-Area: {806.400 1209.600 1075.200 1434.280} 29 of 30
VERIFY DRC ..... Sub-Area: {1075.200 1209.600 1332.380 1434.280} 30 of 30
VERIFY DRC ..... Sub-Area: {30 0} 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 2.00 MEM: 41.0M) ***

innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY_CONNECTIVITY *****
Start Time: Fri Dec 22 03:54:58 2023

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1332.3800, 1434.2800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 03:54:58 **** Processed 5000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Dec 22 03:54:58 2023
Time Elapsed: 0:00:00.0

***** End: VERIFY_CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.4 MEM: 6.000M)

innovus 1>
```

The Connectivity verification results show that no LVS violations have occurred.

## 7. Post Layout simulation result:

```

PASS PATTERN NO.1967
PASS PATTERN NO.1968
PASS PATTERN NO.1969
PASS PATTERN NO.1970
PASS PATTERN NO.1971
PASS PATTERN NO.1972
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns

$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1819630000
VCS Simulation Report
Time: 1819630000 ps
CPU Time: 28.590 seconds; Data structure size: 2.2Mb
Fri Dec 22 04:21:22 2023
CPU time: 2.034 seconds to compile + .411 seconds to elab + .907 seconds to link + 28.696 seconds in simulation
4:21 iclab129@ee22[~/Lab13/Exercise/06_POST]$ 

```

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Post layout simulation is passed with same latency as of Gate level.

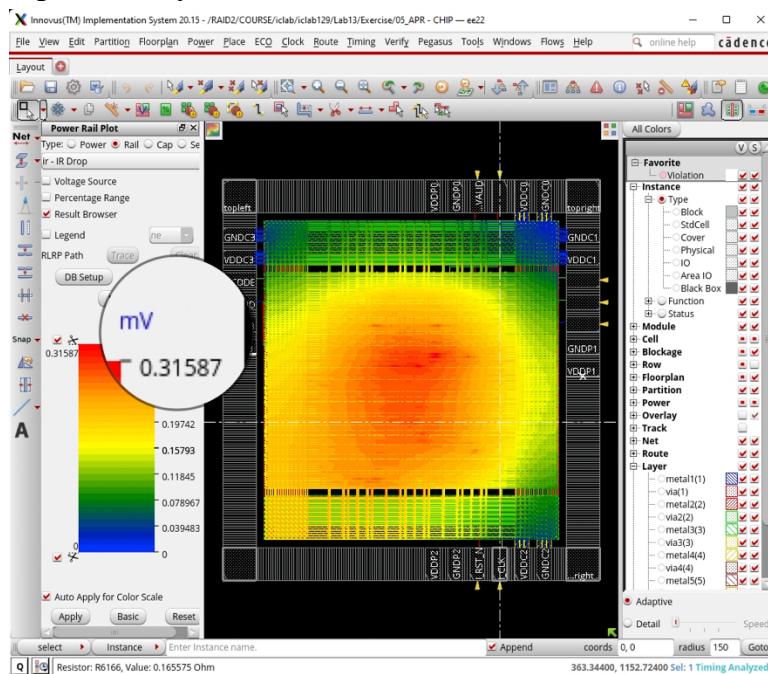
## 8. Power result:

Total Power		
Total Internal Power:	2.31560061	49.1780%
Total Switching Power:	2.39270607	50.8156%
Total Leakage Power:	0.00030072	0.0064%
Total Power:	4.70860740	

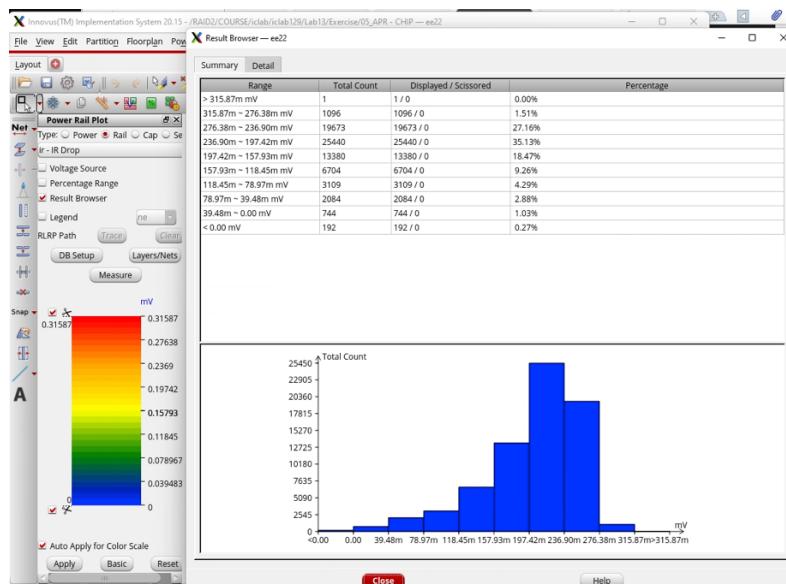
## 9. IR Drop Results:

IR drop Highest value is **0.31587mV** which is larger than 2mV

### IR drop summary:



### IR drop distribution:



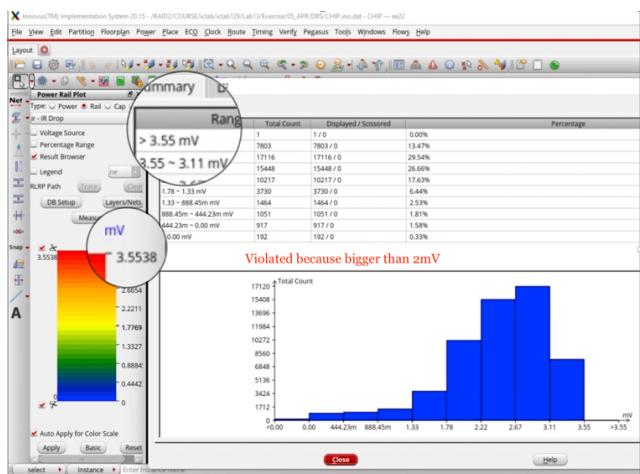
## How did I solve the IR drop problem and stay within the limit of 2mV?

**Ans:** Ensuring that the IR drop stays within the specified limit of 2 mV involves careful design, selection of components, and specific testing methodologies. Some steps that I took to manage and verify the IR drop are:

I added 12 pairs of power stripes and made sure that each side of the layout gets more than sufficient channels. Next is a 60% reduction in the distance to stripe compared to the previous lab. Which result in a denser distribution.

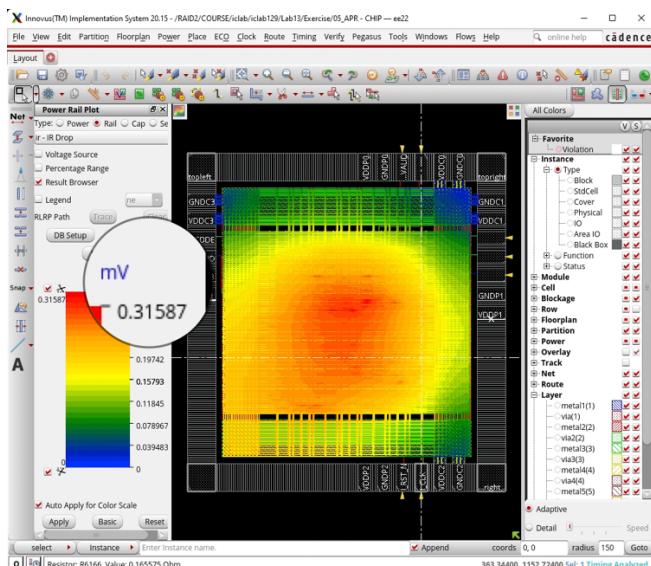
I also ensured that the layout of the circuit minimizes long paths or impedance mismatches that could cause excessive voltage drops. Proper routing and arrangement of components have showed a reduction in IR drops.

### Before



With configuration from previous lab (distance to stripe 100 and only 4 pair of power rings)

### After



(distance to stripe 60 and 10 pairs of power rings)