605.204 - Computer Organization
Module 12: Assignment

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November 20, 2022

Brief Introduction

This assignment involves the implementation of several digital circuits within various Logisim circuits. All of my resulting work can be found at this *GitHub link* and can be cloned and viewed using the following commands:

```
git clone https://github.com/nhinke/computer-organization-repo.git
cd computer-organization-repo/assignments/module12/
```

Problem 1

1. Change the 4-bit adder circuit to be an 8-bit adder in Logisim (double the size of the values that can be added).

Half Adder:

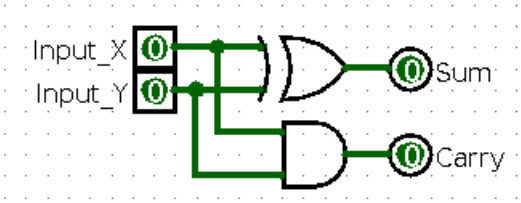

Figure 1: Screenshot of half adder circuit used within full adder circuit

Full Adder:

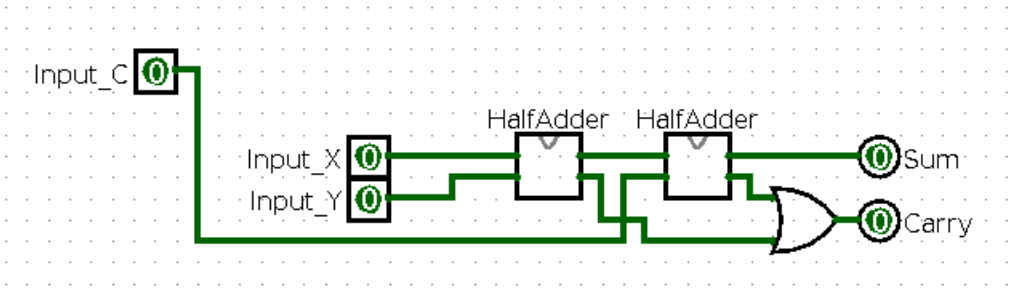

Figure 2: Screenshot of full adder circuit used within 8-bit adder/subtractor circuit

Full 8-bit adder/subtractor circuit is shown on the following page...

8-bit Adder/Subtractor:

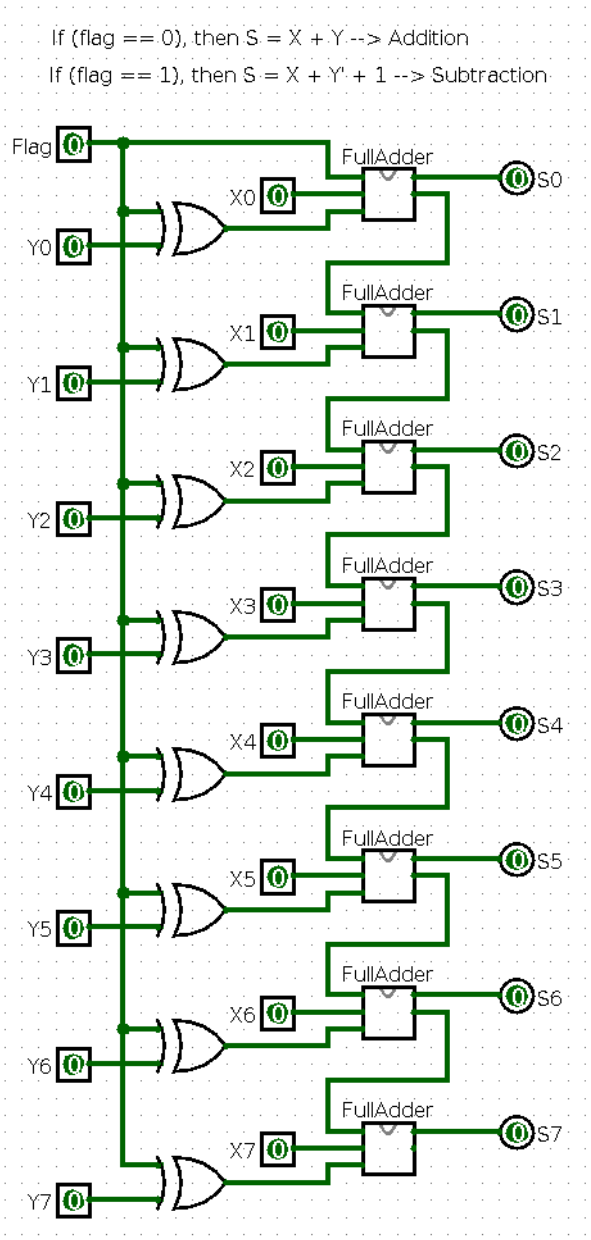

Figure 3: Screenshot of 8-bit adder/subtractor circuit

Problem 2

2. Implement the 1-bit adder using a decoder circuit. Modify this adder to be a 4-bit adder using the Ripple-Carry Adder as a template.

Full Adder (Decoder):

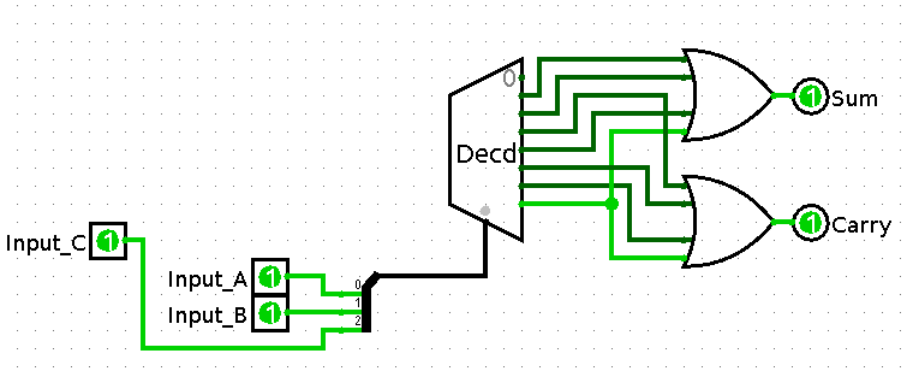

Figure 4: Screenshot of full adder circuit used within 4-bit adder/subtractor circuit

Full 4-bit adder/subtractor circuit is shown on the following page...

4-bit Adder/Subtractor (Decoder):

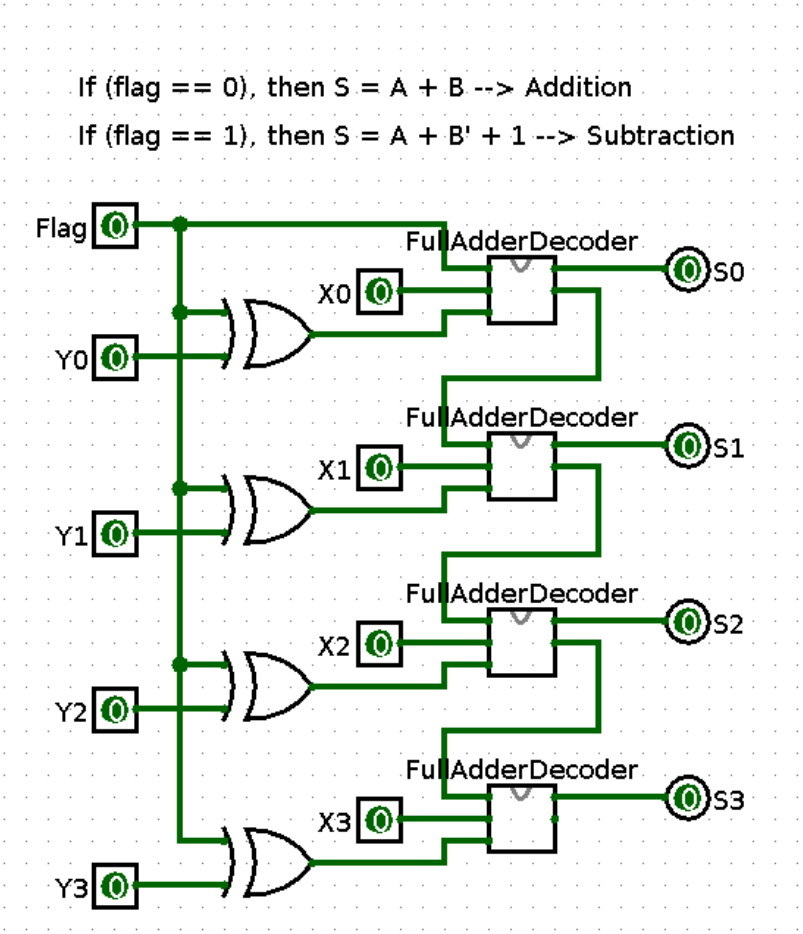

Figure 5: Screenshot of 4-bit adder/subtractor circuit

Problem 3

3. Implement a multiplexor which has a data width of 8 bits and 2 select bits (2 select bits means this multiplexor will have 4 input value, each of 8 bits). The 8 bit inputs should contain the values of 8 , 16, 32, and 64. Change the input select bits between 00-11 so that the value cycles 8, 16, 32, 64, 8, 16, 32, 64, etc.

4-to-1 8-bit Multiplexor:

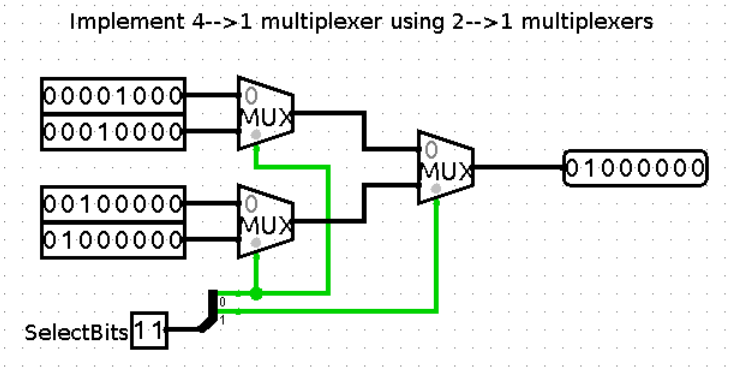

Figure 6: Screenshot of 4-to-1 8-bit multiplexor

Problem 4

4. Implement a 16-to-1 8-bit multiplexor using any combination 4-to-1 and 2-to-1 multiplexors. You will get the maximum points if you use the fewest multiplexers.

16-to-1 8-bit Multiplexor:

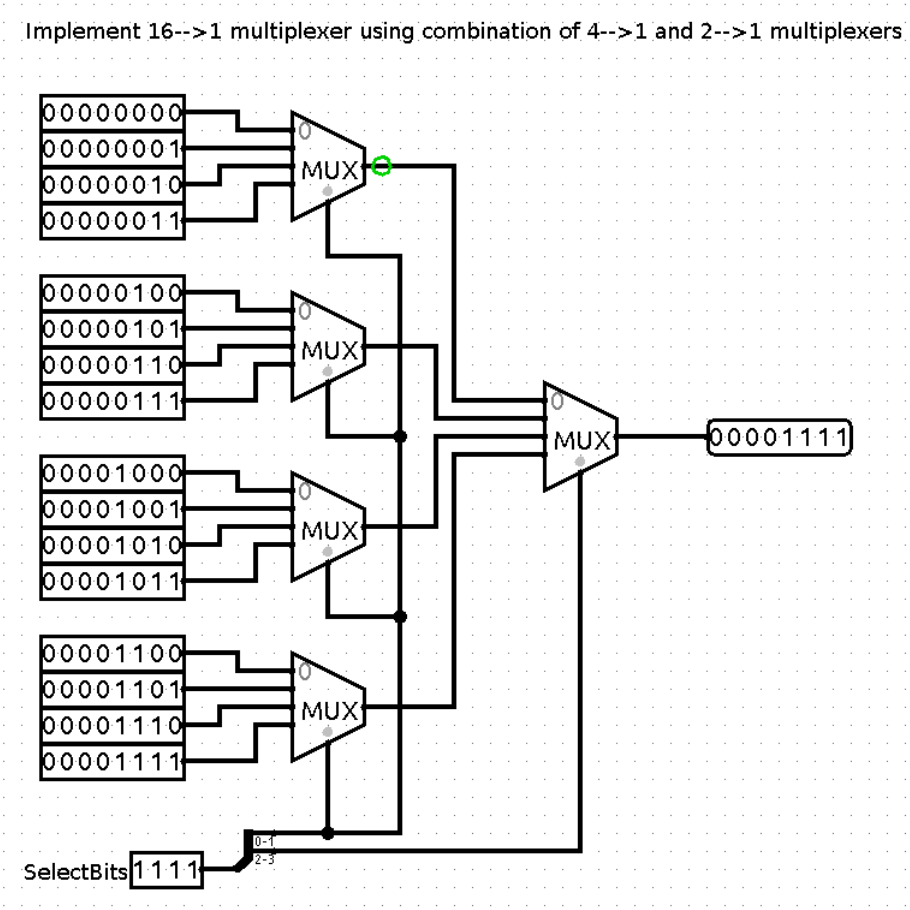

Figure 7: Screenshot of 16-to-1 8-bit multiplexor