Assignment 1

The following figure lists the format for each instruction of our simplified computer.

	Operation	Unused	Unused	Unused	Unused						
Halt	0 0 0 0										
	Halt										
					-						
	Operation	Reg A	Reg B	Reg C	Unused						
Add											
	Add RC, RA, RB	RC	C ← RA + RB								
	Operation	Reg A	Unused	Peg C	Offset						
Load		Keg A	Olluseu	Neg C							
Loud		ffset RC	← MEM(RA + o	ffset)							
	2022 110, 121		(,							
	Operation	Reg A	Reg B	Unused	Offset						
Store	0 0 1 1										
	Store RA + Offse	ration Reg A Reg B Reg C Unused 0 0 1 <td></td>									
	Operation	RC ← RA + RB Reg A Unused Reg C Offset Fiset RC ← MEM(RA + offset) Reg A Reg B Unused Offset t, RB MEM(RA + Offset) ← RB Reg A Unused Unused Offset t Program Counter ← RA + Offset Unused Unused Reg C Value RC ← Value									
Jump											
	Jump RA + Offse	et Pr	ogram Counter	← RA + Offset							
	Operation	Unused	Unused	Reg C	Value						
Mov	 										
	Mov RC, value	R	: : : C ← Value								
	Operation	Unused	Reg B	Reg C	Unused						
Mov	0 1 1 0										
	Mov RC, RB	R	C ← RB								

Translate the following programs into instructions stored in memory (in hexadecimal format).

• Program test 1

mov r1, 1	r1 <- 1	500101
mov r2, 2		500202
mov r3, r2		602300
add r3, r1, r2		112300
halt		000000

• Program test 2: mov, load

mov r5, 1	500501
load r6, r5 + 4	250604

• Program test 3: mov, store, load

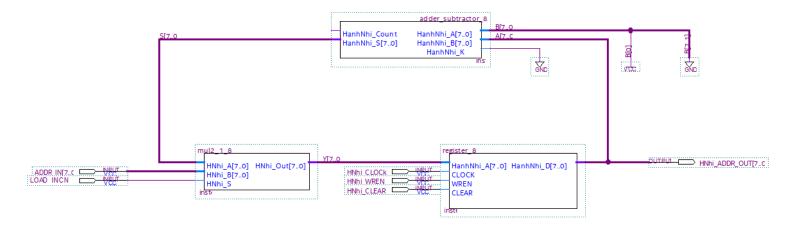
mov r5, 1	500501
mov r6, FF	5006FF
store r5 + 4, r6	356004
load r7, r5 + 4	250704
halt	000000

• Program test 4: jump

Address 0: Mov r4, 7	500407
Address 1: Jump r4 + 3	440003
Address 2: add r3, r1, r2	112300
Address 3: halt	000000
Address 10: Mov r1, 1	500101
Address 11: Mov r2, 2	500202
Address 12: Mov r5, 1	500501
Address 13: Jump r5 + 1	450001

Assignment 2

1. Design the logic diagram to implement the program counter.

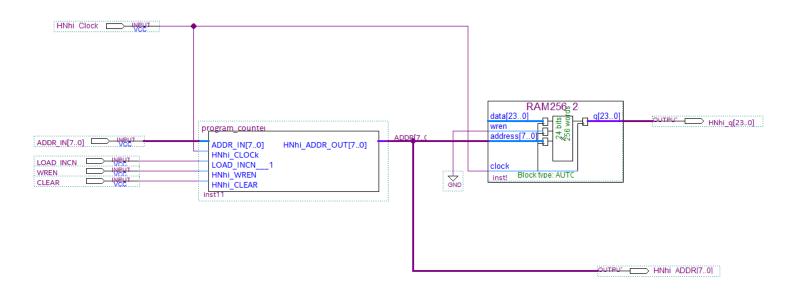


2. Simulate the circuit and check the result.

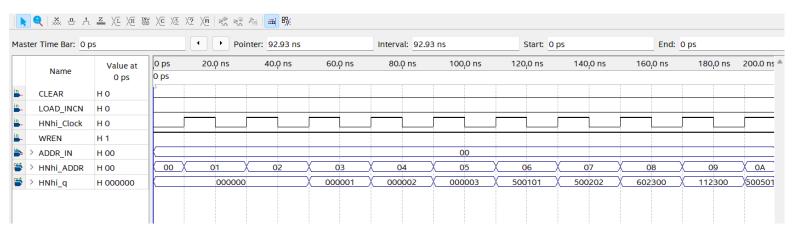
No.	ame Val	ue at	0 ps	2	0.0 ns	40.	0 ns	60.0 n	5	80.0 ns		100 _: 0 ns	120	0 ns	140,0	ns	160.0	ns	180 _, 0	ns 200.0 ns
IN C	0) ps	0 ps																	
놀 > AI	DDR U 0			0	X	20			0		50					0				
in_ LO	DAD B 0																			
in H	Nhi B 0																			
in H	Nhi B 0										-									
<u>i</u> HI	Nhi B 1																			
🛎 > н	Nhi U 0		0	Х	1	X 2	0	21		22		50	5	1	52	X	53	X	54	55

Assignment 3

1. Design the logic diagram to implement the program counter.

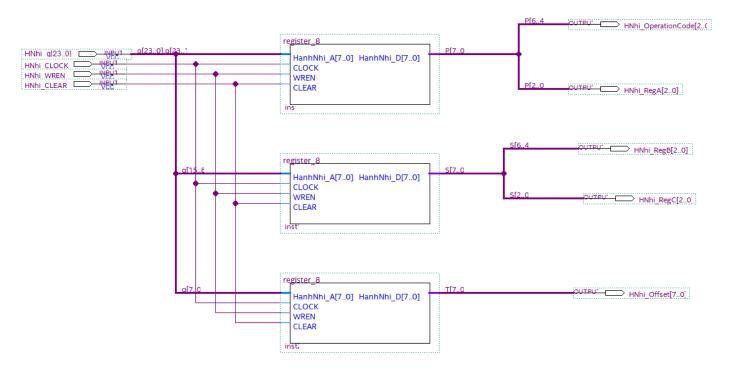


2. Simulate the circuit and check the result.

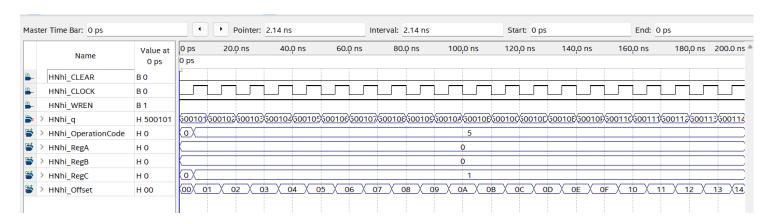


Assignment 4

1. Design the logic diagram to implement the program counter.

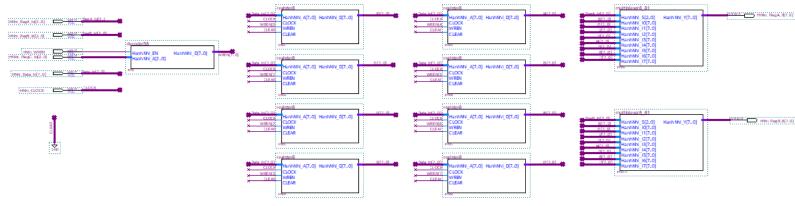


2. Simulate the circuit and check the result.



Assignment 5

1. Design the logic diagram to implement the program counter.



2. Simulate the circuit and check the result.

