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MSSV: 2131209002

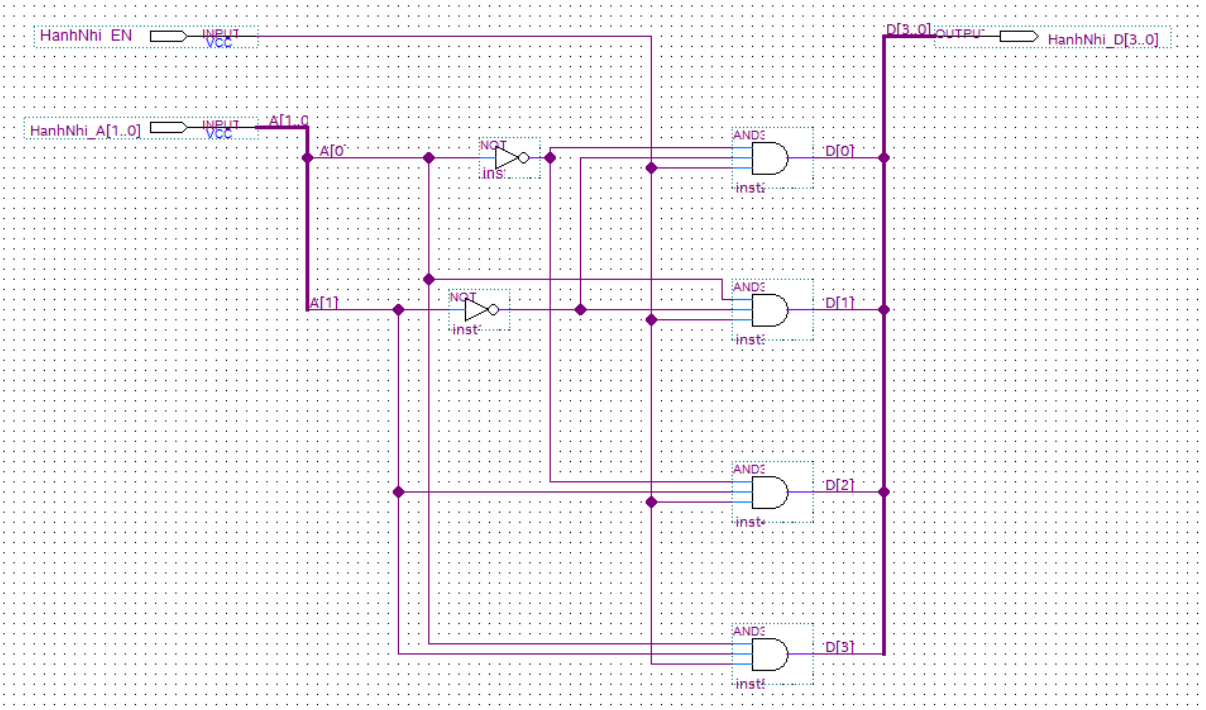
# Assignment 1

## 1. Truth table:

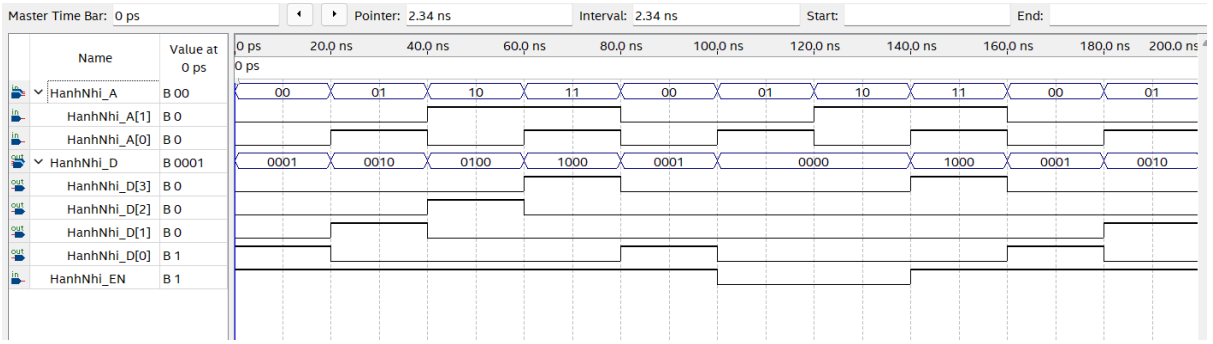
| EN | A1 | A0 | D0 | D1 | D2 | D3 |
|---|---|---|---|---|---|---|
| 0 | x | x | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

## 2. Design the 2-4 decoder's logic diagram:

**D0 = ENA1'A0'**
**D1 = ENA1'A0**
**D2 = ENA1A0'**
**D3 = ENA1A0**
Lines A1, A0: Bus A[1..0]
Lines D3, D2, D1, D0: Bus D[3..0]




## 3. Simulate the circuit:

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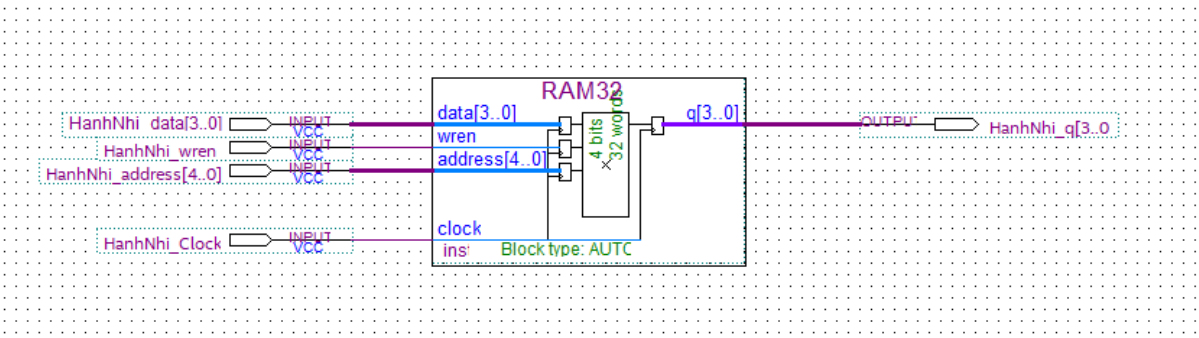
# Assignment 2

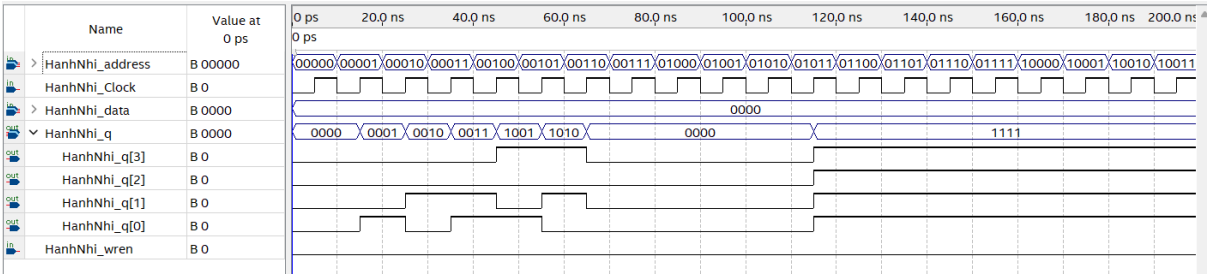
1. **Create the 32-4 RAM (32 by 4):**
2. **Use the RAM32_4:**




3. **We now initialise the memory contents of our RAM:**

| Addr | +0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 | ASCII |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 9 | 10 | 0 | 0 | 0 | ..... |
| 8 | 0 | 0 | 15 | 15 | 15 | 15 | 15 | 15 | ..... |
| 16 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | ..... |
| 24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ..... |

4. **Simulate the circuit:**

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# Assignment 3

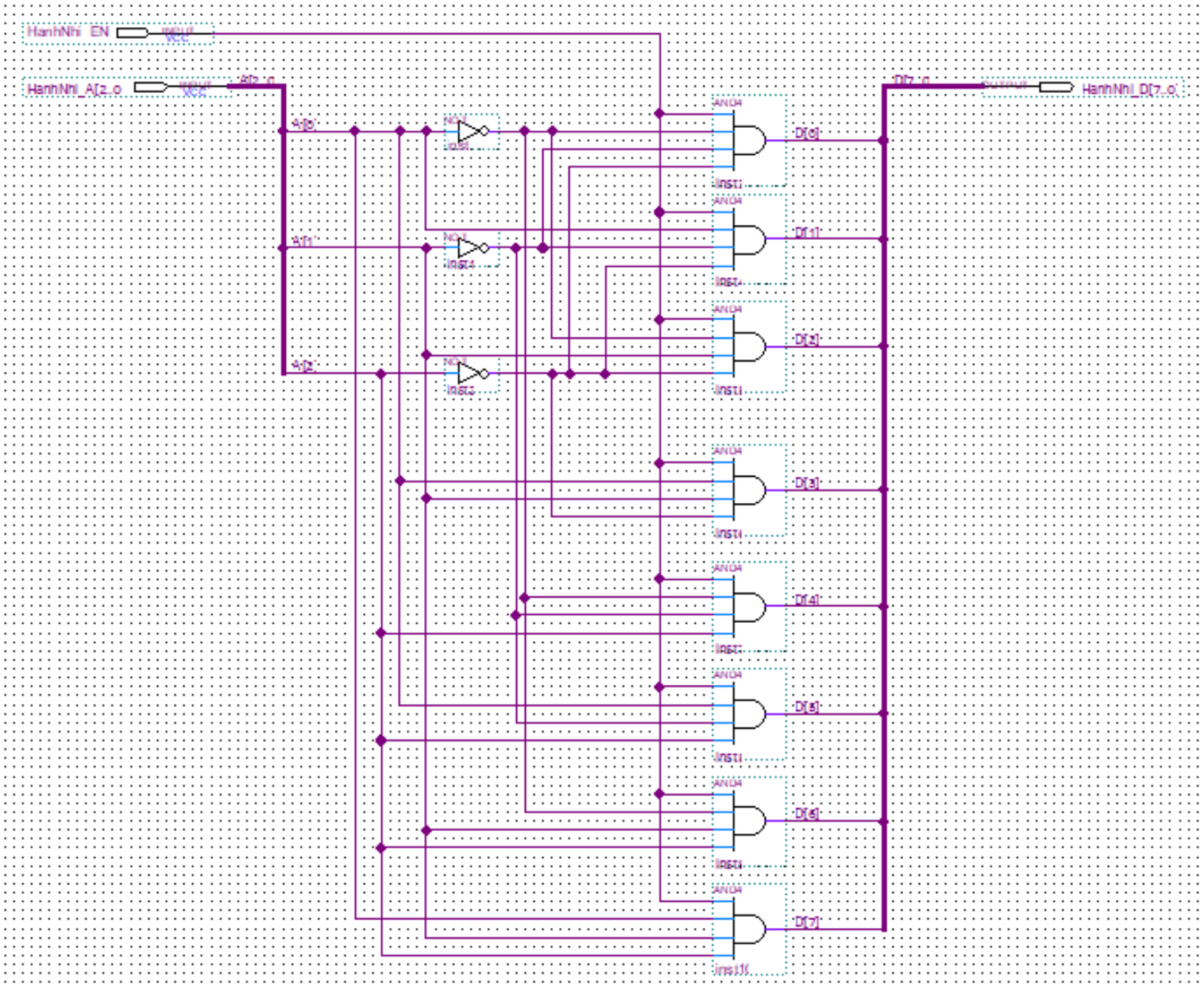
1. **Truth table:**

| EN | A2 | A1 | A0 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

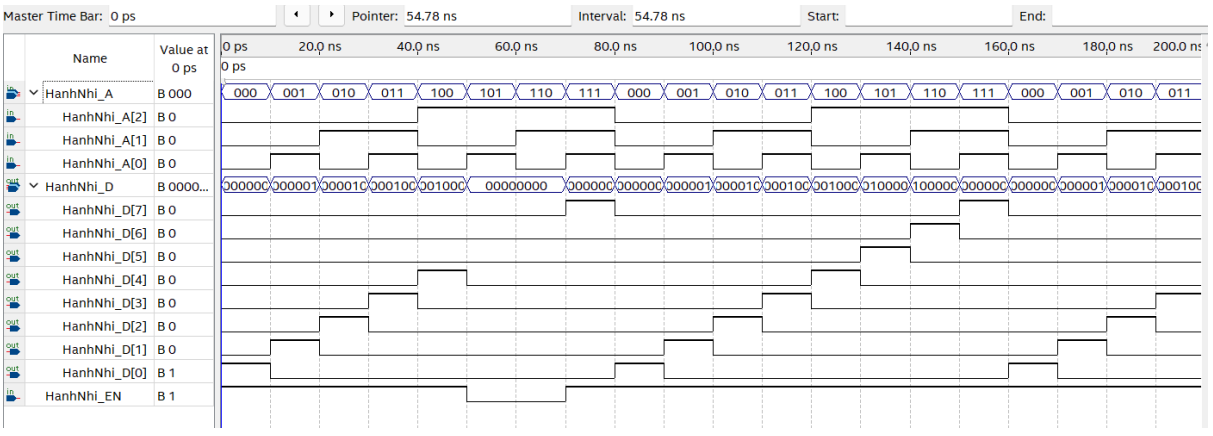
2. **Design the 3 - 8 decoder's logic diagram:**

**D0 = ENA2'A1'A0'**
**D1 = ENA2'A1'A0**
**D2 = ENA2'A1A0'**
**D3 = ENA2'A1A0**
**D4 = ENA2A1'A0'**
**D5 = ENA2A1'A0**
**D6 = ENA2A1A0'**
**D7 = ENA2A1A0**

Lines A2, A1, A0: Bus A[2..0]
Lines D7, D6, D5, D4, D3, D2, D1, D0: Bus D[7..0]

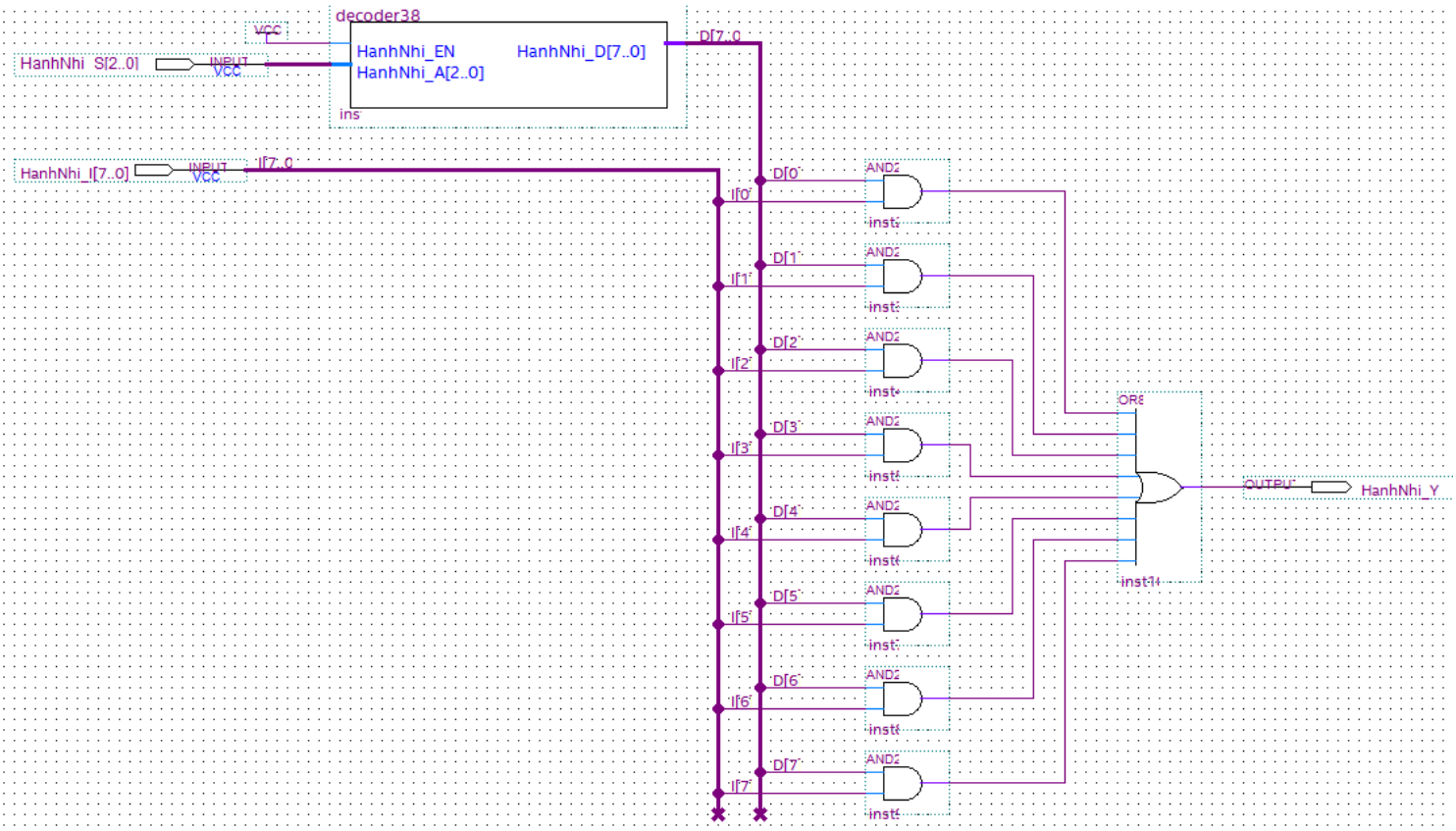



## 3. Simulate the circuit:

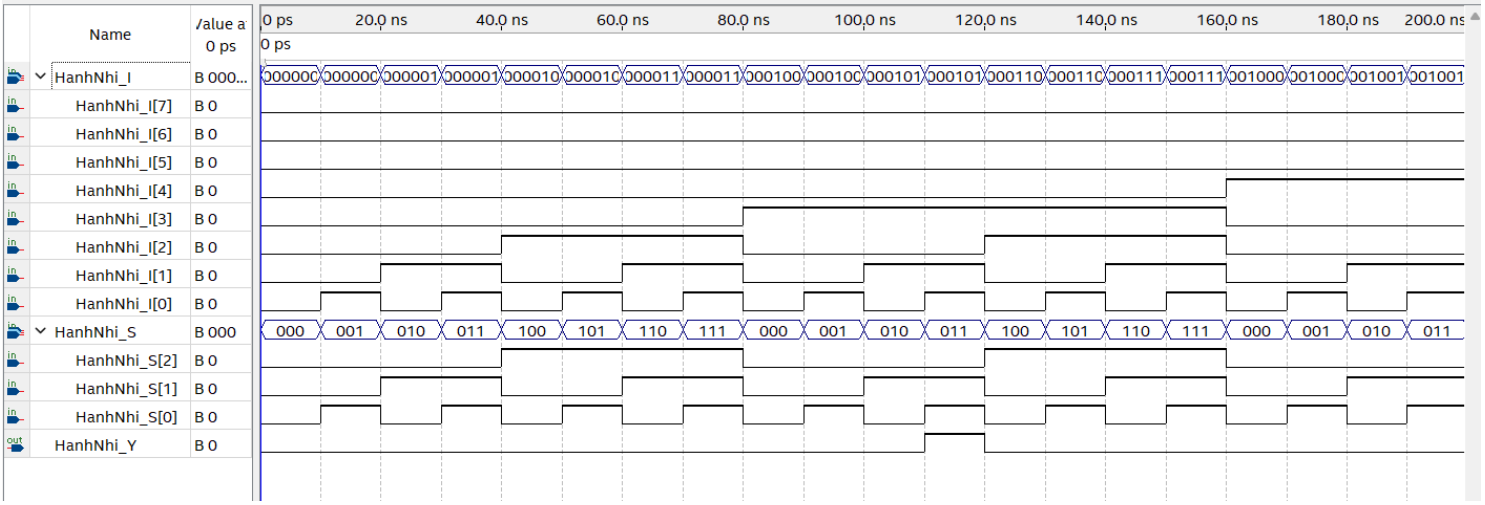


# Assignment 4

## 1. Design the 1-bit 8-1 multiplexer's logic diagram:




## 2. Simulate the circuit:

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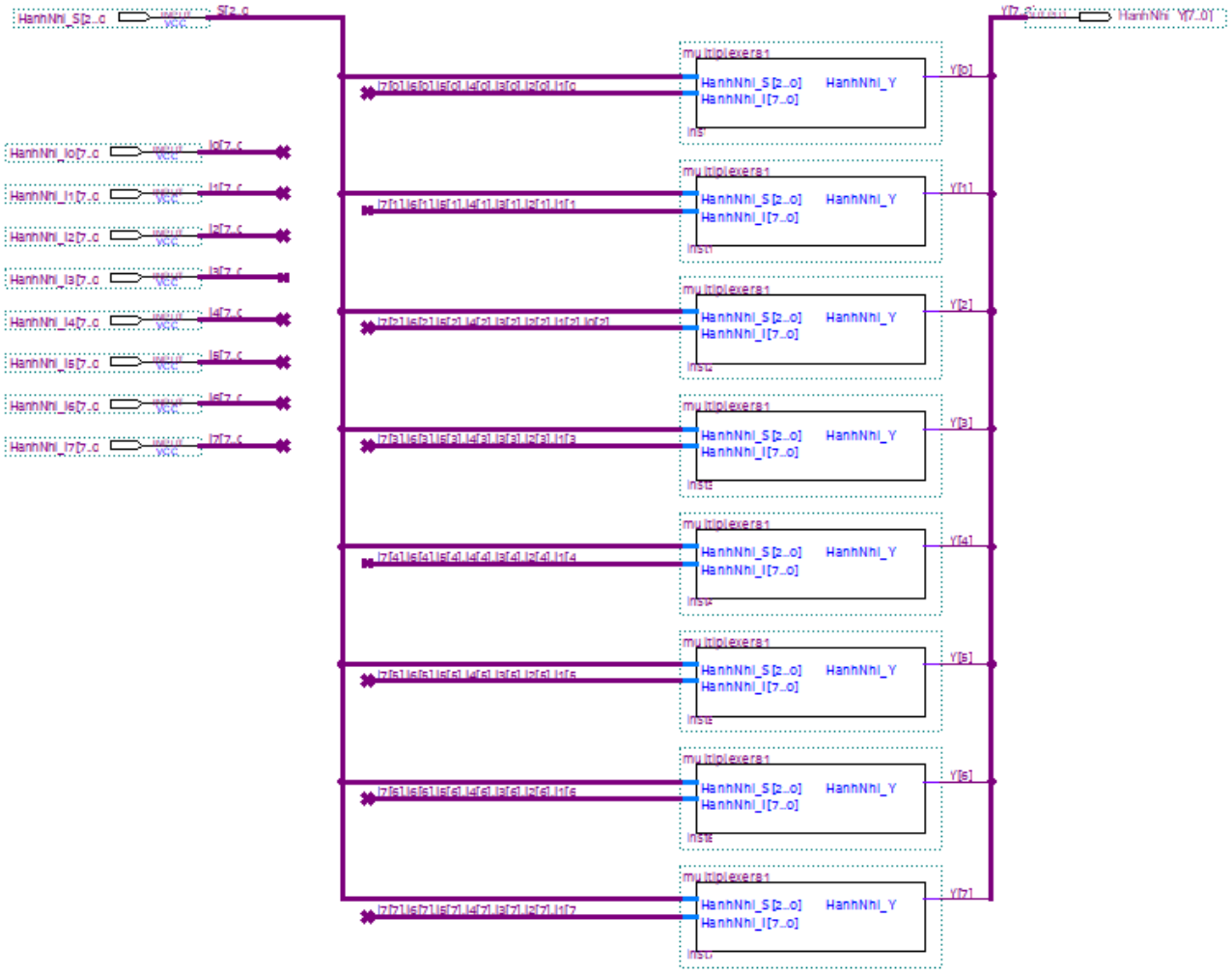
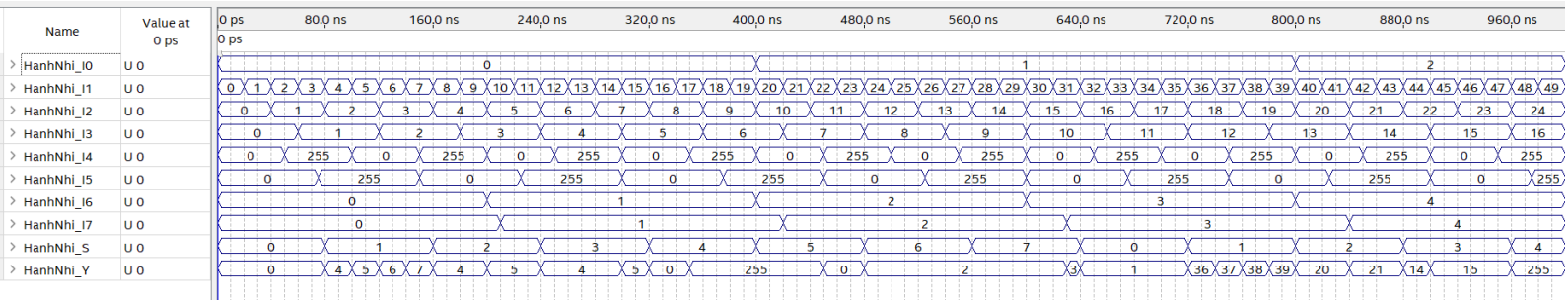
# Assignment 5

## 1. Design a logic diagram to implement 8-bit 8-1 multiplexer:




## 2. Simulate the circuit:

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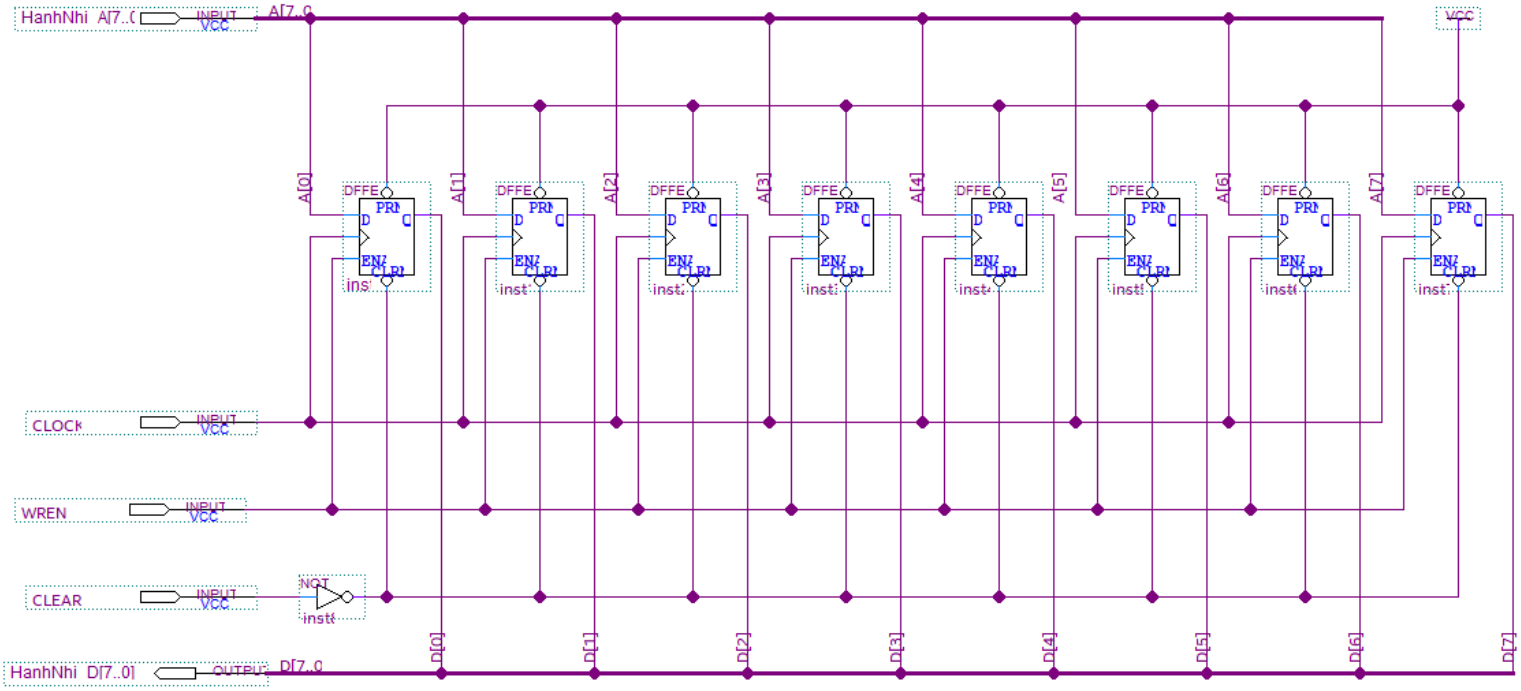
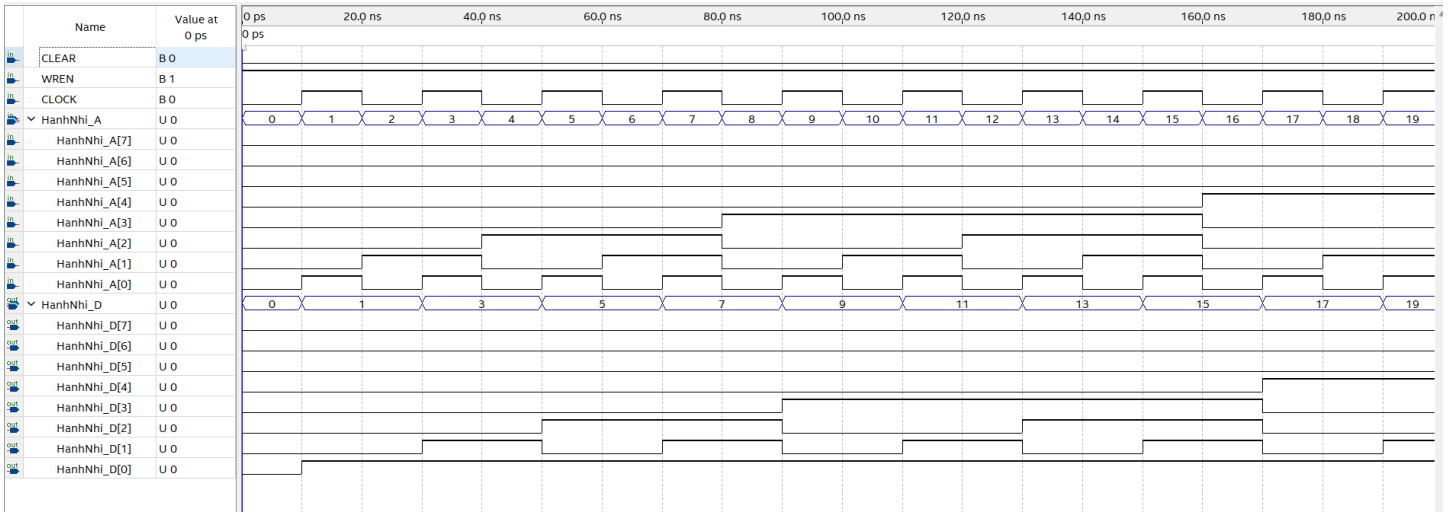
# Assignment 6

## 1. Design the logic diagram of the register:




## 2. Simulate the circuit:

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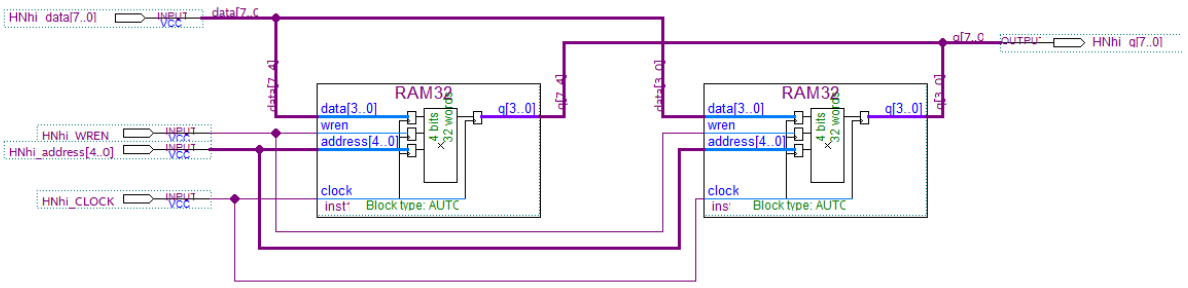
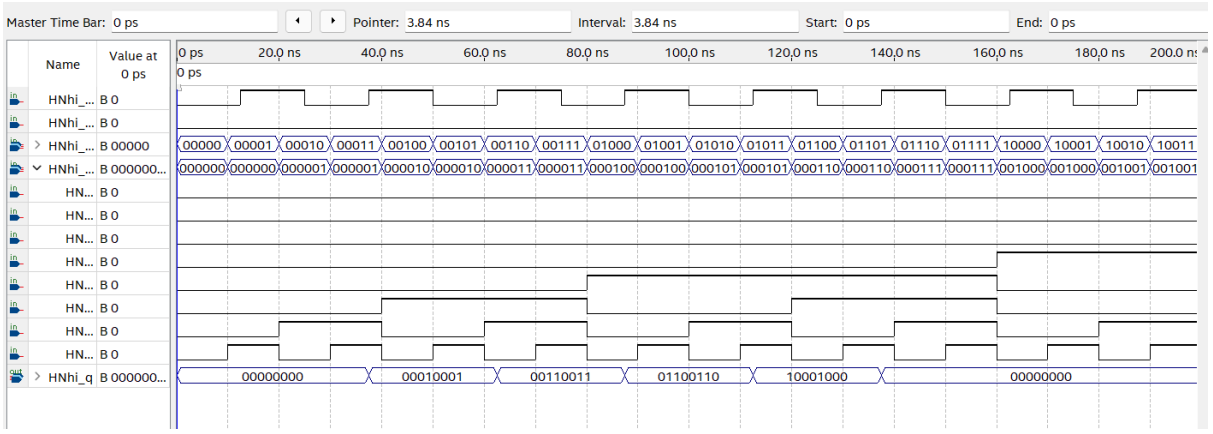
# Assignment 7

## 1. Design a logic diagram of a 32 x 8 RAM using two 32 x 4 RAM chips:



## 2. Simulate the circuit:

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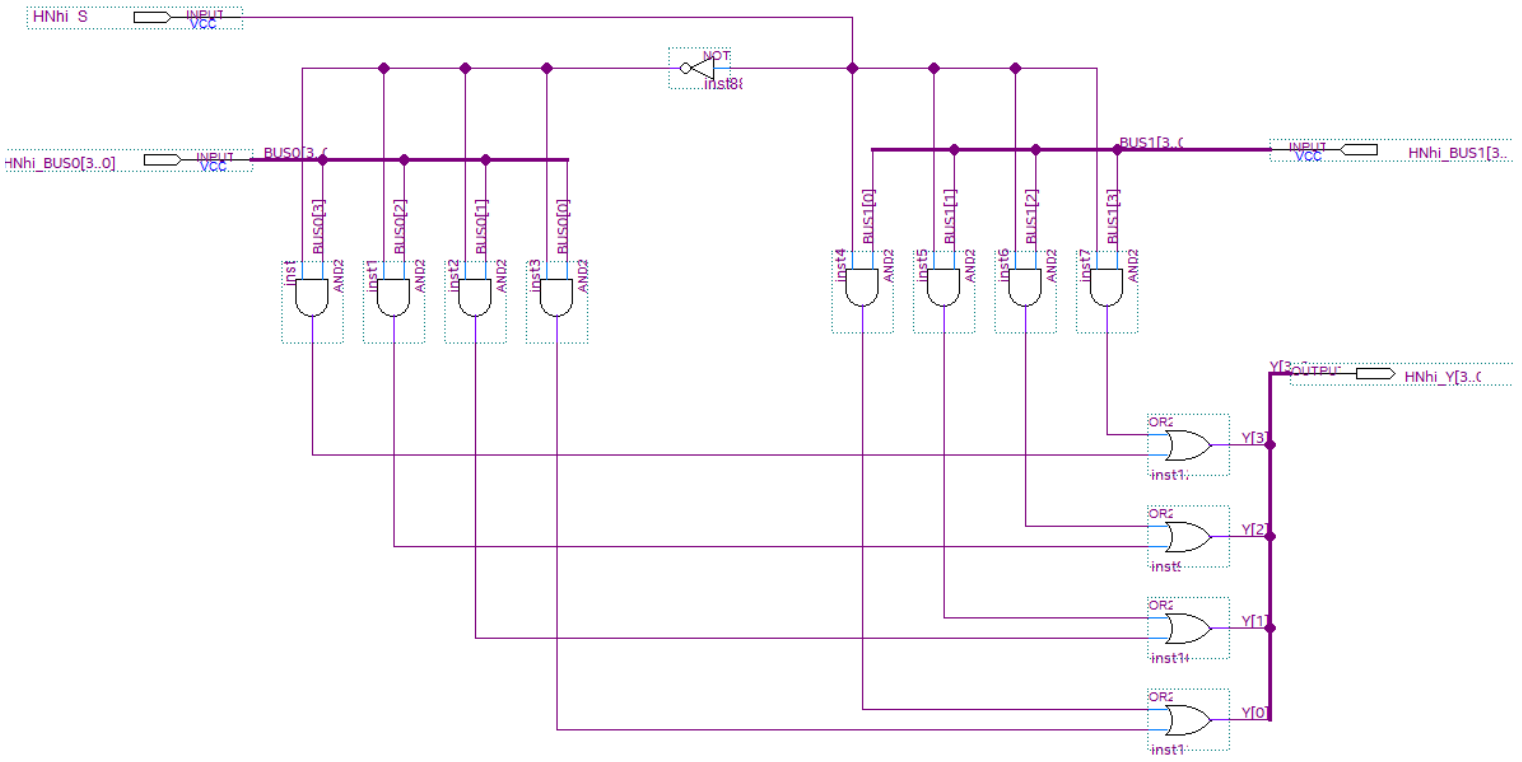
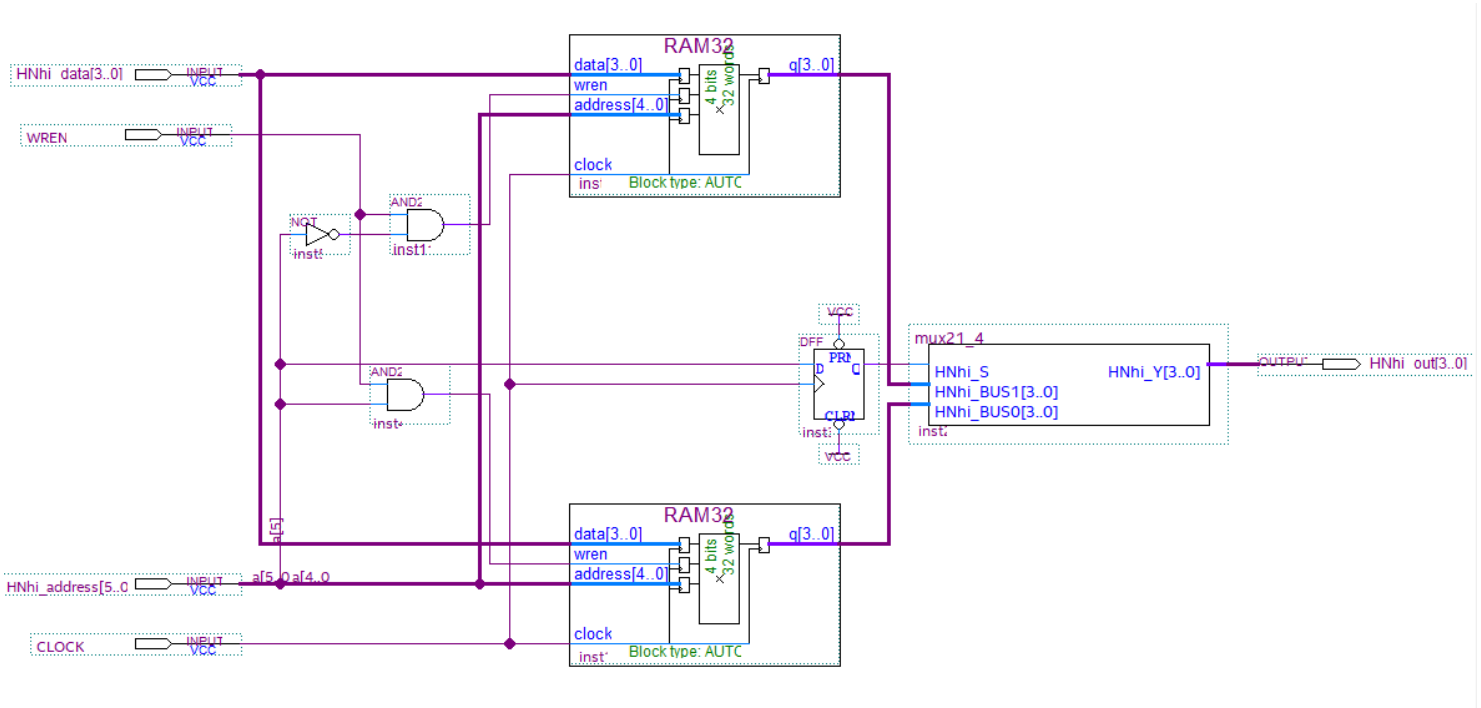
# Assignment 8

## 1. Design a logic diagram of a 64 x 4 RAM using two 32 x 4 RAM chips:

- **Mux21_4:**




- Logic diagram of a 64 x 4 RAM using two 32 x 4 RAM chips




## 2. Simulate the circuit: