Chapter 6
Memory Basics

M. Morris Mano, Charles R. Kime. (2015). *Logic and computer design fundamentals* (5th ed.). Pearson.

Contents

1. Memory Definitions
2. Random-Access Memory
3. SRAM Integrated Circuits
4. Array of SRAM ICs
5. DRAM ICs

1. Memory Definitions

- In digital systems, memory is a collection of cells capable of storing binary information. In addition to these cells, memory contains electronic circuits for storing and retrieving the information.
- Two types of memories are used in various parts of a computer: *random-access memory* (RAM) and *read-only memory* (ROM).
- RAM accepts new information for storage to be available later for use. The process of storing new information in memory is referred to as a *memory write* operation. The process of transferring the stored information out of memory is referred to as a *memory read* operation. RAM can perform both the write and the read operations, whereas ROM performs only read operations.
- RAM sizes may range from hundreds to billions of bits.

2. Random-Access Memory

- Memory is a collection of binary storage cells together with associated circuits needed to transfer information into and out of the cells.
- Memory cells can be accessed to transfer information to or from any desired location, with the access taking the same time regardless of the location, hence the name *random-access memory*.
- Binary information is stored in memory in groups of bits, each group of which is called a *word*.
  - A word is an entity of bits that moves in and out of memory as a unit. A group of eight bits is called a *byte*. Most computer memories use words that are multiples of eight bits in length. Thus, a 16-bit word contains two bytes, and a 32-bit word is made up of four bytes.

2. Random-Access Memory

- The address lines select one particular word. Each word in memory is assigned an identification number called an *address*.
  - Addresses range from 0 to 2^k - 1, where k is the number of address lines.

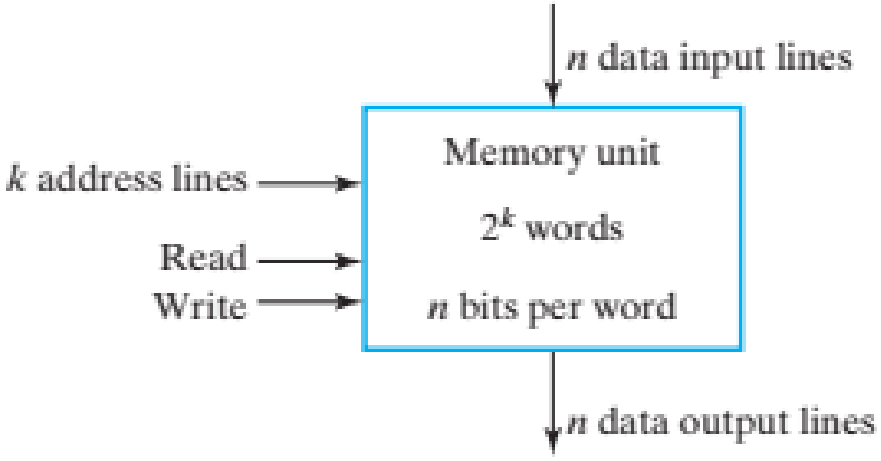


FIGURE 7-1
Block Diagram of Memory

Memory Address		Memory Contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

FIGURE 7-2
Contents of a 1024 × 16 Memory

Write and Read Operations

- A *write* is a transfer into memory of a new word to be stored.
- A *read* is a transfer of a copy of a stored word out of memory.
- The steps that must be taken for a write are as follows:
  1. Apply the binary address of the desired word to the address lines.
  2. Apply the data bits that must be stored in memory to the data input lines.
  3. Activate the Write input.
- The steps that must be taken for a read are as follows:
  1. Apply the binary address of the desired word to the address lines.
  2. Activate the Read input.

Write and Read Operations

- Memory is made up of RAM integrated circuits (chips), plus additional logic circuits.

The Chip Select is used to enable the particular RAM chip or chips containing the word to be accessed.

+ When Chip Select is inactive, the memory chip or chips are not selected, and no operation is performed.

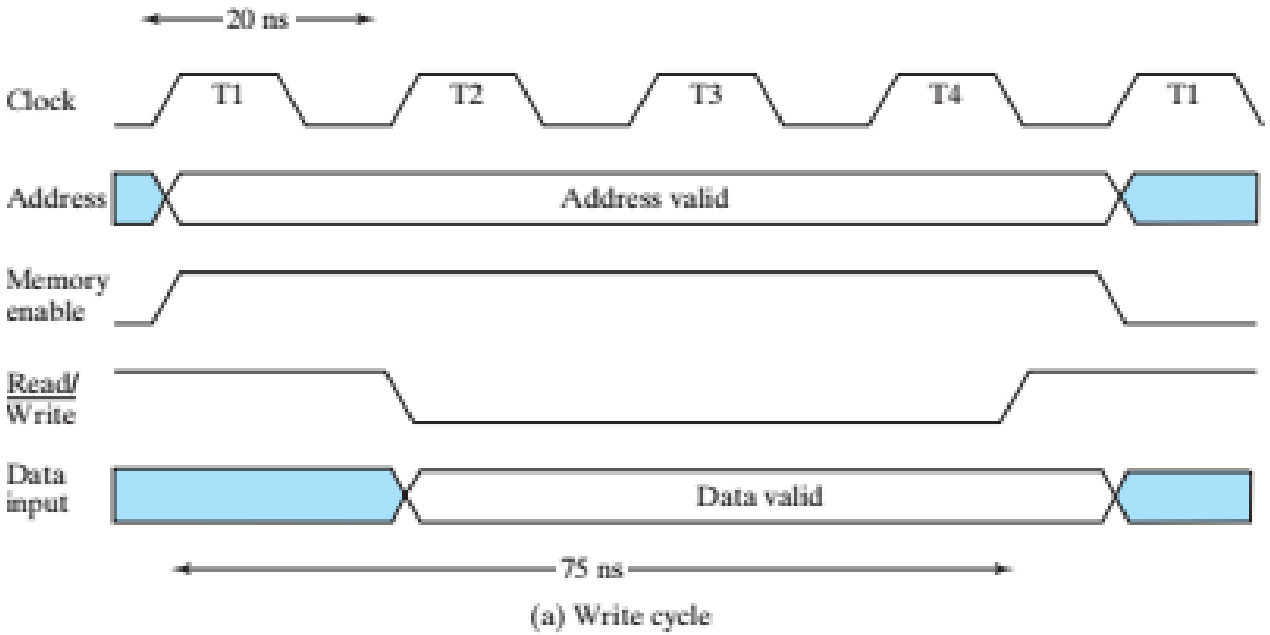
+ When Chip Select is active, the Read/Write input determines the operation to be performed. (Memory Enable)

TABLE 7-1
Control Inputs to a Memory Chip

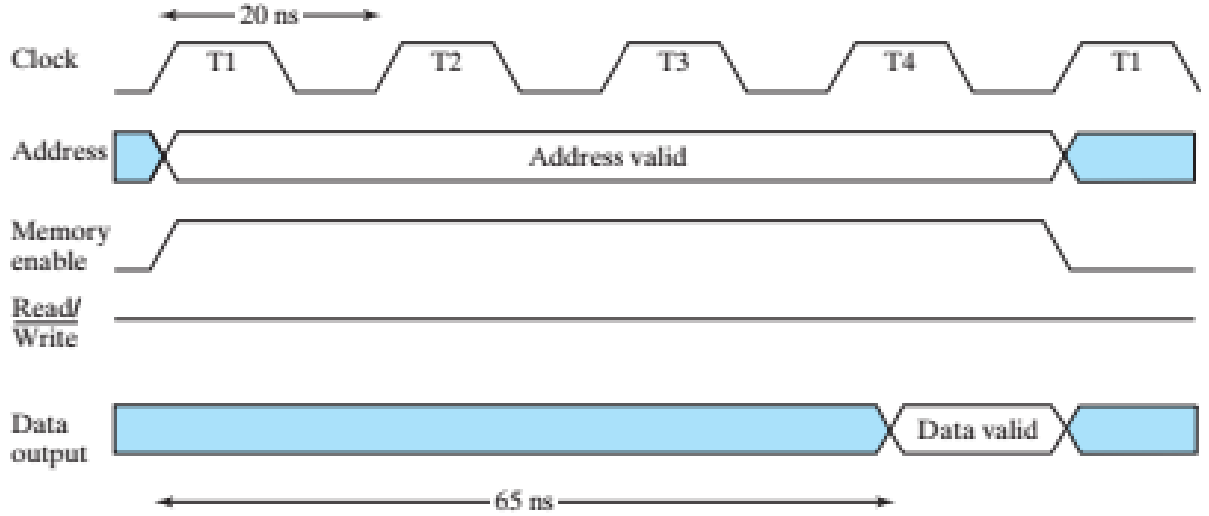
Chip Select CS	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	Memory Operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

Write and Read Operations

- Memory Cycle Timing Diagram



(a) Write cycle



(b) Read cycle

Properties of Memory

- Integrated-circuit RAM may be either *static* or *dynamic*.
- *Static* RAM (SRAM) consists of internal latches that store the binary information.
  - The stored information remains valid as long as power is applied to the RAM.
- *Dynamic* RAM (DRAM) stores the binary information in the form of electric charges on capacitors. The capacitors are accessed inside the chip by *n*-channel MOS transistors.
  - The stored charge on the capacitors tends to discharge with time, and the capacitors must be periodically recharged by refreshing the DRAM. This is done by cycling through the words every few milliseconds, reading and rewriting them to restore the decaying charge.
- DRAM offers reduced power consumption and larger storage capacity in a single memory chip, but SRAM is easier to use and has shorter read and write cycles. Also, no refresh is required for SRAM.

Properties of Memory

- *Volatile* memory: Loses stored information when power is turned off
  - Both static and dynamic memories are of volatile memory.
- *Nonvolatile* memory: Retains its stored information after the removal of power.
  - Magnetic disk
  - ROM

3. SRAM Integrated Circuits

- The *RAM cell* is the basic binary storage cell used in the RAM chip.
  - Stores a single bit
  - Used in a hierarchy to describe the RAM chip
- Static RAM Cell
  - Modeled by an SR latch
  - Enabled by *Select* input
  - Input B, B′: Content to be stored
  - Output C, C′: Stored value

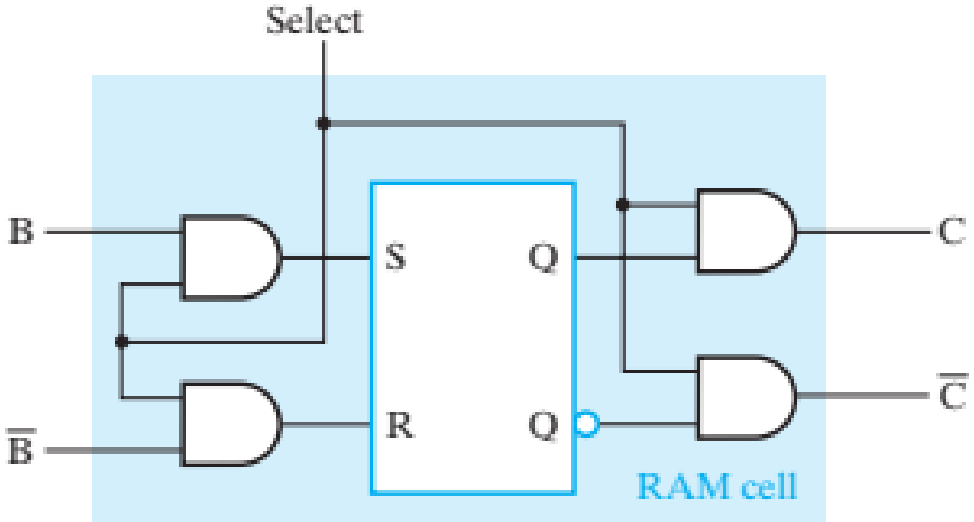


FIGURE 7-4
Static RAM Cell

SRAM Integrated Circuits

- RAM *bit slice*: contains all of the circuitry associated with a single bit position of a set of RAM words.

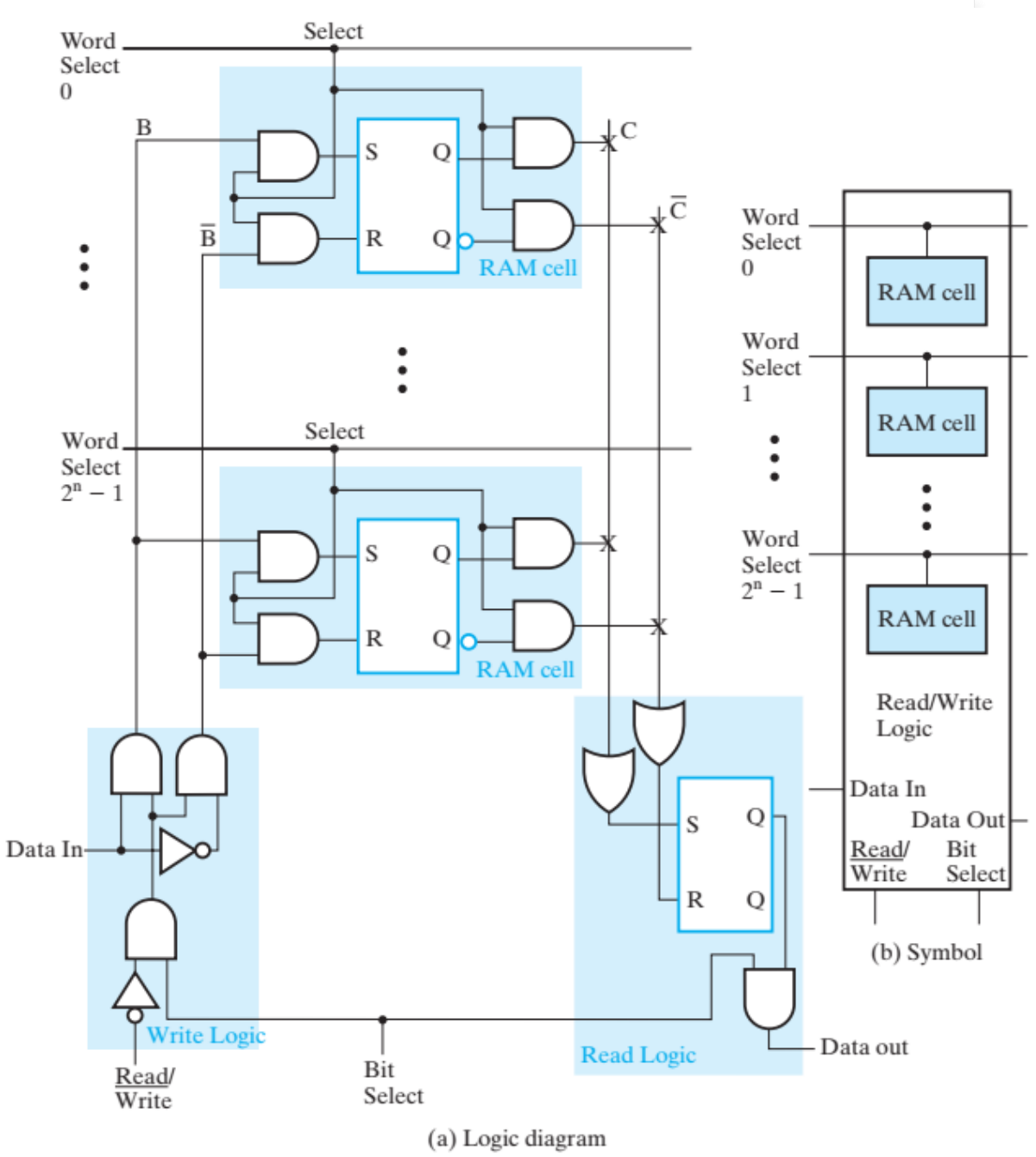
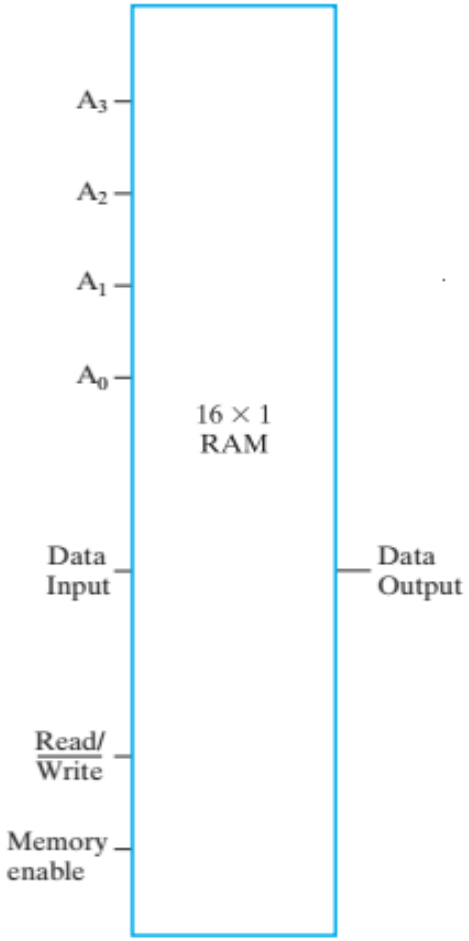
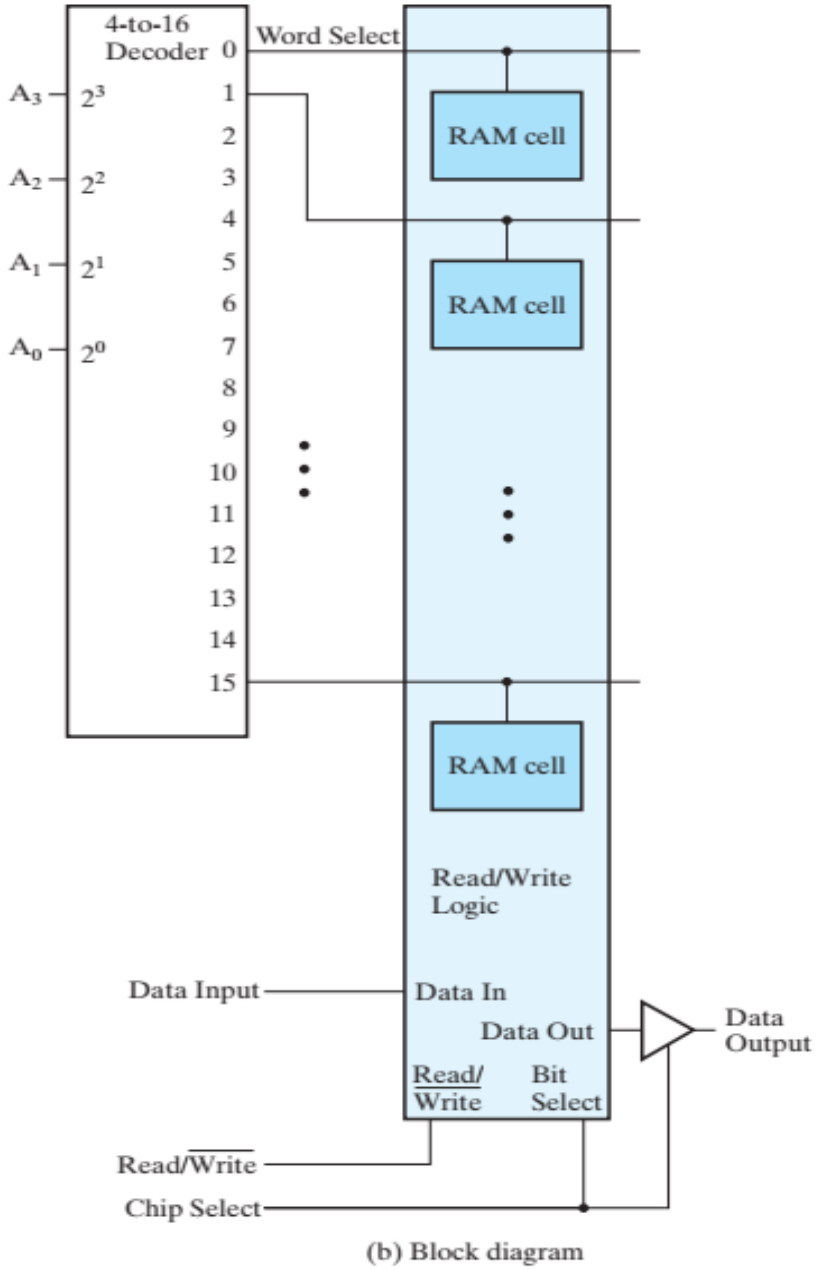


FIGURE 7-5
RAM Bit Slice Model

SRAM Integrated Circuits



(a) Symbol



(b) Block diagram

FIGURE 7-6
16-Word by 1-Bit RAM Chip

SRAM Integrated Circuits

- Inside a RAM chip, the decoder with k inputs and 2^k outputs requires 2^k AND gates with k inputs per gate if a straightforward design approach is used.
- If the number of words is large, and all bits for one bit position in the word are contained in a single RAM bit slice, the number of RAM cells sharing the read and write circuits is also large. The electrical properties resulting from both of these situations cause the access and write cycle times of the RAM to become long, which is undesirable.

SRAM Integrated Circuits

- Coincident Selection
  - Two *k*/2-input decoders are used

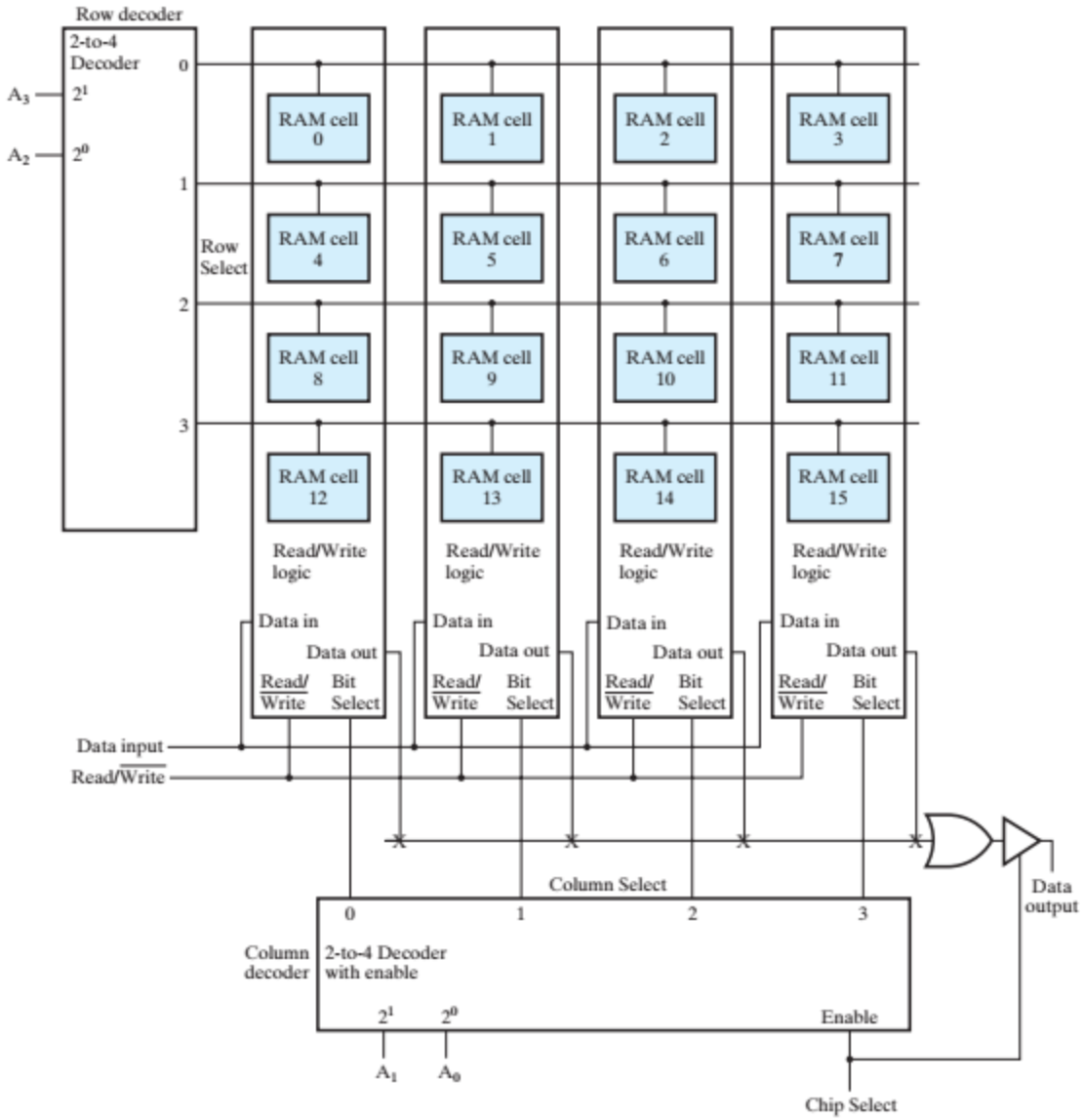


FIGURE 7-7
Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array

SRAM Integrated Circuits

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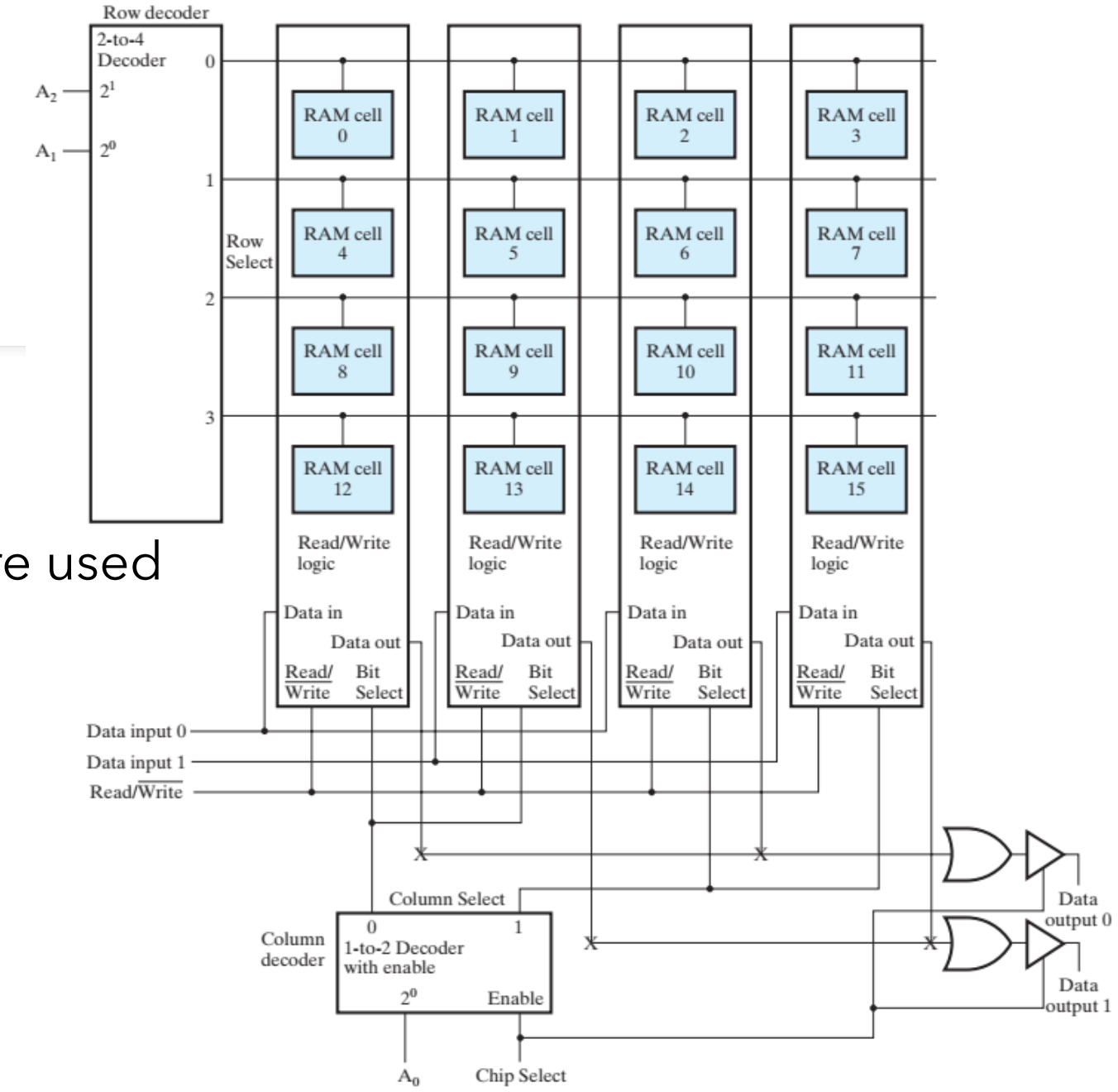

FIGURE 7-8
Block Diagram of an 8 × 2 RAM Using a 4 × 4 RAM Cell Array

4. Array of SRAM ICs

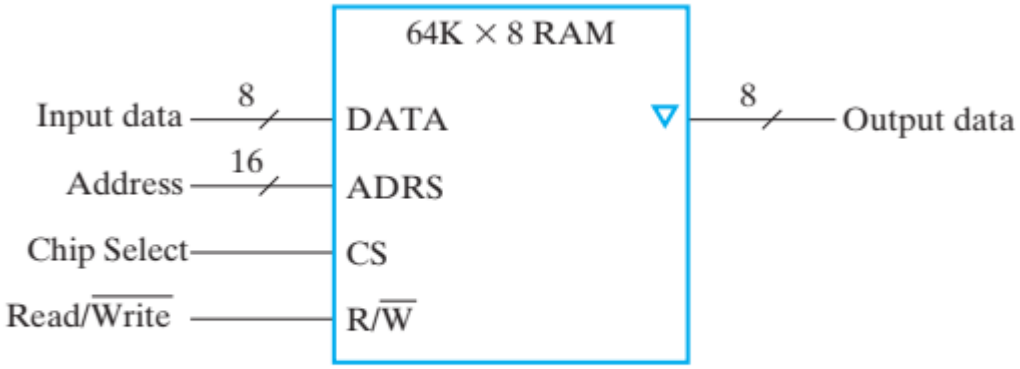

FIGURE 7-9
Symbol for a 64K × 8 RAM Chip

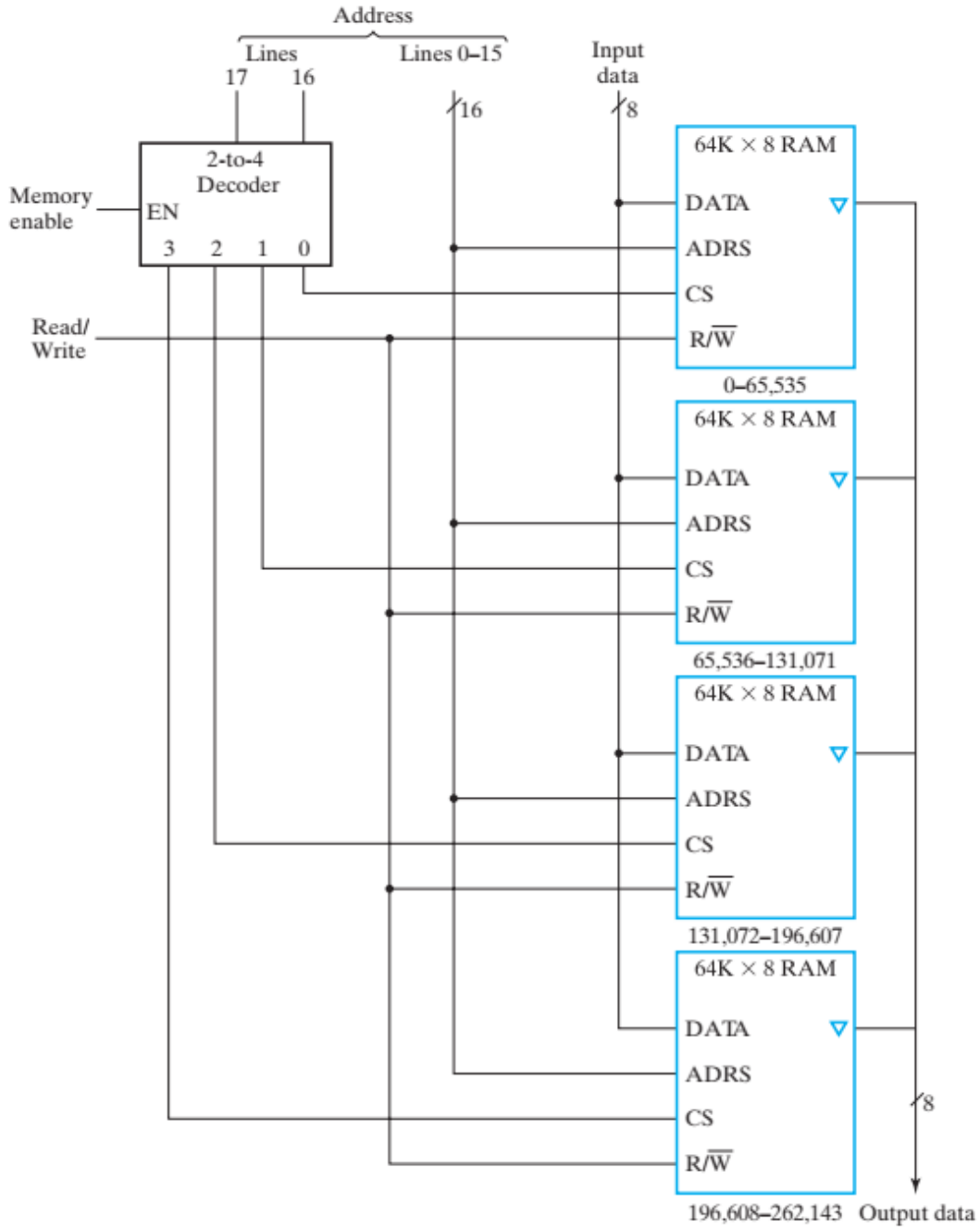

FIGURE 7-10
Block Diagram of a 256K × 8 RAM

4. Array of SRAM ICs

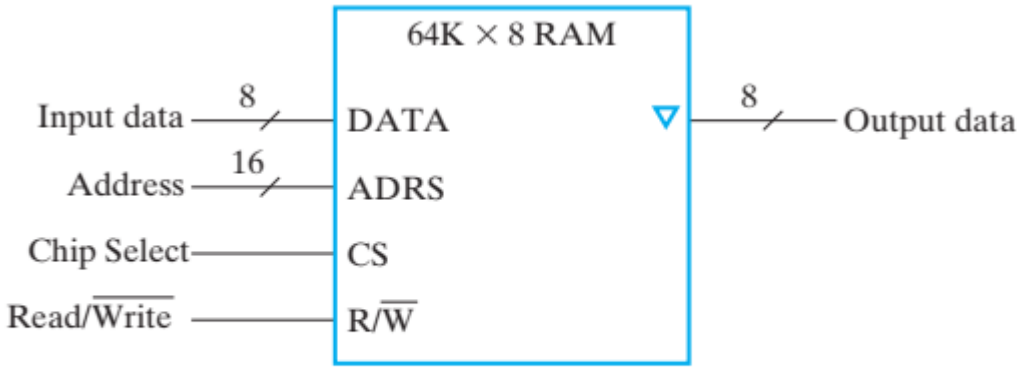

FIGURE 7-9
Symbol for a 64K × 8 RAM Chip

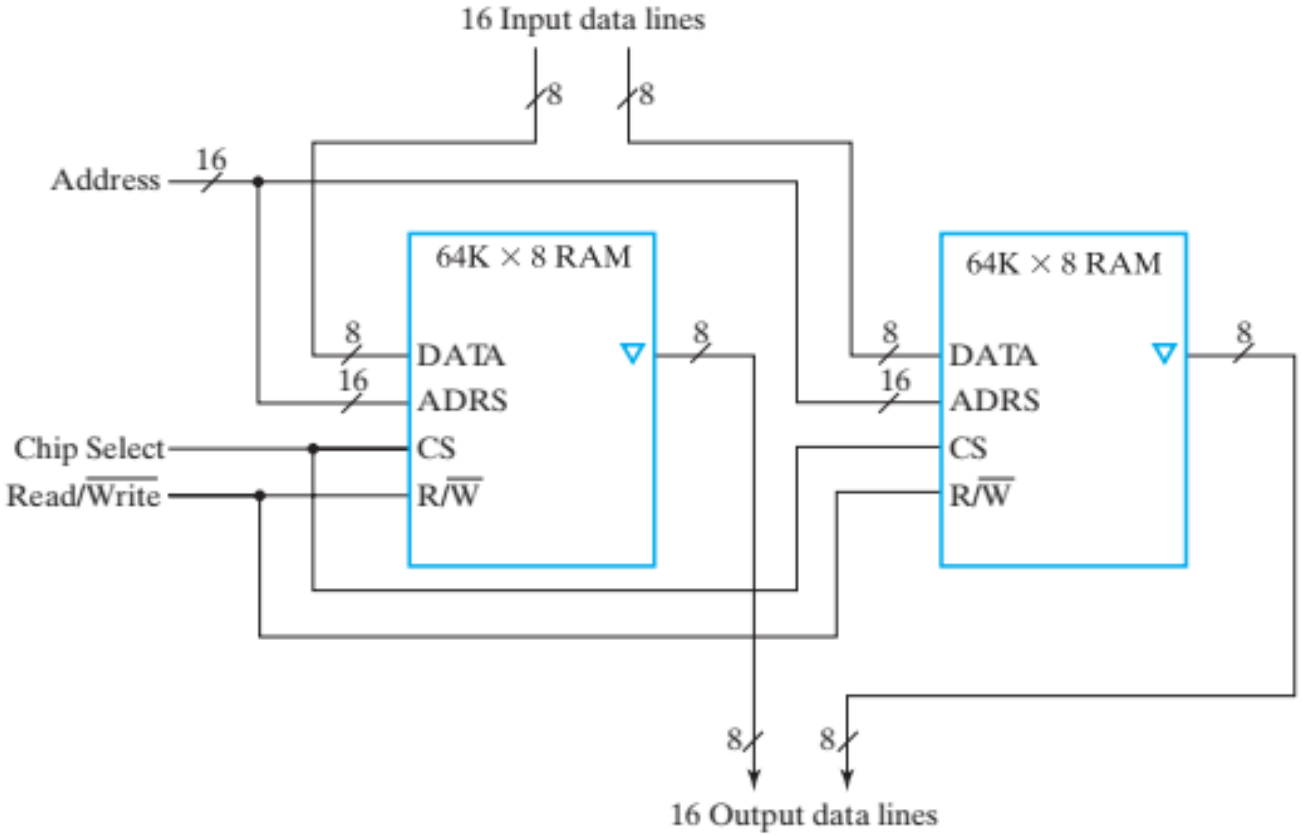

FIGURE 7-11
Block Diagram of a 64K × 16 RAM

5. DRAM ICs

- The dynamic RAM cell circuit consists of a capacitor C and a transistor T.
- The capacitor is used to store electrical charge.
  - If sufficient charge is stored on the capacitor, it can be viewed as storing a logical 1. If insufficient charge is stored on the capacitor, it can be viewed as storing a logical 0.
- The transistor acts much like a switch.
  - When the switch is “open,” the charge on the capacitor roughly remains fixed—in other words, is stored.
  - When the switch is “closed,” charge can flow into and out of the capacitor from the external Bit (B) line. This charge flow allows the cell to be written with a 1 or 0 and to be read

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5. DRAM ICs

- Read operation
  - Stored value 1:
    - Corresponding to a full storage tank.
    - With the large tank at a known intermediate level, the valve is opened. Since the small storage tank is full, water flows from the small tank to the large tank, increasing the level of the water surface in the large tank.
    - This increase in level is observed as the reading of 1 from the storage tank.
  - Stored value 0:
    - The storage tank is initially empty, there will be a slight decrease in the level in the large tank, which is observed as the reading of a 0 from the storage tank.
- So the read operation has destroyed the stored value; this is referred to as a *destructive read*. To be able to read the original stored value in the future, we must *restore* it (i.e., return the storage tank to its original level)

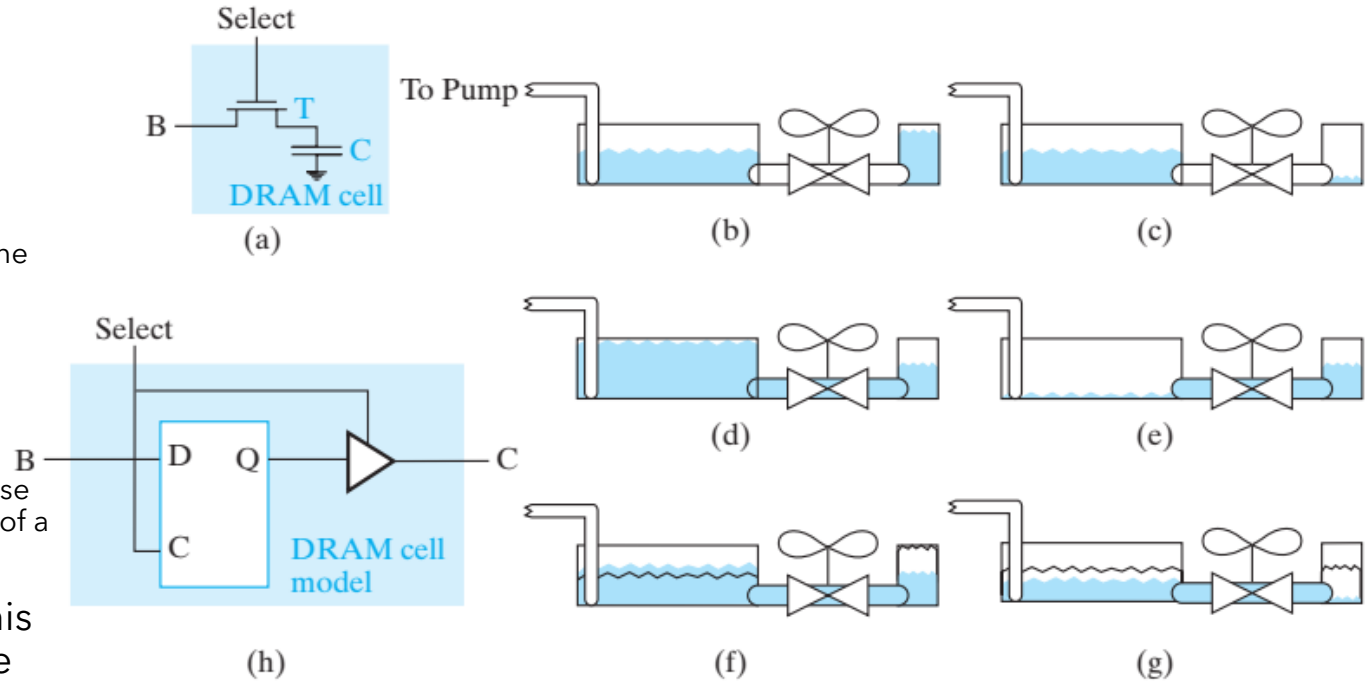

FIGURE 7-12
Dynamic RAM cell, hydraulic analogy of cell operation, and cell model

DRAM Bit Slice

- This model is similar to that for the SRAM bit slice. It is apparent that, aside from the cell structure, the two RAM bit slices are logically similar.
- However, from the standpoint of cost per bit, they are quite different. The DRAM cell consists of a capacitor plus one transistor. The SRAM cell typically contains six transistors, giving a cell complexity roughly three times that of the DRAM.

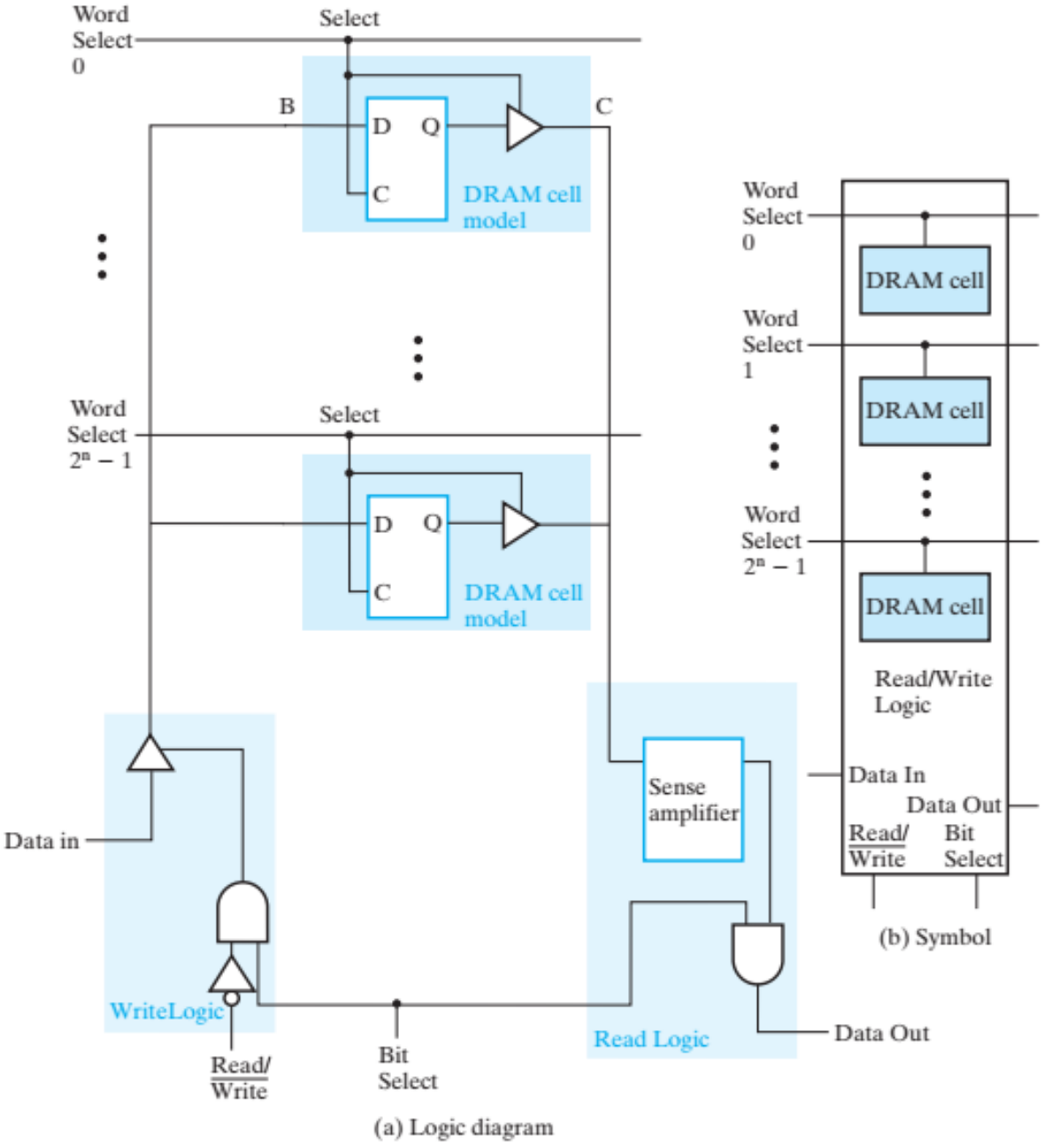

FIGURE 7-13
DRAM Bit-Slice Model

DRAM Bit Slice

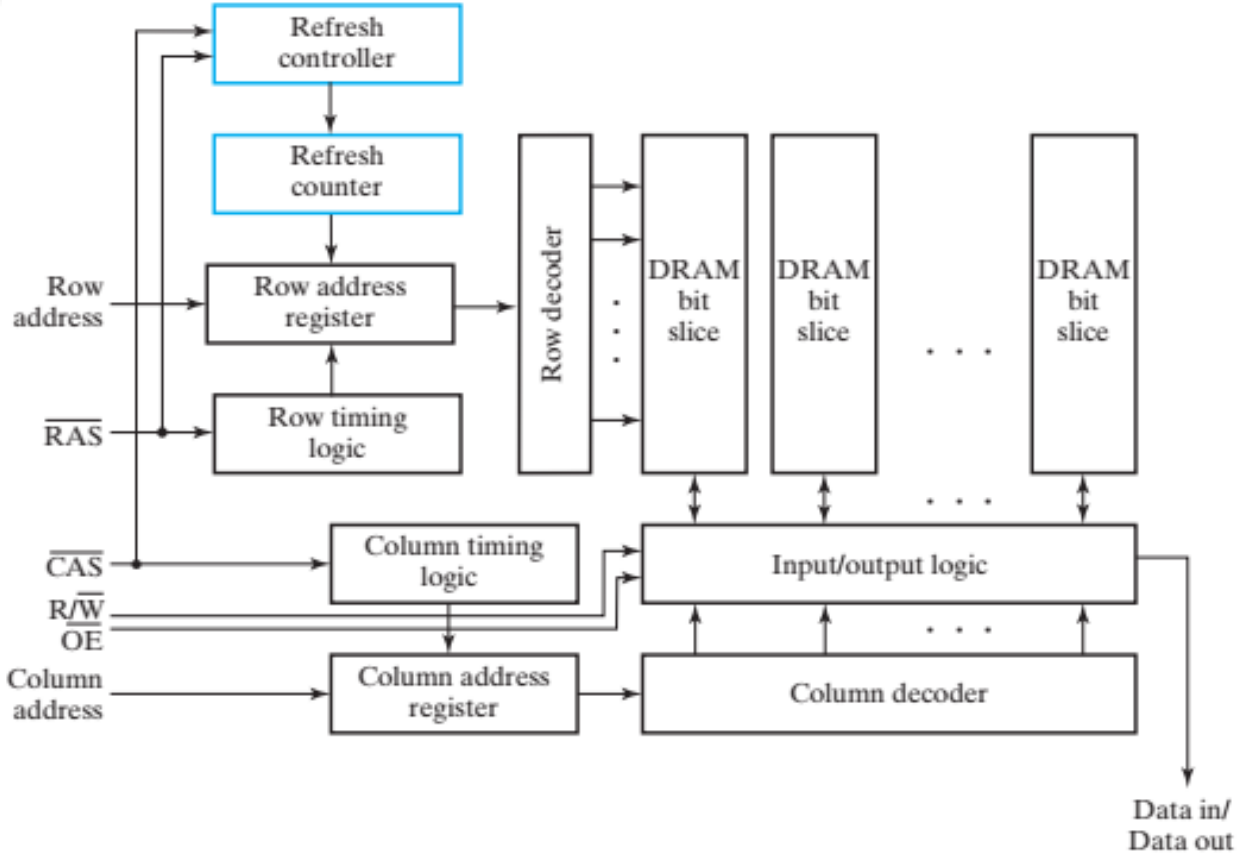

FIGURE 7-14
Block Diagram of a DRAM Including Refresh Logic