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Configuration and Readback of Virtex FPGAs Using JTAG Boundary-Scan

Summary

This application note demonstrates using a Boundary-Scan (JTAG) interface to configure and read back Virtex™ FPGA devices. Virtex devices have Boundary-Scan features that are compatible with IEEE Standard 1149.1. This application note is a complement to the configuration section in the Virtex data sheet and application note **XAPP138 "Virtex FPGA Series Configuration and Readback."** Xilinx recommends reviewing both the data sheet and XAPP138 prior to reading this document.

Note: The information in this application note also applies to the Virtex-E FPGA family.

Introduction

The IEEE 1149.1 Test Access Port (TAP) and Boundary-Scan architecture, commonly referred to as JTAG, is a popular testing method. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially responsible for developing the standard. This standard provides a means to ensure the integrity of individual board-level components and their interconnections. With increasingly dense multi-layer PC boards and more sophisticated surface mounting techniques, Boundary-Scan testing is becoming widely used as an important debugging standard.

Devices containing Boundary-Scan logic can send data out on I/O pins in order to test connections between devices at the board level. The circuitry can also be used to send signals internally to test the device specific behavior. These tests are commonly used to detect opens and shorts at both the board and device level.

In addition to testing, Boundary-Scan offers the flexibility for a device to have its own set of user-defined instructions. The added common vendor-specific instructions, such as configure and verify, have increased the popularity of Boundary-Scan testing and functionality.

Boundary-Scan for Virtex Devices

The Virtex family is fully compliant with the IEEE Standard 1149.1 Test Access Port and Boundary-Scan architecture. The architecture includes all mandatory elements defined in the IEEE 1149.1 Standard. These elements include the TAP, the TAP controller, the instruction register, the instruction decoder, the Boundary-Scan register, and the bypass register. The Virtex family also supports some optional instructions – the 32-bit identification register and a configuration register in full compliance with the standard. Outlined in the following sections are the details of the JTAG architecture for Virtex devices.

Test Access Port

The Virtex TAP contains four mandatory dedicated pins as specified by the protocol (Table 1).

Table 1: **Virtex TAP Controller Pins**

Pin	Description
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TCK	Test Clock

Three input pins and one output pin control the IEEE 1149.1 Boundary-Scan TAP controller. In addition to the required pins, there are optional control pins such as $\overline{\text{TRST}}$ (Test Reset) and enable pins, which can be found on devices from other manufacturers. Be aware of these optional signals when interfacing Xilinx devices with devices from different vendors because these signals can need to be driven. (To determine the set of signals that must be driven to enable IEEE 1149.1 compliance, see the vendor documentation for each device on the Boundary-Scan chain.)

The TAP controller is a 16-state state machine (Figure 1). Mandatory TAP pins are as follows:

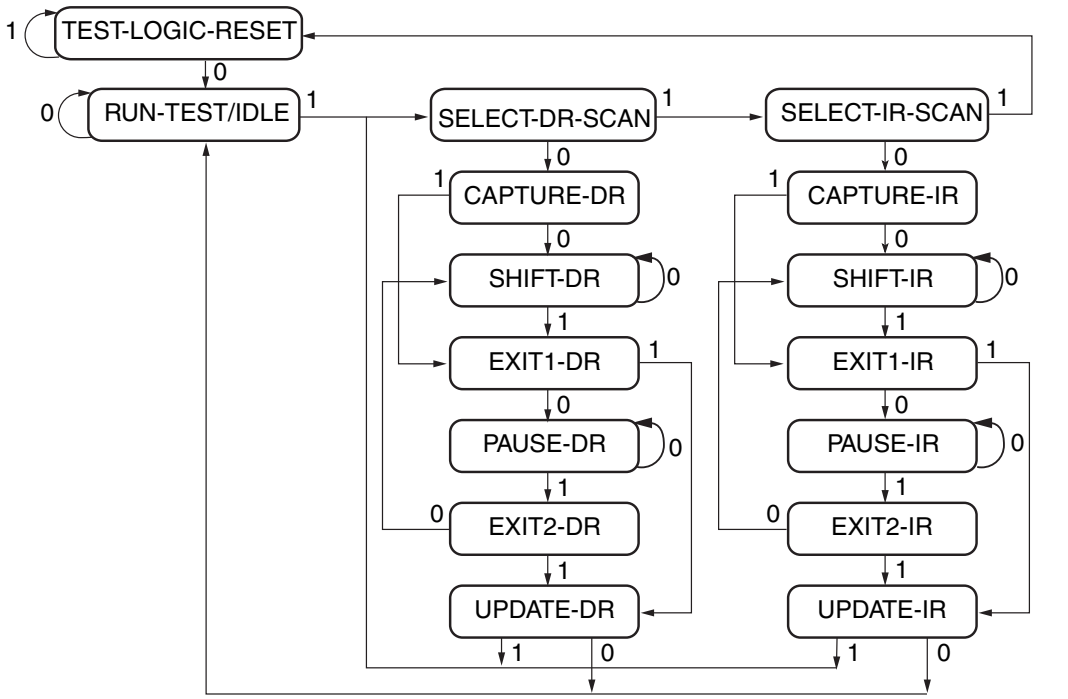
- TMS - The sequence of states through the TAP controller is determined by the state of the TMS pin on the rising edge of TCK. TMS has an internal resistive pull-up to provide a logic High if the pin is not driven.
- TCK - This pin is the JTAG test clock. It sequences the TAP controller and the JTAG registers in the Virtex devices.
- TDI - This pin is the serial input to all JTAG instruction and data registers. The state of the TAP controller and the current instruction held in the instruction register determine which register is fed by the TDI pin for a specific operation. TDI has an internal resistive pull-up to provide a logic High to the system if the pin is not driven. TDI is applied into the JTAG registers on the rising edge of TCK.
- TDO - This pin is the serial output for all JTAG instruction and data registers. The state of the TAP controller and the current instruction held in the instruction register determine which register (instruction or data) feeds TDO for a specific operation. TDO changes state on the falling edge of TCK and is active only during the shifting of instructions or data through the device. This pin is placed in a 3-state condition at all other times.

Note: As specified by the IEEE Standard, the TMS and TDI pins all have internal pull-ups. These internal pull-ups of 50-150 kΩ are active regardless of the mode selection.

When using the Boundary-Scan operations in Virtex devices, the V_{CCO} for Bank 2 must be at 3.3V for the TDO pin to operate at the required LVTTL level.

TAP Controller

Figure 1 diagrams a 16-state finite state machine. The four TAP pins control how the data is scanned into the various registers. The state of the TMS pin at the rising edge of the TCK determines the sequence of state transitions. There are two main sequences, one for shifting data into the data register and the other for shifting an instruction into the instruction register.



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

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Figure 1: **State Diagram for the TAP Controller**

Boundary-Scan Instruction Set

To determine the operation to be invoked, a 5-bit instruction is loaded into the instruction register. Table 2 lists the available Boundary-Scan instructions for Virtex devices.

Table 2: **Virtex Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code (4:0)	Description
EXTEST	00000	Enables Boundary-Scan EXTEST operation
SAMPLE	00001	Enables Boundary-Scan SAMPLE operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for readback
CFG_IN	00101	Access the configuration bus for configuration
INTEST	00111	Enables Boundary-Scan INTEST operation

Table 2: **Virtex Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code (4:0)	Description
USERCODE	01000	Enables shifting out user code
IDCODE	01001	Enables shifting out of ID code
HIGHZ	01010	Places output pins in a 3-states condition while enabling the bypass register
JSTART	01100	Clocks the start-up sequence when StartClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The mandatory IEEE 1149.1 commands are supported in Virtex devices along with several Xilinx vendor-specific commands. Virtex devices have a powerful command set. The EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions are all included. The TAP also supports two internal user-defined registers (USER1 and USER2) and configuration/readback of the device. The Virtex Boundary-Scan operations are independent of the mode selection. The Boundary-Scan mode in Virtex devices overrides the other mode selections. For this reason, Boundary-Scan instructions using the Boundary-Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) must not be performed during configuration. All instructions except USER1 and USER2 are available before the Virtex device is configured. After configuration, all instructions are available.

JSTART is an instruction specific to the Virtex architecture and configuration flow. As described in Table 2, the JSTART instruction clocks the startup sequence when the appropriate bitgen option is selected. The instruction does not work correctly without the correct bitgen option selected.

```
bitgen -g startupclk:jtagclk designName.ncd
```

For details on the standard Boundary-Scan instructions, EXTEST, INTEST, and BYPASS, refer to the IEEE Standard. The user-defined registers (USER1/USER2) are described in a later section of this application note.

Boundary-Scan Architecture

Virtex devices have several registers including all registers required by the IEEE 1149.1. In addition to the standard registers, the family contains optional registers for simplified testing and verification (Table 3).

Table 3: **Virtex JTAG Registers**

Register Name	Register Length	Description
Instruction register	5 bits	Holds current instruction OPCODE and captures internal device status
Boundary-Scan register	3 bits per I/O	Controls and observes input, output, and output enable
Bypass register	1 bit	Device bypass
Identification register	32 bits	Captures device ID
JTAG configuration register	32 bits	Allows access to the configuration bus when using the CFG_IN or CFG_OUT instructions
USERCODE register	32 bits	Captures user-programmable code

Boundary-Scan Register

The test primary data register is the Boundary-Scan register. The Boundary-Scan operation is independent of individual input/output block (IOB) configurations. Each IOB, bonded or unbonded, starts out as bidirectional with 3-state control. Later, it can be configured to be an input, output, or 3-state only. Therefore, three data register bits are provided per IOB (Figure 2).

When conducting a data register (DR) operation, the DR captures data in a parallel fashion during the CAPTURE-DR state. The data is then shifted out and replaced by new data during the SHIFT-DR state. For each bit of the DR, an update latch is used to hold the input data stable during the next SHIFT-DR state. The data is then latched during UPDATE-DR state when the TCK is Low.

The update latch is opened each time the TAP Controller enters the UPDATE-DR state. Care is necessary when exercising an INTEST or EXTEST to ensure the proper data has been latched before exercising the command. This is typically accomplished by using the SAMPLE/PRELOAD instruction.

Consider the presence of internal pull-ups and pull-down resistors when developing test vectors for testing opens and shorts. The IOB can be connected to an internal pull-up or pull-down resistor depending on the configuration state of the FPGA. (For more information on Virtex configuration modes and IOB connections to pull-up resistors, see the section on "Configuring through Boundary-Scan.")

- For an FPGA that is not yet configured, the Virtex configuration mode determines whether or not to connect the IOB to an internal pull-up resistor.
- For a configured FPGA, the connectivity of an IOB to an internal pull-up or pull-down resistor depends on the user configuration of the IOB or the BitGen setting for unused pins.

Figure 2 shows the Virtex Boundary-Scan architecture.

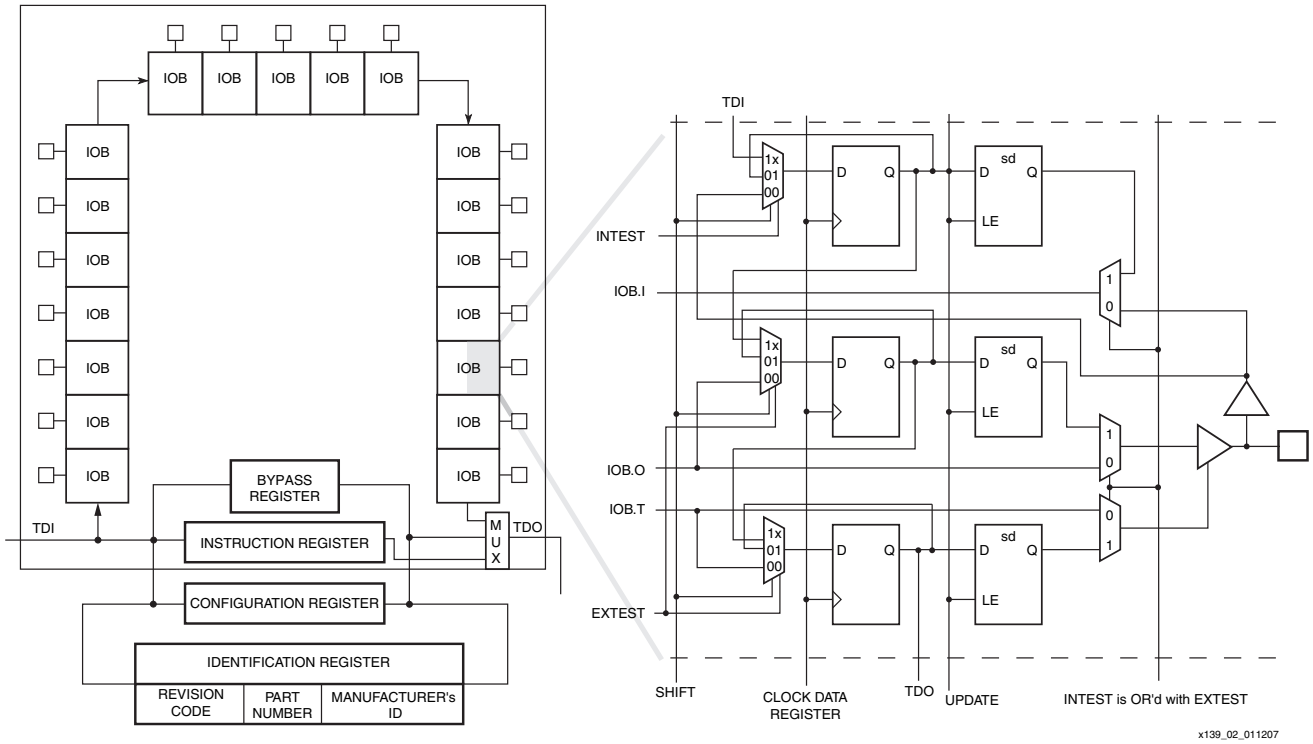

Figure 2: **Virtex Series Boundary-Scan Logic**

Bit Sequence

The order in each non-TAP IOB is described in this section. The input is first, followed by the output and finally the 3-state IOB control. The 3-state IOB control is closest to the TDO. The input-only pins contribute only the input bit to the Boundary-Scan I/O data register. The bit sequence of the device is obtainable from the “Boundary-Scan Description Language Files” (BSDL files) for the Virtex family. These files can be obtained from the Xilinx software download area. The bit sequence is invariant of the design. It always has the same bit order and the same number of bits.

Bypass Register

The other standard data register is the single flip-flop BYPASS register. It directly passes data serially from the TDI pin to the TDO pin during a bypass instruction. This register is initialized to zero when the TAP controller is in the UPDATE-DR state.

Instruction Register

The instruction register is a 5-bit register that loads the OPCODE necessary for the Virtex Boundary-Scan instruction set. This register loads the current OPCODE and captures internal device status.

Configuration Register (Boundary-Scan)

The configuration register is a 32-bit register. This register allows access to the configuration bus and readback operations.

Identification Register

The Virtex devices have an identification register, commonly referred to as the IDCODE register. This register is based upon the IEEE Standard 1149.1 and allows easy identification of the part being tested or programmed through Boundary-Scan. Table 4 lists the general format of the identification register.

Table 4: **Virtex Identification Register**

Revision Code	Part Number		Manufacturers ID	LSB
	Family Code	Part Size Code		
31 ... 28	27 ... 21	20 ... 12	11 ... 1	0
XXXX	0000011	YYYYYYYYY	0000 1001 001	1

Table 5 lists specific IDCODES assigned to Virtex series FPGAs.

Table 5: **IDCODEs Assigned to Virtex Series FPGAs**

FPGA	IDCODE
XCV50	v0610093h
XCV50E	v0A10093h
XCV100	v0614093h
XCV100E	v0A14093h
XCV150	v0618093h
XCV200	v061C093h
XCV200E	v0A1C093h
XCV300	v0620093h
XCV300E	v0A20093h
XCV400	v0628093h
XCV400E	v0A28093h
XCV405E	v0C28093h
XCV600	v0630093h
XCV600E	v0A30093h
XCV800	v0638093h
XCV812E	v0C38093h
XCV1000	v0640093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Notes:

1. The "v" in the IDCODE is the revision code field.

USERCODE Register

USERCODE is supported in the Virtex family as well. This register allows a user to specify a design-specific identification code. The USERCODE can be programmed into the device and read back for verification at a later time. The USERCODE is embedded into the bitstream during bitstream generation (`bitgen -g` UserID option) and is valid only after configuration.

Single Device Configuration

Note: Refer to **XAPP058** for the recommended embedded solution.

To configure a Virtex part as a single device through Boundary-Scan operations, use the steps listed in Table 8, which lists and describes the TAP controller commands required to configure a Virtex device. Ensure the bitstream is generated with the JTAG clock option:

```
bitgen -g startupclk:jtagclk designName.ncd
```

Also, when programming with iMPACT software, verify that the most current version of software is used. Refer to Figure 1 for the TAP controller states. These TAP controller commands are issued automatically if configuring the part with the iMPACT software.

Table 8: **Single Device Configuration Sequence**

TAP Controller Step Description		Set and Hold		Number of Clocks
		TDI	TMS	TCK
1	On power-up, place a "1" on the TMS and clock the TCK five times. (This ensures starting in the TLR (Test-Logic-Reset) state.)	X	1	5
2	Move into the RTI state.	X	0	1
3	Move into the SELECT-IR state.	X	1	2
4	Enter the SHIFT-IR state.	X	0	2
5	Start loading the CFG_IN instruction .(1)	0101	0	4
6	Load the last bit of CFG_IN instruction when exiting SHIFT-IR (defined in the IEEE standard).	0	1	1
7	Enter the SELECT-DR state.	X	1	2
8	Enter the SHIFT-DR state.	X	0	2
9	Shift in the Virtex bitstream. (bit_N (MSB) is the first bit in the bitstream (1))	bit_1... bit_N	0	(Number of bits in bitstream) –1
10	Shift in the last bit of the bitstream. (bit_0 (LSB) is shifted on the transition to EXIT1-DR)	bit_0	1	1
11	Enter UPDATE-DR state.	X	1	1
12	Enter the SELECT-IR state.	X	1	2
13	Move to the SHIFT-IR state.	X	0	2
14	Start loading the JSTART instruction.(1) (The JSTART instruction initializes the startup sequence.)	1100	0	4
15	Load the last bit of the JSTART instruction.	0	1	1
16	Move to the SELECT-DR state.	X	1	2
17	Move to SHIFT-DR and clock the STARTUP sequence. (by applying a minimum of 12 clock cycles to the TCK).	X	0	≥14
18	Move to the UPDATE-DR state.	X	1	2
19	Return to the RTI state. (The device is now functional).	X	0	1

Note:

1. In the TDI column, the right-most bit is shifted in first.