MIXED-SIGNAL EDGE ACCELERATOR FOR REAL-TIME MMWAVE PLATFORM VIBRATION COMPENSATION

BACKGROUND AND INTRODUCTION

Background/Motivation:

In recent years, the technological community has witnessed remarkable innovation in the development of robust and configurable CMOS sensors, powerful processing engines, and, in the algorithm domain, increasingly generalizable machine-learning models. The consolidation of advances in these three domains has thus created an eminent opportunity for the creation of truly autonomous edge perception devices to an extent heretofore unexplored. While edge sensing is by no means a novel concept in a modern age of distributed device networks, the inherent tradeoff between computational capacity and power consumption has ultimately rendered current solutions infeasible for energy-constrained edge devices operating on battery power. Autonomous vehicles employing peripheral tensor core GPU accelerators, for instance, devote close to a kW of power toward their 100-TOPs edge sensor processing pipelines, a clear limitation for truly edge-based systems such as wearable devices in the public safety domain or motion-capture VR applications. Mitigating this processing load is even more crucial for 3D mmWave radar sensors yielding higher dimensions of complex data. Ultimately, attaining sub-Watt power levels while achieving similar 100-TOPs performance requires a paradigm shift towards verticalization and end-to-end design of the target system. Through a hybrid circuits-, signal processing-, and learning-based approach, sensors with hardware-embedded intelligence can be optimized for energy and throughput given the known computational requirements, permitting feasible integration into relatively low-power peripheral devices. Compared with alternative sensing modalities, mmWave radar represents an optimal vehicle for edge-based perception, given its suitability for 3D imaging and relative immunity to adverse environmental conditions [1]. Thus, the proposed mixed-signal edge accelerator IC will be design specifically for integration into multi-sensor mmWave RF systems, with the circuits hardware and signal processing algorithms designed in parallel to enable power-constrained, high-resolution edge perception.

Any reliable system design, however, must address one aspect inherent in any active intelligent mmWave edge device and detrimental to signal reception: the motion of the sensor itself, an issue, for instance, with head-mount systems. To account for such arbitrary or deterministic parasitic motion, the sensor must be capable of filtering and deconvolving the RX returns to generate a noise-free signal. For this project, I consider the effect of vibration on the radar platform, for which [2] provides a detailed theoretical analysis. Given empirical knowledge of a superposition of vibration forces applied to the sensor, I seek to, in real time, extract the associated bias from the range-Doppler response to obtain a clean image of stationary and non-stationary targets in the environment. The proposed approach utilizes an external IMU to retrieve high-resolution motion data capturing the complex, multi-source motion. Both a sliding window, regularization-aided estimation approach, as well as a frequency-domain inverse kernel estimation approach will be explored to correct the phases of the received FMCW radar chirps on a per-frame basis. Through a frame-level phase correction algorithm implemented inside the edge accelerator IC itself, I hope to develop a precise early-fusion method of correcting the RX

signal returns. Such edge-based analysis replaces the conventional, compute-intensive post-processing methods used, for instance, in synthetic aperture migration-correction [3].

Related work:

Architecture wise, any intelligent mmWave sensor solution must comprise an integrated radar transceiver, typically designed for frequency-modulated continuous wave (FMCW) operation, as well as a processing core capable of parsing and performing computation on the received data. Fully integrated on-chip radars are certainly not novel, but application-specific solutions incorporating hybrid DSP-cores into the radar system are less common. While both industrial and academic efforts have produced integrated solutions that allow for configurability and programmability, most systems locate the processing cores on a device separate from the radar chip. The FMCW MIMO array demonstrated in [4], for instance, utilizes a standalone direct digital synthesizer IC which routes the waveform to thirteen separate radar chips. Similarly, solutions such as [5]-[6], which present wide-bandwidth radar sensors with integrated antennas, [7], which demonstrates 25 dBi TX-RX isolation in its integrated antenna solution, and [8], which presents a high-resolution PLL-based fast-chirp FM modulation scheme, lack the capacity for on-chip processing or learning. Distributed FMCW radars, such as the repeater tag architecture proposed in [9] and the frequency division multiplexing MIMO array presented in [10], while achieving improved signal quality and performance, also perform processing off-chip.

In the RFID realm, complex wirelessly powered mm-scale systems incorporating integrated RF antennas and receivers have been proposed, as in [11], but again lack the desired “intelligence” facet. The wideband FMCW SoC presented in [12] does integrate a DSP core; however, this is geared primarily towards waveform and timing sequence generation, rather than post-processing. Meanwhile, complex industrial solutions which do incorporate data processing capabilities on the radar solution itself, such as the mmWave IC’s developed by Texas Instruments, are designed to be highly programmable and interfaceable and thus operate with much higher power consumption, including complete microprocessor cores [13]. The goal is to find a middle ground in such edge devices: sensors with integrated intelligence capabilities which are designed for, and can thus be optimized for, specific applications.

This project, of course, seeks to compensate the motion of the mmWave platform itself. Active sensors, after all, cannot operate under the idealized assumption that they are completely stationary. When placed on the body, as they often are in motion capture applications, for instance, sensors are subject to continuous motion. In order to account for such arbitrary or deterministic parasitic motion, the sensor must be capable of filtering the received signal to generate a noise-free version. Such a task, however, is ultimately non-trivial and, indeed, lacks a proven, well-established solution given the acceleration of the radar platform. As discussed in [14], conventional fast-chirp and digital radars employ traditional signal processing schemes, which assume that estimation of range, velocity, and angle can be posed as three independent problems in three independent dimensions: fast time, slow time, and the spatial domain. The reality, however, is that these measurement dimensions are not independent. Range migration, which occurs as the range of a moving target shifts over consecutive chirp waveforms, and Doppler migration, in which distinct frequencies in a wideband signal undergo varying Doppler

shifts, both contribute to the smearing of the signal energy into multiple adjacent range and velocity cells, thereby reducing resolution. This effect is particularly evident in synthetic aperture radar systems, in which the radar itself is moving along a trajectory orthogonal to the imaged target [15]. In such cases, the Doppler keystone transform (DKT) may be used to implement the range cell migration correction needed to address these range walk and range curvature nonidealities [16]. In fact, [17] and [18] discuss the viability of this method for imaging vibrating targets. When the vibration source is placed on the radar platform itself, however, the entire scene, including all clutter, undergoes the characteristic deterministic motion induced by the vibration, rather than simply a point scatterer target. Given this added "universal" acceleration, the DKT cannot fully correct for the resulting Doppler smear. Furthermore, the DKT algorithm typically takes place in SAR post-processing, thereby precluding the real-time response desired for intelligent edge-sensor networks. This work, therefore, seeks to correct the acceleration induced on the sensor platform in real time, so as to generate a deconvolved signal prior to post-processing.

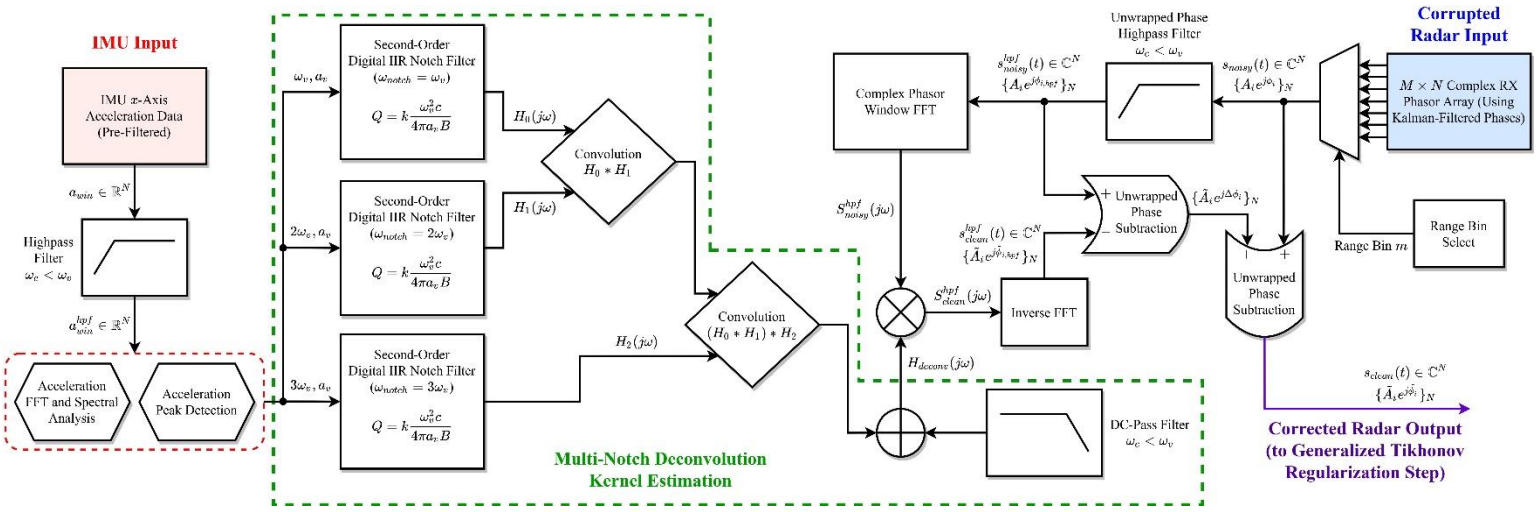
Proposed Approach:

As aforementioned, I will consider the effect of vibration on the radar platform, which will be induced via an external eccentric rotating mass motor (ERM). Given the desire for real-time filtering of the vibration motion induced on the radar platform, this works employs the services of an inertial measurement unit (IMU), which provides instantaneous accelerometer, gyroscope, and magnetometer measurements along all three coordinate axes. However, for this chip, I may decide to only use the accelerometer data, depending on the need for additional sensor fusion. Currently, I am planning on using an analog IMU, which provides data that can be filtered, smoothed, and conditioned in a manner more efficiently than with a digital IMU. From these clean acceleration measurements, the amplitude and frequency of the parasitic vibration motion induced upon the radar platform can be inferred, and all subsequent signal processing can be performed to correct for the effect of the vibrations in real time. In particular, time windows of data from both the radar and accelerometer will be considered, thereby reducing the amount of memory required on-chip. The sliding window technique integral to the processing pipeline can then be easily implemented via a FIFO-based input serial link and an analog sample-and-hold circuit for the accelerometer data.

A diagram of the proposed motion correction scheme is shown on the next page. The window of N phase measurements is determined via a range FFT, with the resulting sequence first high-pass-filtered to remove the DC component. This high-pass filter will be done as a digital FIR filter since the phase measurements are already digitized. Meanwhile, the analog IMU measurements will be high-pass-filtered in the analog domain to remove any existing DC component. After an FFT is performed on the IMU data to detect the vibration frequency, a multi-notch low-Q IIR filter is generated, with notches at the vibration harmonics. The final multi-notch deconvolution kernel is then multiplied point-wise by the frequency-domain phase data to yield the correct frequency-domain phase progression. An inverse FFT is then performed in the digital domain, with result subtracted from the original high-pass-filtered data and the original phases in succession, yielding a final window of corrected phases as the output of the

algorithm. Successive windows are concatenated together to yield the continuous stream of corrected output phases.

Phasor Correction Algorithm Diagram:



The fundamental circuit blocks needed for the proposed chip are outlined below. Notes are added beneath each block to denote which components will be included off-chip on a PCB rather than on-chip.

Fundamental Circuit Blocks:

Clock Generation Block:

The clock generation block will consist of a low-frequency oscillator circuit as well as a frequency-multiplying PLL, which will synthesize the clock frequency needed for the digital processing engine on the chip. This will entail primarily analog circuit design to generate a clean clock output from the PLL. Aside from the digital processing engine, other core blocks requiring a clock include the IMU sample-and-hold circuit (which sets the IMU sampling rate), and the receiver serial link connected to the DCA1000EVM radar board, which will require a higher frequency given the quantity of raw ADC data output from the on-board FPGA.

The oscillator will be integrated off-chip on the PCB, with the base frequency for the PLL supplied by an off-chip component.

Power Regulation Block:

The power regulation block will include an LDO regulator, which will provide the power for the radar data I/O interface as well as the 3.3 V supply needed for the off-chip IMU. A 1.8 V bandgap reference will be used to generate the reference voltage used in the SAR ADC, as well as the supply voltages used in the analog signal conditioning chain for the IMU.

The power regulation components will be integrated off-chip on the PCB.

Analog Signal Conditioning Chain:

The data from the off-chip analog IMU will first be conditioned via a series of band-pass filters and amplifiers to generate a noise-free, low-frequency signal representing the vibration principal tone. A frequency-locking PLL will then be used to measure the frequency of the input vibration signal during a given window of time (determined by the sampling frequency), while an envelope/peak detector circuit will record the peak acceleration values in the retrieved data (to be used in the multi-notch deconvolution filter construction). The peak levels, as well as the measured vibration frequency (PLL low-pass filter output voltage), will then be sampled and digitized via two SAR ADCs, and the resulting data for this time period will be stored in a small memory bank (8 KB SRAM) to be used for the digital IIR multi-notch deconvolution kernel estimation. While the first three harmonics of the measured vibration frequency will determine the locations of the notches along the frequency spectrum, the vibration amplitude measured by the peak detector circuit will be used to compute the quality factor/bandwidth of notches, thereby adapting to possible acceleration-induced leakage in the primary Doppler bin. The alternative to this method of notch filter construction would have been to digitize all of the incoming IMU data and to estimate the frequency and amplitude of vibration in the digital domain. However, this

would have been a much more power-hungry solution to a problem that can easily be addressed in the analog domain.

Radar Raw ADC Data Receiver:

This will be a simple serial link implemented via an SPI interface with the FPGA on the DCA100EVM, which provides the raw RX ADC data over the two LVDS lanes provided by the AWR1843 module. The SPI interface will be operated using a simple digital SPI controller, with the received data for a given time window stored in a local memory bank.

The logic SPI controller will be integrated off-chip, with the extracted raw complex ADC data fed as direct inputs to the PCB.

Digital Processing Engine:

The digital processing engine will take as inputs the frequency and amplitude of the vibrations measured by the analog receive chain, as well as the raw ADC RX signals obtained from the DCA1000EVM board. The digital processing block includes a second-order IIR notch filter estimation unit for the deconvolution kernel computation and an FFT engine for the complex radar data frequency-domain analysis. An inverse FFT and unwrapped phase subtraction are then performed to evaluate the corrected time-domain phasor sequence, with a regularization step performed at the end to smooth the resulting phase progression. The digital output will then be serialized and transmitted via an output serial link to an off-chip processor, which can perform all post-processing analysis on the cleaned-up/filtered radar cube of data.

The digital processing engine on the final chip will include only the deconvolution kernel estimator module as well as several SRAMs to store computational vectors and the computed IIR notch filter frequency response. Integration with the radar data will occur off-chip.

Performance/Energy/Area Targets:

The chip will be integrated in the Efabless Caravel test harness, which includes a 3.5 mm x 2.9 mm user area; the area of the design must fit within these constraints, yielding a maximum chip area of 10 mm^2. The target total power consumption is under 50 mW, which is compatible with the concept of a a real-time edge-based approach to intelligent radar processing that can be implemented at a power consumption level magnitudes smaller than typical tensor core GPUs.

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