i.

a) Consider 32 words cache and 512 words main memory. Block size 4 words. Deter main the number of memory blocks and cache lines. Determine the number of bits required for physical address, tag, index and block offset. Also draw and explain the direct mapping cache configuration with main memory. 7

b) Give example of Cache Hit and Cache Miss. 3

ii.

a) Draw and explain the single cycle data path organization for (MIPS) the following high level statement.

$$R[i] = R[i] + Y;$$

b) How many basic components are in MIPS single cycle data path.explin all functions of all components?