

Memory:

1. Give a brief descriptions of different types of memory.
2. Draw and explain memory hierarchy according to time, size and cost.
3. Steps of Cache memory working procedure.
4. Draw the hardware logics of cache hit or miss.
5. Define the following terms:
 - Cache
 - memory hierarchy
 - direct-mapped cache
 - tag
 - hit time
 - miss rate
 - block
 - hit
 - miss
6. Consider 32 words cache and 512 words main memory. Block size 4 words. Determine the number of memory blocks and cache lines. Determine the number of bits required for physical address, tag, index and block offset. Also draw and explain the direct mapping cache configuration with main memory.
7. What are the four questions that are help us to design cache.
8. Find the number of misses and hits for a cache with four 1-word blocks given the following sequence of memory block accesses: 0, 8, 0, 6, 6, 8, 7, 11
for each of the following cache configurations
i) Direct mapped
ii) 2-way set associative (use LRU replacement policy)
Fully associative.

Data path:

9. Draw all the functional units of processor.(elements of data path)

10. Draw and explain the single cycle data path organization for (MIPS) the following high level statement.

$R[i] = R[i+2] - Y$; where i = last two digits of your ID number.