

# COD Ch. 3



## Instructions: Language of the Machine

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# Instructions: Overview

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- Language of the machine
- More primitive than higher level languages, e.g., no sophisticated control flow such as *while* or *for* loops
- Very restrictive
  - e.g., MIPS arithmetic instructions
- We'll be working with the MIPS instruction set architecture
  - inspired most architectures developed since the 80's
  - used by NEC, Nintendo, Silicon Graphics, Sony
  - the name is just not related to *millions of instructions per second* !
  - it stands for **m**icrocomputer **w**ithout **i**nterlocked **p**ipeline **s**tages !
- Design goals: *maximize performance* and *minimize cost* and *reduce design time*



# MIPS Arithmetic

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- All MIPS arithmetic instructions have 3 operands
- Operand order is fixed (e.g., destination first)
- *Example:*

C code:

$A = B + C$

compiler's job to associate  
variables with registers

MIPS code:

add  $\underbrace{\$s0, \$s1, \$s2}$



# MIPS Arithmetic

- Design Principle 1: *simplicity favors regularity.*

*Translation: Regular instructions make for simple hardware!*

- *Simpler hardware reduces design time and manufacturing cost.*

- Of course this complicates some things...

C code:             $A = B + C + D;$   
                      $E = F - A;$

MIPS code  
(arithmetic):     $\text{add } \$t0, \$s1, \$s2$   
                      $\text{add } \$s0, \$t0, \$s3$   
                      $\text{sub } \$s4, \$s5, \$s0$

Allowing variable number of operands would simplify the assembly code but complicate the hardware.

- Performance penalty: high-level code translates to denser machine code.



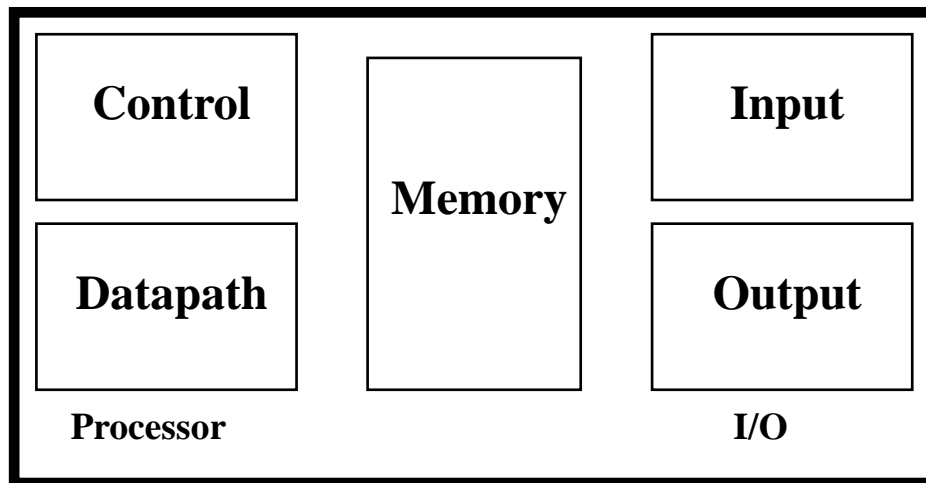
# MIPS Arithmetic

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- *Operands must be in registers* – only 32 registers provided (which require 5 bits to select one register). Reason for small number of registers:
- Design Principle 2: *smaller is faster.*    *Why?*
  - *Electronic signals have to travel further on a physically larger chip increasing clock cycle time.*
  - *Smaller is also cheaper!*

# Registers vs. Memory

- Arithmetic instructions operands must be in registers
  - MIPS has 32 registers
- Compiler associates variables with registers
- What about programs with lots of variables (arrays, etc.)? Use *memory, load/store* operations to transfer data from memory to register – if not enough registers *spill registers* to memory
- *MIPS is a load/store architecture*





# Memory Organization

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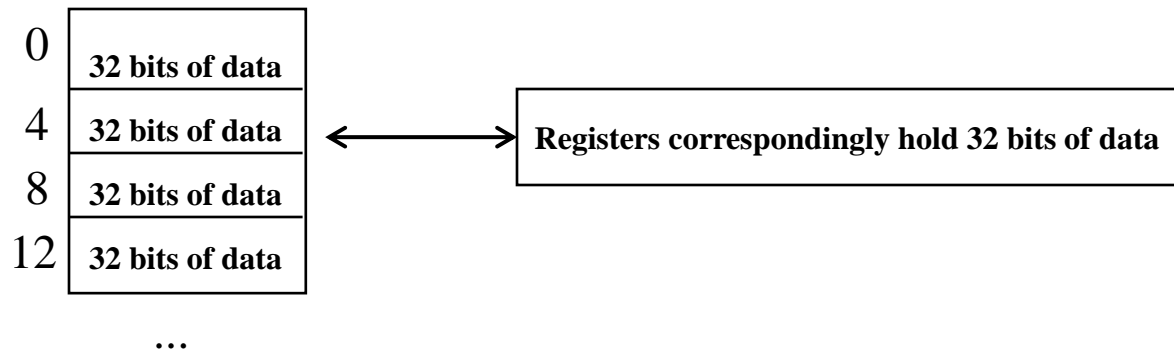
- Viewed as a large single-dimension array with access by *address*
- A memory address is an *index* into the memory array
- *Byte addressing* means that the index points to a byte of memory, and that the unit of memory accessed by a load/store is a byte

0	8 bits of data
1	8 bits of data
2	8 bits of data
3	8 bits of data
4	8 bits of data
5	8 bits of data
6	8 bits of data

...

# Memory Organization

- Bytes are load/store units, but most data items use larger *words*
- For MIPS, a word is 32 bits or 4 bytes.



- $2^{32}$  bytes with byte addresses from 0 to  $2^{32}-1$
- $2^{30}$  words with byte addresses 0, 4, 8, ...  $2^{32}-4$ 
  - i.e., words are *aligned*
  - *what are the least 2 significant bits of a word address?*





# Load/Store Instructions

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- *Load* and *store* instructions
- *Example:*

C code:             $A[8] = h + A[8];$

MIPS code    (load):     $\text{lw } \$t0, 32(\$s3)$

                 (arithmetic):     $\text{add } \$t0, \$s2, \$t0$

                 (store):     $\text{sw } \$t0, 32(\$s3)$

Diagram labels:   
- **value** points to  $\$t0$  in the load instruction.   
- **offset** points to  $32$  in the load instruction.   
- **address** points to  $\$s3$  in the load instruction.

- Load word has destination first, store has destination last
- Remember MIPS arithmetic operands are registers, not memory locations
  - therefore, words must first be moved from memory to registers using loads before they can be operated on; then result can be stored back to memory