

Nian-Ze Lee

Curriculum Vitae

2024-04-04

Coordinates

Affiliation:	Ludwig-Maximilians-Universität München Software and Computational Systems Lab Oettingenstr. 67, Munich, Germany	Webpage:	nianzelee.github.io
Citizenship:	Taiwanese	Phone:	+49-176-677-030-45
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		Year of birth:	1991

Research Interests

My research focuses on the application of formal methods to the analysis and optimization of computational models, including software programs, VLSI circuits, and emerging technologies. Specifically, I am active in the following directions (tools which I have developed or contributed to are given in parentheses):

- Cross-application of hardware and software verification techniques ([BTOR2C](#), [BTOR2-CERT](#), and [CPV](#))
- Development of new algorithms for software verification ([CPACHECKER](#))
- Stochastic Boolean satisfiability and its application to probabilistic models ([RESSAT](#) and [ERSSAT](#))
- Optimization and verification of threshold logic circuits ([TLCOLLAPSEVERIFY](#))

The theoretical foundation of my work is algorithms and data structures, formal methods, mathematical logic, and system modeling. My goal is to invent new approaches for real-world applications with heterogeneous components. I also emphasize software engineering for tool implementation and reproducible evaluation.

Education

2015 – 2021	Ph.D., Graduate Institute of Electronics Engineering National Taiwan University, Taipei, Taiwan Advisor: Prof. Jie-Hong R. Jiang Lam Research Thesis Award Dissertation: <i>Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications</i>
2009 – 2014	B.Sc. in Eng., Department of Electrical Engineering Minor in Economics National Taiwan University, Taipei, Taiwan

Academic Employment

since 2021	Postdoctoral Researcher , Host: Prof. Dirk Beyer Ludwig-Maximilians-Universität München, Munich, Germany
2019 – 2020	DAAD Scholarship Student , Host: Prof. Dirk Beyer Ludwig-Maximilians-Universität München, Munich, Germany
2018 – 2019	Internship Student at ERATO MMSD Project , Host: Prof. Ichiro Hasuo National Institute of Informatics, Tokyo, Japan
2015 – 2021	Research and Teaching Assistant , Advisor: Prof. Jie-Hong R. Jiang National Taiwan University, Taipei, Taiwan

Industrial Employment

2016	Research Intern , Mentor: Dr. Victor N. Kravets IBM Thomas J. Watson Research Center, Yorktown Heights, NY, U.S.A.
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Grants

2024-2027	German Research Foundation (DFG) Research funding, €363.6 K Topic: <i>Bridging Hardware and Software Analysis</i> (1 Ph.D. position)
2023-2024	LMUexcellent PostDoc Support Fund Travel funding, €10.6 K
2019-2020	German Academic Exchange Service (DAAD) Joint scholarship with National Science and Technology Council, Taiwan, €15 K

Awards and Recognitions

2022	Best Master Lecture <i>Methods in Software Engineering</i> , instructor: Prof. Gidon Ernst
2021	Lam Research Thesis Award Dissertation title: <i>Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications</i>
2021	Honorary Member of the Phi Tau Phi Scholastic Honor Society Achievement of academic excellence upon graduation

Important Publications

Statistics: h-index 9; 3 journal papers and 20 peer-reviewed conference papers in prestigious venues, including the **IEEE Transactions on Computers** and **AAAI Conference on Artificial Intelligence**.

The complete list of my peer-reviewed publications can be found via

- My personal website: <https://nianzelee.github.io>
- DBLP: <https://dblp.org/pid/154/3010.html>
- Google Scholar: <https://scholar.google.com/citations?user=.8OD03gAAAAJ>

Below are my five most important publications.

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-Based Model Checking Revisited: Adoption to Software Verification. *Journal of Automated Reasoning*, 2024. Accepted, preprint available via <https://doi.org/10.48550/arXiv.2208.05046>.
2. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 13994, pages 152–172. Springer, 2023. doi: [10.1007/978-3-031-30820-8_12](https://doi.org/10.1007/978-3-031-30820-8_12).
3. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021. doi: [10.1609/aaai.v35i5.16506](https://doi.org/10.1609/aaai.v35i5.16506).
4. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021. doi: [10.1109/TCAD.2020.3015441](https://doi.org/10.1109/TCAD.2020.3015441).
5. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018. doi: [10.1109/TC.2018.2807431](https://doi.org/10.1109/TC.2018.2807431).

Talks

Invited Speech

“*Bridging Hardware and Software Formal Verification for Reliable Computing Systems*”, Interview of Tenure-Track Assistant Professorship for “Reliable Software and Distributed Systems”, School of Electrical, Information, and Media Engineering, University of Wuppertal, January 2024

“*Bridging Hardware and Software Analysis*”, EDA Group Seminar, Graduate Institute of Electronics Engineering, National Taiwan University, November 2023

Workshop Presentation

“*Bridging Hardware and Software Verification Witnesses*”, [1st Workshop on Verification Witnesses and Their Validation](#), July 2023

“*Enriching Software Verification with Analyses and Applications from Hardware*”, [7th International Workshop on CPAchecker](#), October 2022

Software

[ABC](#): Sequential logic synthesis and formal verification

Contributor

[BENCHEXEC](#): Reliable benchmarking and resource measurement

Contributor

[BTOR2C](#): Translation from word-level circuits to C programs

Principal designer, implementer, and maintainer

[BTOR2-CERT](#): Certifying hardware verification using software analysis

Principal designer and maintainer

[CPACHECKER](#): Configurable software verification

Contributor, conceptual extensions, and implementation of interpolation-based analyses

[CPV](#): Circuit-based program verification

Principal designer and maintainer

[RESSAT](#) and [ERSSAT](#): Stochastic satisfiability solvers

Principal designer, implementer, and maintainer

[TLCOLLAPSEVERIFY](#): Optimization and verification of threshold logic circuits

Principal designer, implementer, and maintainer

Student Mentoring

2021-	Po-Chun Chien, DFG RTG ConVeY Ph.D. student, LMU Munich Topic: Bridging hardware and software verification
2023-	Marek Jankola, DFG RTG ConVeY Ph.D. student, LMU Munich Topic: Replicating interpolation-based hardware verification for software
2023	Ádám Zófia, Erasmus Program Ph.D. student, Budapest University of Technology and Economics Topic: Witness validation for programs translated from hardware models
2023	Bastiaan Laarakker, Google Summer of Code Master student, University of Amsterdam Topic: Backward bounded model checking in CPAchecker

University Activities

Statistics: I have been a teaching assistant for 5 graduate courses, 2 graduate seminars, 2 undergraduate courses, and 1 undergraduate seminar, and supervised 3 Bachelor's theses/projects at LMU Munich and NTU since 2016.

Graduate Course

Software Verification, Summer 2023, instructor: Prof. Dirk Beyer

Methods in Software Engineering, Summer 2022, instructor: Prof. Gidon Ernst
(**Best Master Lecture** at Institute of Informatics)

Software Verification, Winter 2021, instructor: Prof. Dirk Beyer

Logic Synthesis and Verification, Fall 2020, instructor: Prof. Jie-Hong R. Jiang

Logic Synthesis and Verification, Fall 2018, instructor: Prof. Jie-Hong R. Jiang

Graduate Seminar

Algorithms for Model Checking, Winter 2023, with Po-Chun Chien

Undergraduate Course

Formal Languages and Complexity, Summer 2020, instructor: Prof. Dirk Beyer

Introduction to Electronic Design Automation, Spring 2016, instructor: Prof. Jie-Hong R. Jiang

Undergraduate Seminar

Tools for Software Verification, Winter 2021, with Dr. Stefan Winter and Sudeep Kanav

Bachelor's Thesis or Project

Salih Ates, *Improving Array Encoding in Hardware-to-Software Translation*, 2023

Siang-Yun Lee, *Threshold Logic Synthesis and Canonicalization*, 2018-2019

Yen-Shi Wang, *Random-Exist and Exist-Random Stochastic Satisfiability Solving*, 2017-2018

Professional Activities

Conference/Workshop Organizer

The 8th International Workshop on CPAchecker, 2023 (co-chair: Prof. Marie-Christine Jakobs)

Journal Referee

IEEE Transactions on Computers, 2023

International Journal on Software Tools for Technology Transfer, Springer, 2023

ACM Transactions on Design Automation of Electronic Systems, 2023

Formal Methods in System Design, Springer, 2022

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018

Conference Referee

Int. Symposium on Automated Technology for Verification and Analysis (ATVA), 2024

Int. Conference on Computer Design (ICCD), 2023

Int. Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023

AAAI Conference on Artificial Intelligence (AAAI), 2022

Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering (ESEC/FSE), 2022

Annual NASA Formal Methods Symposium (NFM), 2022

Design Automation Conference (DAC), 2022

Int. Conference on Automated Software Engineering (ASE), 2022

AAAI Conference on Artificial Intelligence (AAAI), 2021

Design Automation Conference (DAC), 2021

Int. Conference on Computer-Aided Design (ICCAD), 2021

Int. Conference on Software Engineering and Formal Methods (SEFM), 2020

References

1. Dirk Beyer, Professor, LMU Munich, Munich, Germany, <https://www.sosy-lab.org/people/beyer>

2. Jie-Hong R. Jiang, Professor, NTU, Taipei, Taiwan, <http://cc.ee.ntu.edu.tw/~jhjiang>
3. Victor N. Kravets, Full Researcher, IBM Thomas J. Watson Research Center, NY, U.S.A.

Additional references are available on request.