Nian-Ze Lee

Curriculum Vitae

2023-07-10

Coordinates

Affiliation:	Ludwig-Maximilians-Universität München Software and Computational Systems Lab Oettingenstr. 67, Munich, Germany	Webpage:	www.sosy-lab.org/people/lee/
		Phone:	+49-176-67703045
		Email:	nian-ze.lee@sosy.ifi.lmu.de
Citizenship:	Taiwanese	Year of birth:	1991

Research Interests

My research focuses on the application of formal methods to the analysis and optimization of computing systems, including software programs, conventional VLSI circuits, and emerging technologies. Specifically, I am active in the following directions (tools which I developed or contributed to are given in parentheses):

- Development of new algorithms for software verification (CPACHECKER)
- Verification of sequential digital circuits with software techniques (BTOR2C)
- Stochastic Boolean satisfiability and its application to probabilistic systems (RESSAT and ERSSAT)
- Optimization and verification of threshold logic circuits (TLCOLLAPSEVERIFY)

The theoretical foundation of my work is data structures and algorithms, formal methods, mathematical logic, and system modeling. My goal is to invent new approaches and apply them to real-world challenges. I also put emphasis on tool implementation and reproducible evaluation.

Education

2015 – 2021 Ph.D., Graduate Institute of Electronics Engineering
National Taiwan University, Taipei, Taiwan
Advisor: Prof. Jie-Hong Roland Jiang

- Dissertation: *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*; Lam Research Ph.D. Thesis Award

2009 – 2014 B.Sc. in Eng., Department of Electrical Engineering (minor in Economics)
National Taiwan University, Taipei, Taiwan

Academic Employment

since 2021 Postdoctoral Researcher, Host: Prof. Dirk Beyer
Ludwig-Maximilians-Universität München, Munich, Germany

2019 – 2020 Visiting Student on DAAD Scholarship, Host: Prof. Dirk Beyer
Ludwig-Maximilians-Universität München, Munich, Germany

2018 – 2019 Internship Student in ERATO MMSD Project, Host: Prof. Ichiro Hasuo
National Institute of Informatics, Tokyo, Japan

2015 – 2021 Research and Teaching Assistant, Advisor: Prof. Jie-Hong Roland Jiang
National Taiwan University, Taipei, Taiwan

Industrial Employment

2016 Research Intern, Mentor: Dr. Victor N. Kravets
IBM Thomas J. Watson Research Center, Yorktown Heights, NY, U.S.A.

Software

ABC: Sequential logic synthesis and formal verification
https://github.com/berkeley-abc/abc
Contributor.

BENCHEXEC: Reliable benchmarking and resource measurement
https://github.com/sosy-lab/benchexec
Contributor.

BTOR2C: Translation from word-level circuits to C programs
https://gitlab.com/sosy-lab/software/btor2c
Principal designer, implementer, and maintainer.

CPACHECKER: Configurable software verification
https://gitlab.com/sosy-lab/software/cpachecker
Contributor, conceptual extensions, and implementation of interpolation-based analyses.

RESSAT and ERSSAT: Stochastic satisfiability solvers
https://github.com/NTU-ALComLab/ssatABC
Principal designer, implementer, and maintainer.

TLCOLLAPSEVERIFY: Optimization and verification of threshold logic circuits
https://github.com/NTU-ALComLab/TLCollapseVerify
Principal designer, implementer, and maintainer.

Publications

Books

1. Nian-Ze Lee. *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*. PhD thesis, 2021. doi: 10.6342/NTU202101397.

Journal Papers

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *Journal of Automated Reasoning*, 2023. Accepted, preliminary version available on https://doi.org/10.48550/arXiv.2208.05046.
2. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021. doi: 10.1109/TCAD.2020.3015441.
3. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018. doi: 10.1109/TC.2018.2807431.

Conference Papers (with published proceedings)

1. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. CPA-DF: A tool for configurable interval analysis to boost program verification. In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, 2023. Accepted, preliminary version available on https://doi.org/10.5281/zenodo.7963094.
2. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 13994, pages 152–172. Springer, 2023. doi: 10.1007/978-3-031-30820-8_12.
3. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021. doi: 10.1609/aaai.v35i5.16506.
4. Jie-Hong R. Jiang, Victor N. Kravets, and Nian-Ze Lee. Engineering change order for combinational and sequential design rectification. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition*, pages 726–731. IEEE, 2020. doi: 10.23919/DATE48585.2020.9116504.
5. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Searching parallel separating hyperplanes for effective compression of threshold logic networks. In *Proceedings of the International Conference on Computer-Aided Design*, pages 1–8. ACM, 2019. doi: 10.1109/ICCAD45719.2019.8942143.
6. Nian-Ze Lee, Paolo Arcaini, Shaukat Ali, and Fuyuki Ishikawa. Stability analysis for safety of automotive multi-product lines: A search-based approach. In *Proceedings of the Genetic and Evolutionary Computation Conference*, pages 1241–1249. ACM, 2019. doi: 10.1145/3321707.3321755.

7. Victor N. Kravets, Nian-Ze Lee, and Jie-Hong R. Jiang. Comprehensive search for ECO rectification using symbolic sampling. In *Proceedings of the Annual Design Automation Conference*, pages 71:1–71:6. ACM, 2019. doi: 10.1145/3316781.3317790.
8. Shaukat Ali, Paolo Arcaini, Ichiro Hasuo, Fuyuki Ishikawa, and Nian-Ze Lee. Towards a framework for the analysis of multi-product lines in the automotive domain. In *Proceedings of the International Workshop on Variability Modelling of Software-Intensive Systems*, pages 12:1–12:6. ACM, 2019. doi: 10.1145/3302333.3302345.
9. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Canonicalization of threshold logic representation and its applications. In *Proceedings of the International Conference on Computer-Aided Design*, pages 85:1–85:8. ACM, 2018. doi: 10.1145/3240765.3240785.
10. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving exist-random quantified stochastic Boolean satisfiability via clause selection. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 1339–1345. IJCAI Organization, 2018. doi: 10.24963/ijcai.2018/186.
11. Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, and Robert K. Brayton. Efficient computation of ECO patch functions. In *Proceedings of the Annual Design Automation Conference*, pages 51:1–51:6. ACM, 2018. doi: 10.1145/3195970.3196039.
12. Nian-Ze Lee, Victor N. Kravets, and Jie-Hong R. Jiang. Sequential engineering change order under retiming and resynthesis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 109–116. IEEE, 2017. doi: 10.1109/ICCAD.2017.8203767.
13. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving stochastic Boolean satisfiability under random-exist quantification. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 688–694. IJCAI Organization, 2017. doi: 10.24963/ijcai.2017/96.
14. Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Analytic approaches to the collapse operation and equivalence verification of threshold logic circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 5:1–5:8. ACM, 2016. doi: 10.1145/2966986.2967001.
15. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. In *Proceedings of the International Conference on Computer-Aided Design*, pages 340–347. IEEE, 2014. doi: 10.1109/ICCAD.2014.7001372.

Technical Reports

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *arXiv/CoRR*, 2208(05046), July 2022. doi: 10.48550/arXiv.2208.05046.

University Activities

Teaching Assistant at LMU Munich and NTU

Graduate courses:

Software Verification, Summer 2023, Prof. Dirk Beyer

Software Verification, Winter 2021/22, Prof. Dirk Beyer

Methods in Software Engineering, Summer 2022, Prof. Gidon Ernst

Logic Synthesis and Verification, Fall 2020, Prof. Jie-Hong Roland Jiang

Logic Synthesis and Verification, Fall 2018, Prof. Jie-Hong Roland Jiang

Undergraduate courses:

Introduction to Electronic Design Automation, Spring 2016, Prof. Jie-Hong Roland Jiang

Graduate seminars:

Reproducibility of Software Engineering Research, Winter 2022/23, with Dr. Stefan Winter

Undergraduate seminars:

Tools for Software Verification, Winter 2021/22, with Dr. Stefan Winter and Sudeep Kanav

Professional Activities

Conference/Workshop Organizer

The 8th International Workshop on CPAchecker, 2023 (co-chair: Prof. Marie-Christine Jakobs).

Journal Referee

International Journal on Software Tools for Technology Transfer, Springer, 2023.

ACM Transactions on Design Automation of Electronic Systems, 2023.

Formal Methods in System Design, Springer, 2022.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018.

Conference Referee

Int. Conf. on Computer Design (ICCD), 2023

Int. Conf. on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023

AAAI Conf. on Artificial Intelligence (AAAI), 2022.

Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering (ESEC/FSE), 2022

Annual NASA Formal Methods Symposium (NFM), 2022.

Design Automation Conference (DAC), 2022.

Int. Conf. on Automated Software Engineering (ASE), 2022

AAAI Conf. on Artificial Intelligence (AAAI), 2021.

Design Automation Conference (DAC), 2021.

Int. Conf. on Computer-Aided Design (ICCAD), 2021.

Int. Conf. on Software Engineering and Formal Methods (SEFM), 2020.

References

1. Dirk Beyer, Professor, LMU Munich, Germany, https://www.sosy-lab.org/people/beyer/
2. Jie-Hong Roland Jiang, Professor, NTU, Taipei, Taiwan, http://cc.ee.ntu.edu.tw/∼jhjiang/
3. Victor N. Kravets, Full Researcher, IBM Thomas J. Watson Research Center, NY, U.S.A.

Additional references are available on request.