List of Publications

2025-11-11

Statistics: h-index 12; 5 journal papers and 25 peer-reviewed conference papers in prestigious venues, including the **Proceedings of the ACM on Software Engineering** and **IEEE Transactions on Computers**.

My five recent and most important publications are highlighted in boldface.

Books

1. Nian-Ze Lee. *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*. PhD thesis, 2021. doi: 10.6342/NTU202101397.

Journal Papers

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. **Interpolation and SAT-Based Model Checking Revisited: Adoption to Software Verification**. *Journal of Automated Reasoning*, 69(1):5, 2025. doi: 10.1007/s10817-024-09702-9.
2. Dirk Beyer, Po-Chun Chien, Marek Jankola, and Nian-Ze Lee. **A Transferability Study of Interpolation-Based Hardware Model Checking for Software Verification**. *Proceedings of the ACM on Software Engineering*, 1(FSE):90:1–90:23, 2024. doi: 10.1145/3660797.
3. Marie-Christine Jakobs and Nian-Ze Lee. Summary of the eighth international workshop on CPAchecker (CPAchecker 2023). *ACM SIGSOFT Software Engineering Notes*, 49(2):25–26, 2024. doi: 10.1145/3650142.3650150.
4. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021. doi: 10.1109/TCAD.2020.3015441.
5. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018. doi: 10.1109/TC.2018.2807431.

Conference Papers (with published proceedings)

1. Zhengyang Lu, Po-Chun Chien, Nian-Ze Lee, Arie Gurfinkel, and Vijay Ganesh. Btor2-Select: Machine learning based algorithm selection for hardware model checking. In *Proceedings of the International Conference on Computer Aided Verification*, LNCS 15931, pages 296–311. Springer, 2025. doi: 10.1007/978-3-031-98668-0_15.
2. Zhengyang Lu, Po-Chun Chien, Nian-Ze Lee, and Vijay Ganesh. Algorithm selection for word-level hardware model checking (student abstract). In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 29426–29427. AAAI Press, 2025. doi: 10.1609/AAAI.V39I28.35275.
3. Salih Ates, Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. MoXIchecker: An extensible model checker for MoXI. In *Proceedings of the International Conference on Verified Software: Theories, Tools, and Experiments*, LNCS 15525, pages 1–14. Springer, 2024. doi: 10.1007/978-3-031-86695-1_1.
4. Dirk Beyer and Nian-Ze Lee. The transformation game: Joining forces for verification. In *Principles of Verification: Cycling the Probabilistic Landscape - Essays Dedicated to Joost-Pieter Katoen on the Occasion of His 60th Birthday, Part III*, LNCS 15262, pages 175–205. Springer, 2024. doi: 10.1007/978-3-031-75778-5_9.
5. Daniel Baier, Dirk Beyer, Po-Chun Chien, Marie-Christine Jakobs, Marek Jankola, Matthias Kettl, Nian-Ze Lee, Thomas Lemberger, Marian Lingsch Rosenfeld, Henrik Wachowitz, and Philipp Wendler. Software verification with CPAchecker 3.0: Tutorial and user guide. In *Proceedings of the International Symposium on Formal Methods*, LNCS 14934, pages 543–570. Springer, 2024. doi: 10.1007/978-3-031-71177-0_30.
6. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. **Augmenting Interpolation-Based Model Checking with Auxiliary Invariants**. In *Proceedings of the International Symposium on Model Checking Software*, LNCS 14624, pages 227–247. Springer, 2024. doi: 10.1007/978-3-031-66149-5_13.
7. Zsófia Ádám, Dirk Beyer, Po-Chun Chien, Nian-Ze Lee, and Nils Sirrenberg. **Btor2-Cert: A Certifying Hardware-Verification Framework Using Software Analyzers**. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 14572, pages 129–149. Springer, 2024. doi: 10.1007/978-3-031-57256-2_7.

8. Po-Chun Chien and Nian-Ze Lee. CPV: A circuit-based program verifier (competition contribution). In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 14572, pages 365–370. Springer, 2024. doi: 10.1007/978-3-031-57256-2_22.
9. Daniel Baier, Dirk Beyer, Po-Chun Chien, Marek Jankola, Matthias Kettl, Nian-Ze Lee, Thomas Lemberger, Marian Lingsch-Rosenfeld, Martin Spiessl, Henrik Wachowitz, and Philipp Wendler. CPAchecker 2.3 with strategy selection (competition contribution). In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 14572, pages 359–364. Springer, 2024. doi: 10.1007/978-3-031-57256-2_21.
10. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. CPA-DF: A tool for configurable interval analysis to boost program verification. In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, pages 2050–2053. IEEE, 2023. doi: 10.1109/ASE56229.2023.00213.
11. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with Btor2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 13994, pages 152–172. Springer, 2023. doi: 10.1007/978-3-031-30820-8_12.
12. Nian-Ze Lee and Jie-Hong R. Jiang. **Dependency Stochastic Boolean Satisfiability: A Logical Formalism for NEXPTIME Decision Problems with Uncertainty**. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021. doi: 10.1609/aaai.v35i5.16506.
13. Jie-Hong R. Jiang, Victor N. Kravets, and Nian-Ze Lee. Engineering change order for combinational and sequential design rectification. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition*, pages 726–731. IEEE, 2020. doi: 10.23919/DATE48585.2020.9116504.
14. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Searching parallel separating hyperplanes for effective compression of threshold logic networks. In *Proceedings of the International Conference on Computer-Aided Design*, pages 1–8. ACM, 2019. doi: 10.1109/ICCAD45719.2019.8942143.
15. Nian-Ze Lee, Paolo Arcaini, Shaukat Ali, and Fuyuki Ishikawa. Stability analysis for safety of automotive multi-product lines: A search-based approach. In *Proceedings of the Genetic and Evolutionary Computation Conference*, pages 1241–1249. ACM, 2019. doi: 10.1145/3321707.3321755.
16. Victor N. Kravets, Nian-Ze Lee, and Jie-Hong R. Jiang. Comprehensive search for ECO rectification using symbolic sampling. In *Proceedings of the Annual Design Automation Conference*, pages 71:1–71:6. ACM, 2019. doi: 10.1145/3316781.3317790.
17. Shaukat Ali, Paolo Arcaini, Ichiro Hasuo, Fuyuki Ishikawa, and Nian-Ze Lee. Towards a framework for the analysis of multi-product lines in the automotive domain. In *Proceedings of the International Workshop on Variability Modelling of Software-Intensive Systems*, pages 12:1–12:6. ACM, 2019. doi: 10.1145/3302333.3302345.
18. Akihisa Yamada, Clovis Eberhart, Fuyuki Ishikawa, and Nian-Ze Lee. Scenario sampling for cyber physical systems using combinatorial testing. In *Proceedings of the International Conference on Software Testing, Verification and Validation Workshops*, pages 198–199. IEEE, 2019. doi: 10.1109/ICSTW.2019.00053.
19. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Canonicalization of threshold logic representation and its applications. In *Proceedings of the International Conference on Computer-Aided Design*, pages 85:1–85:8. ACM, 2018. doi: 10.1145/3240765.3240785.
20. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving exist-random quantified stochastic Boolean satisfiability via clause selection. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 1339–1345. IJCAI Organization, 2018. doi: 10.24963/ijcai.2018/186.
21. Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, and Robert K. Brayton. Efficient computation of ECO patch functions. In *Proceedings of the Annual Design Automation Conference*, pages 51:1–51:6. ACM, 2018. doi: 10.1145/3195970.3196039.
22. Nian-Ze Lee, Victor N. Kravets, and Jie-Hong R. Jiang. Sequential engineering change order under retiming and resynthesis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 109–116. IEEE, 2017. doi: 10.1109/ICCAD.2017.8203767.
23. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving stochastic Boolean satisfiability under random-exist quantification. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 688–694. IJCAI Organization, 2017. doi: 10.24963/ijcai.2017/96.
24. Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Analytic approaches to the collapse operation and equivalence verification of threshold logic circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 5:1–5:8. ACM, 2016. doi: 10.1145/2966986.2967001.

25. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. In *Proceedings of the International Conference on Computer-Aided Design*, pages 340–347. IEEE, 2014. doi: 10.1109/ICCAD.2014.7001372.

Technical Reports

1. Daniel Baier, Dirk Beyer, Po-Chun Chien, Marie-Christine Jakobs, Marek Jankola, Matthias Kettl, Nian-Ze Lee, Thomas Lemberger, Marian Lingsch Rosenfeld, Henrik Wachowitz, and Philipp Wendler. Software verification with CPAchecker 3.0: Tutorial and user guide (extended version). *arXiv/CoRR*, 2409, 2024. doi: 10.48550/arXiv.2409.02094.
2. Salih Ates, Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. MoXIchecker: An extensible model checker for MoXI. *arXiv/CoRR*, 2407(15551), July 2024. doi: 10.48550/arXiv.2407.15551.
3. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Augmenting interpolation-based model checking with auxiliary invariants (extended version). *arXiv/CoRR*, 2403(07821), March 2024. doi: 10.48550/arXiv.2403.07821.
4. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *arXiv/CoRR*, 2208(05046), July 2022. doi: 10.48550/arXiv.2208.05046.
5. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. *arXiv/CoRR*, 1911(04112), February 2021. doi: 10.48550/arXiv.1911.04112.

Submitted Manuscripts

1. Dirk Beyer, Po-Chun Chien, Bo-Yuan Huang, Nian-Ze Lee, and Thomas Lemberger. A case study in firmware verification: Applying formal methods to Intel TDX Module. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*. Springer, 2026. Submitted on 2025-10-17, under review.
2. Dirk Beyer, Po-Chun Chien, Bo-Yuan Huang, Nian-Ze Lee, and Thomas Lemberger. HarnessForge: Automated extraction of verification tasks from industry-scale software projects. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*. Springer, 2026. Submitted on 2025-10-17, under review.
3. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Augmenting interpolation-based model checking with auxiliary invariants. *International Journal on Software Tools for Technology Transfer*. Invited submission, conditionally accepted on 2025-05-26.
4. Salih Ates, Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with Btor2C: A word-level-circuit-to-C translator. *International Journal on Software Tools for Technology Transfer*. Invited submission, accepted on 2025-05-14.

Reproduction Packages

1. Dirk Beyer, Po-Chun Chien, Bo-Yuan Huang, Nian-Ze Lee, and Thomas Lemberger. The Intel TDX Module benchmark set (version 1.0). Zenodo, 2025. doi: 10.5281/zenodo.16547223.
2. Zhengyang John Lu, Po-Chun Chien, Nian-Ze Lee, Arie Gurfinkel, and Vijay Ganesh. Reproduction package for CAV 2025 article 'Btor2-Select: Machine learning based algorithm selection for hardware model checking'. Zenodo, 2025. doi: 10.5281/zenodo.15485472.
3. Dirk Beyer, Po-Chun Chien, Marek Jankola, and Nian-Ze Lee. Reproduction package for FSE 2024 article 'A transferability study of interpolation-based hardware model checking for software verification'. Zenodo, 2024. doi: 10.5281/zenodo.11070973.
4. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for SPIN 2024 submission 'Augmenting interpolation-based model checking with auxiliary invariants'. Zenodo, 2024. doi: 10.5281/zenodo.10548594.
5. Zsófia Ádám, Dirk Beyer, Po-Chun Chien, Nian-Ze Lee, and Nils Sirrenberg. Reproduction package for TACAS 2024 article 'Btor2-Cert: A certifying hardware-verification framework using software analyzers'. Zenodo, 2024. doi: 10.5281/zenodo.10548597.
6. Zsófia Ádám, Dirk Beyer, Po-Chun Chien, Nian-Ze Lee, and Nils Sirrenberg. Reproduction package for TACAS 2024 submission 'Btor2-Cert: A certifying hardware-verification framework using software analyzers'. Zenodo, 2023. doi: 10.5281/zenodo.10013059.
7. Po-Chun Chien and Nian-Ze Lee. CPV: A circuit-based program verifier. Zenodo, 2023. doi: 10.5281/zenodo.10203472.

8. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for ASE 2023 article 'CPA-DF: A tool for configurable interval analysis to boost program verification'. Zenodo, 2023. doi: 10.5281/zenodo.8245821.
9. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for TACAS 2023 article 'Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator'. Zenodo, 2023. doi: 10.5281/zenodo.7551707.
10. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Reproduction package for JAR article 'Interpolation and SAT-based model checking revisited'. Zenodo, 2023. doi: 10.5281/zenodo.8245824.
11. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for TACAS 2023 submission 'Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator'. Zenodo, 2022. doi: 10.5281/zenodo.7303732.
12. Nian-Ze Lee. Reproduction package for doctoral dissertation 'Stochastic Boolean satisfiability: Decision procedures, generalization, and applications'. Zenodo, 2021. doi: 10.5281/zenodo.5084146.