# Nian-Ze Lee

## Curriculum Vitae

2023-09-30

## Coordinates


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| Affiliation: | Ludwig-Maximilians-Universität München<br>Software and Computational Systems Lab<br>Oettingenstr. 67, Munich, Germany | Webpage: | nianzelee.github.io |
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| Citizenship: | Taiwanese | Year of birth: | 1991 |


## Research Interests

My research focuses on the application of formal methods to the analysis and optimization of computing systems, including software programs, VLSI circuits, and emerging technologies. Specifically, I am active in the following directions (tools which I developed or contributed to are given in parentheses):

- Development of new algorithms for software verification (CPACHECKER)
- Verification of sequential digital circuits with software techniques (BTOR2C)
- Stochastic Boolean satisfiability and its application to probabilistic systems (RESSAT and ERSSAT)
- Optimization and verification of threshold logic circuits (TLCOLLAPSEVERIFY)

The theoretical foundation of my work is algorithms and data structures, formal methods, mathematical logic, and system modeling. My goal is to invent new approaches and apply them to real-world challenges. I also emphasize software engineering for tool implementation and reproducible evaluation.

## Education

2015 – 2021 **Ph.D., Graduate Institute of Electronics Engineering**
National Taiwan University, Taipei, Taiwan
Advisor: Prof. Jie-Hong R. Jiang

**Lam Research Thesis Award**

Dissertation: *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*

2009 – 2014 **B.Sc. in Eng., Department of Electrical Engineering**
Minor in Economics
National Taiwan University, Taipei, Taiwan

## Academic Employment

since 2021 **Postdoctoral Researcher**, Host: Prof. Dirk Beyer
Ludwig-Maximilians-Universität München, Munich, Germany

2019 – 2020 **DAAD Scholarship Student**, Host: Prof. Dirk Beyer
Ludwig-Maximilians-Universität München, Munich, Germany

2018 – 2019 **Internship Student in ERATO MMSD Project**, Host: Prof. Ichiro Hasuo
National Institute of Informatics, Tokyo, Japan

2015 – 2021 **Research and Teaching Assistant**, Advisor: Prof. Jie-Hong R. Jiang
National Taiwan University, Taipei, Taiwan

## Industrial Employment

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| 2016 | **Research Intern**, Mentor: Dr. Victor N. Kravets<br>IBM Thomas J. Watson Research Center, Yorktown Heights, NY, U.S.A. |

## Awards and Honors

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| 2022 | **Best Master Lecture**<br>*Methods in Software Engineering*, instructor: Prof. Gidon Ernst |
| 2021 | **Lam Research Ph.D. Thesis Award**<br>Dissertation title: *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications* |
| 2021 | **Honorary Member of the Phi Tau Phi Scholastic Honor Society**<br>Achievement of academic excellence upon graduation |

## Grants

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| 2023 | **German Research Foundation (DFG)**, submitted in July<br>Research funding, requested € 300 K (1 Ph.D. position) |
| 2023 | **LMUexcellent PostDoc Support Fund**<br>Travel funding, € 6.5 K |
| 2019-2020 | **German Academic Exchange Service (DAAD)**<br>Joint scholarship with National Science and Technology Council, € 15 K |

## Important Publications

*h-Index: 8, more than 15 peer-reviewed publications in top-tier conferences and journals*

The complete list of my peer-reviewed publications can be found via

- My personal website: https://nianzelee.github.io
- DBLP: https://dblp.org/pid/154/3010.html
- Google Scholar: https://scholar.google.com/citations?user=_8OD03gAAAAJ

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *Journal of Automated Reasoning*, 2023. Accepted, preliminary version available on https://doi.org/10.48550/arXiv.2208.05046.
2. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. CPA-DF: A tool for configurable interval analysis to boost program verification. In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, 2023. Accepted, preliminary version available on https://doi.org/10.5281/zenodo.7963094.
3. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 13994, pages 152–172. Springer, 2023. doi: 10.1007/978-3-031-30820-8_12.
4. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021. doi: 10.1609/aaai.v35i5.16506.
5. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021. doi: 10.1109/TCAD.2020.3015441.
6. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018. doi: 10.1109/TC.2018.2807431.

## Software

ABC: Sequential logic synthesis and formal verification
https://github.com/berkeley-abc/abc
Contributor

BenchExec: Reliable benchmarking and resource measurement
https://github.com/sosy-lab/benchexec
Contributor

Btor2C: Translation from word-level circuits to C programs
https://gitlab.com/sosy-lab/software/btor2c
Principal designer, implementer, and maintainer

CPAchecker: Configurable software verification
https://cpachecker.sosy-lab.org
Contributor, conceptual extensions, and implementation of interpolation-based analyses

reSSAT and erSSAT: Stochastic satisfiability solvers
https://github.com/NTU-ALComLab/ssatABC
Principal designer, implementer, and maintainer

TLCollapseVerify: Optimization and verification of threshold logic circuits
https://github.com/NTU-ALComLab/TLCollapseVerify
Principal designer, implementer, and maintainer

## Student Supervision

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| 2021- | Po-Chun Chien, **DFG RTG ConVeY**<br>Ph.D. student, LMU Munich<br>Topic: Bridging hardware and software verification |
| 2023 | Ádám Zófia, **Erasmus Program**<br>Ph.D. student, Budapest University of Technology and Economics<br>Topic: Witness validation for hardware-translated programs |
| 2023 | Bastiaan Laarakker, **Google Summer of Code**<br>Master student, University of Amsterdam<br>Topic: Backward bounded model checking in CPAchecker |

## University Activities

### Teaching Assistant at LMU Munich, since 2020

*Graduate courses:*

*Software Verification*, Summer 2023, instructor: Prof. Dirk Beyer

*Methods in Software Engineering*, Summer 2022, instructor: Prof. Gidon Ernst
(**Best Master Lecture** at Institute of Informatics)

*Software Verification*, Winter 2021, instructor: Prof. Dirk Beyer

*Undergraduate courses:*

*Formal Languages and Complexity*, Summer 2020, instructor: Prof. Dirk Beyer

*Graduate seminars:*

*Reproducibility of Software Engineering Research*, Winter 2022, with Dr. Stefan Winter

*Undergraduate seminars:*

*Tools for Software Verification*, Winter 2021, with Dr. Stefan Winter and Sudeep Kanav

*Bachelor's Thesis or Project:*

Salih Ates, *Improving Array Encoding in Hardware-to-Software Translation*, 2023

### Teaching Assistant at National Taiwan University, 2016-2021

*Graduate courses:*

*Logic Synthesis and Verification*, Fall 2020, instructor: Prof. Jie-Hong R. Jiang

*Logic Synthesis and Verification*, Fall 2018, instructor: Prof. Jie-Hong R. Jiang

*Undergraduate courses:*

*Introduction to Electronic Design Automation*, Spring 2016, instructor: Prof. Jie-Hong R. Jiang

*Bachelor's Thesis or Project:*

Siang-Yun Lee, *Threshold Logic Synthesis and Canonicalization*, 2018-2019

Yen-Shi Wang, *Random-Exist and Exist-Random Stochastic Satisfiability Solving*, 2017-2018

## Professional Activities

### Conference/Workshop Organizer

The 8th International Workshop on CPAchecker, 2023 (co-chair: Prof. Marie-Christine Jakobs)

### Journal Referee

International Journal on Software Tools for Technology Transfer, Springer, 2023

ACM Transactions on Design Automation of Electronic Systems, 2023

Formal Methods in System Design, Springer, 2022

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018

### Conference Referee

Int. Conf. on Computer Design (ICCD), 2023

Int. Conf. on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023

AAAI Conf. on Artificial Intelligence (AAAI), 2022

Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering (ESEC/FSE), 2022

Annual NASA Formal Methods Symposium (NFM), 2022

Design Automation Conference (DAC), 2022

Int. Conf. on Automated Software Engineering (ASE), 2022

AAAI Conf. on Artificial Intelligence (AAAI), 2021

Design Automation Conference (DAC), 2021

Int. Conf. on Computer-Aided Design (ICCAD), 2021

Int. Conf. on Software Engineering and Formal Methods (SEFM), 2020

## References


1. Dirk Beyer, Professor, LMU Munich, Germany, https://www.sosy-lab.org/people/beyer
2. Jie-Hong R. Jiang, Professor, NTU, Taipei, Taiwan, http://cc.ee.ntu.edu.tw/∼jhjiang
3. Victor N. Kravets, Full Researcher, IBM Thomas J. Watson Research Center, NY, U.S.A.


Additional references are available on request.