

# List of Publications

2023-10-24

*h-Index: 8, more than 15 peer-reviewed publications in top-tier conferences and journals*

The complete list of my peer-reviewed publications can be found via

- My personal website: <https://nianzelee.github.io>
- DBLP: <https://dblp.org/pid/154/3010.html>
- Google Scholar: [https://scholar.google.com/citations?user=\\_8OD03gAAAAJ](https://scholar.google.com/citations?user=_8OD03gAAAAJ)

## Books

---

1. Nian-Ze Lee. *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*. PhD thesis, 2021. doi: [10.6342/NTU202101397](https://doi.org/10.6342/NTU202101397).

## Journal Papers

---

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *Journal of Automated Reasoning*, 2023. Accepted, preliminary version available on <https://doi.org/10.48550/arXiv.2208.05046>.
2. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021. doi: [10.1109/TCAD.2020.3015441](https://doi.org/10.1109/TCAD.2020.3015441).
3. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018. doi: [10.1109/TC.2018.2807431](https://doi.org/10.1109/TC.2018.2807431).

## Conference Papers (with published proceedings)

---

1. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. CPA-DF: A tool for configurable interval analysis to boost program verification. In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, 2023. Accepted, preliminary version available on <https://doi.org/10.5281/zenodo.7963094>.
2. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS 13994, pages 152–172. Springer, 2023. doi: [10.1007/978-3-031-30820-8\\_12](https://doi.org/10.1007/978-3-031-30820-8_12).
3. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021. doi: [10.1609/aaai.v35i5.16506](https://doi.org/10.1609/aaai.v35i5.16506).
4. Jie-Hong R. Jiang, Victor N. Kravets, and Nian-Ze Lee. Engineering change order for combinational and sequential design rectification. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition*, pages 726–731. IEEE, 2020. doi: [10.23919/DATe48585.2020.9116504](https://doi.org/10.23919/DATe48585.2020.9116504).
5. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Searching parallel separating hyperplanes for effective compression of threshold logic networks. In *Proceedings of the International Conference on Computer-Aided Design*, pages 1–8. ACM, 2019. doi: [10.1109/ICCAD45719.2019.8942143](https://doi.org/10.1109/ICCAD45719.2019.8942143).
6. Nian-Ze Lee, Paolo Arcaini, Shaukat Ali, and Fuyuki Ishikawa. Stability analysis for safety of automotive multi-product lines: A search-based approach. In *Proceedings of the Genetic and Evolutionary Computation Conference*, pages 1241–1249. ACM, 2019. doi: [10.1145/3321707.3321755](https://doi.org/10.1145/3321707.3321755).

7. Victor N. Kravets, Nian-Ze Lee, and Jie-Hong R. Jiang. Comprehensive search for ECO rectification using symbolic sampling. In *Proceedings of the Annual Design Automation Conference*, pages 71:1–71:6. ACM, 2019. doi: [10.1145/3316781.3317790](https://doi.org/10.1145/3316781.3317790).
8. Shaukat Ali, Paolo Arcaini, Ichiro Hasuo, Fuyuki Ishikawa, and Nian-Ze Lee. Towards a framework for the analysis of multi-product lines in the automotive domain. In *Proceedings of the International Workshop on Variability Modelling of Software-Intensive Systems*, pages 12:1–12:6. ACM, 2019. doi: [10.1145/3302333.3302345](https://doi.org/10.1145/3302333.3302345).
9. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Canonicalization of threshold logic representation and its applications. In *Proceedings of the International Conference on Computer-Aided Design*, pages 85:1–85:8. ACM, 2018. doi: [10.1145/3240765.3240785](https://doi.org/10.1145/3240765.3240785).
10. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving exist-random quantified stochastic Boolean satisfiability via clause selection. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 1339–1345. IJCAI Organization, 2018. doi: [10.24963/ijcai.2018/186](https://doi.org/10.24963/ijcai.2018/186).
11. Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, and Robert K. Brayton. Efficient computation of ECO patch functions. In *Proceedings of the Annual Design Automation Conference*, pages 51:1–51:6. ACM, 2018. doi: [10.1145/3195970.3196039](https://doi.org/10.1145/3195970.3196039).
12. Nian-Ze Lee, Victor N. Kravets, and Jie-Hong R. Jiang. Sequential engineering change order under retiming and resynthesis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 109–116. IEEE, 2017. doi: [10.1109/ICCAD.2017.8203767](https://doi.org/10.1109/ICCAD.2017.8203767).
13. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving stochastic Boolean satisfiability under random-exist quantification. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 688–694. IJCAI Organization, 2017. doi: [10.24963/ijcai.2017/96](https://doi.org/10.24963/ijcai.2017/96).
14. Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Analytic approaches to the collapse operation and equivalence verification of threshold logic circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 5:1–5:8. ACM, 2016. doi: [10.1145/2966986.2967001](https://doi.org/10.1145/2966986.2967001).
15. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. In *Proceedings of the International Conference on Computer-Aided Design*, pages 340–347. IEEE, 2014. doi: [10.1109/ICCAD.2014.7001372](https://doi.org/10.1109/ICCAD.2014.7001372).

## Technical Reports

---

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *arXiv/CoRR*, 2208(05046), July 2022. doi: [10.48550/arXiv.2208.05046](https://doi.org/10.48550/arXiv.2208.05046).

## Reproduction Packages

---

1. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for ASE 2023 article ‘CPA-DF: A tool for configurable interval analysis to boost program verification’. Zenodo, 2023. doi: [10.5281/zenodo.8245821](https://doi.org/10.5281/zenodo.8245821).
2. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Reproduction package for TACAS 2023 article ‘Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator’. Zenodo, 2023. doi: [10.5281/zenodo.7551707](https://doi.org/10.5281/zenodo.7551707).
3. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Reproduction package for JAR article ‘Interpolation and SAT-based model checking revisited’. Zenodo, 2023. doi: [10.5281/zenodo.8245824](https://doi.org/10.5281/zenodo.8245824).