

Nian-Ze Lee

Curriculum Vitae

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Coordinates

Affiliation:	Ludwig-Maximilians-Universität München Software and Computational Systems Lab Oettingenstr. 67, Munich, Germany	Webpage:	www.sosy-lab.org/people/lee/
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Citizenship:	Taiwanese	Year of birth:	1991

Research Interests

My research focuses on the application of formal methods to the analysis and optimization of computational models, including software systems, conventional VLSI circuits, and emerging technologies. In particular, I am active in the following directions (tools which I developed or contributed to are given in parentheses):

- Development of new algorithms for software verification (CPACHECKER)
- Verification of word-level hardware with software techniques (BTOR2C)
- Stochastic Boolean satisfiability and its application to probabilistic systems (RESSAT and ERSSAT)
- Optimization and verification of threshold logic circuits (TLCOLLAPSEVERIFY)

The theoretical foundation of my work is data structures and algorithms, formal methods, mathematical logic, and system modeling. My goal is to invent new approaches and apply them to real-world challenges. I also put emphasis on tool implementation and reproducible evaluation.

Education

2015 – 2021	Ph.D., Graduate Institute of Electronics Engineering National Taiwan University, Taipei, Taiwan <ul style="list-style-type: none">• Dissertation: <i>Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications</i>; Lam Research Ph.D. Thesis Award
2009 – 2013	B.Sc. in Eng., Department of Electrical Engineering (minor in Economics) National Taiwan University, Taipei, Taiwan

Academic Employment

since 2021	Postdoctoral Researcher, Host: Prof. Dirk Beyer Ludwig-Maximilians-Universität München, Munich, Germany
2019 – 2020	Visiting Student on DAAD Scholarship, Host: Prof. Dirk Beyer Ludwig-Maximilians-Universität München, Munich, Germany
2018 – 2019	Internship Student in ERATO MMSD Project, Host: Prof. Ichiro Hasuo National Institute of Informatics, Tokyo, Japan
2015 – 2021	Research and Teaching Assistant, Advisor: Prof. Jie-Hong Roland Jiang National Taiwan University, Taipei, Taiwan

Industrial Employment

2016 – 2016	Research Intern, Mentor: Dr. Victor N. Kravets IBM Thomas J. Watson Research Center, Yorktown Heights, NY, U.S.A.
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Software

ABC: Sequential logic synthesis and formal verification

<https://github.com/berkeley-abc/abc>

Contributor.

BENCHEXEC: Reliable benchmarking and resource measurement

<https://github.com/sosy-lab/benchexec>

Contributor.

BTOR2C: Translation from word-level circuits to C programs

<https://gitlab.com/sosy-lab/software/btor2c>

Principal designer, implementer, and maintainer.

CPACHECKER: Configurable software verification

<https://gitlab.com/sosy-lab/software/cpachecker>

Contributor, conceptual extensions, and implementation of interpolation-based analyses.

RESSAT and ERSSAT: Stochastic satisfiability solvers

<https://github.com/NTU-ALComLab/ssatABC>

Principal designer, implementer, and maintainer.

TLCOLLAPSEVERIFY: Optimization and verification of threshold logic circuits

<https://github.com/NTU-ALComLab/TLCollapseVerify>

Principal designer, implementer, and maintainer.

Publications

Books

1. Nian-Ze Lee. *Stochastic Boolean Satisfiability: Decision Procedures, Generalization, and Applications*. National Taiwan University, 2021. Dissertation.

Journal Papers

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *Journal of Automated Reasoning*, 2023. Under review.
2. Nian-Ze Lee and Jie-Hong R. Jiang. Constraint solving for synthesis and verification of threshold logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(5):904–917, 2021.
3. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. *IEEE Transactions on Computers*, 67(8):1202–1216, 2018.

Conference Papers (with published proceedings)

1. Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee. Bridging hardware and software analysis with BTOR2C: A word-level-circuit-to-C translator. In *Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, LNCS . Springer, 2023.
2. Nian-Ze Lee and Jie-Hong R. Jiang. Dependency stochastic Boolean satisfiability: A logical formalism for NEXPTIME decision problems with uncertainty. In *Proceedings of the AAAI Conference on Artificial Intelligence*, pages 3877–3885. AAAI Press, 2021.
3. Jie-Hong R. Jiang, Victor N. Kravets, and Nian-Ze Lee. Engineering change order for combinational and sequential design rectification. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition*, pages 726–731. IEEE, 2020.
4. Shaukat Ali, Paolo Arcaini, Ichiro Hasuo, Fuyuki Ishikawa, and Nian-Ze Lee. Towards a framework for the analysis of multi-product lines in the automotive domain. In *Proceedings of the International Workshop on Variability Modelling of Software-Intensive Systems*, pages 12:1–12:6. ACM, 2019.
5. Victor N. Kravets, Nian-Ze Lee, and Jie-Hong R. Jiang. Comprehensive search for ECO rectification using symbolic sampling. In *Proceedings of the Annual Design Automation Conference*, pages 71:1–71:6. ACM, 2019.
6. Nian-Ze Lee, Paolo Arcaini, Shaukat Ali, and Fuyuki Ishikawa. Stability analysis for safety of automotive multi-product lines: A search-based approach. In *Proceedings of the Genetic and Evolutionary Computation Conference*, pages 1241–1249. ACM, 2019.
7. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Searching parallel separating hyperplanes for effective compression of threshold logic networks. In *Proceedings of the International Conference on Computer-Aided Design*, pages 1–8. ACM, 2019.

8. Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, and Robert K. Brayton. Efficient computation of ECO patch functions. In *Proceedings of the Annual Design Automation Conference*, pages 51:1–51:6. ACM, 2018.
9. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving exist-random quantified stochastic Boolean satisfiability via clause selection. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 1339–1345. IJCAI Organization, 2018.
10. Siang-Yun Lee, Nian-Ze Lee, and Jie-Hong R. Jiang. Canonicalization of threshold logic representation and its applications. In *Proceedings of the International Conference on Computer-Aided Design*, pages 85:1–85:8. ACM, 2018.
11. Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving stochastic Boolean satisfiability under random-exist quantification. In *Proceedings of the International Joint Conference on Artificial Intelligence*, pages 688–694. IJCAI Organization, 2017.
12. Nian-Ze Lee, Victor N. Kravets, and Jie-Hong R. Jiang. Sequential engineering change order under retiming and resynthesis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 109–116. IEEE, 2017.
13. Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Analytic approaches to the collapse operation and equivalence verification of threshold logic circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 5:1–5:8. ACM, 2016.
14. Nian-Ze Lee and Jie-Hong R. Jiang. Towards formal evaluation and verification of probabilistic design. In *Proceedings of the International Conference on Computer-Aided Design*, pages 340–347. IEEE, 2014.

Technical Reports

1. Dirk Beyer, Nian-Ze Lee, and Philipp Wendler. Interpolation and SAT-based model checking revisited: Adoption to software verification. *arXiv/CoRR*, 2208(05046), July 2022.

University Activities

Teaching Assistant at LMU Munich and NTU

Graduate courses:

Methods in Software Engineering, Prof. Gidon Ernst
Summer 2022

Software Verification, Prof. Dirk Beyer
Summer 2023 and Winter 2021/22

Logic Synthesis and Verification, Prof. Jie-Hong Roland Jiang
Fall 2018 and Fall 2020

Undergraduate courses:

Introduction to Electronic Design Automation, Prof. Jie-Hong Roland Jiang
Spring 2016

Graduate seminars:

Reproducibility of Software Engineering Research, with Dr. Stefan Winter
Winter 2022/23

Undergraduate seminars:

Tools for Software Verification, with Dr. Stefan Winter and Sudeep Kanav
Winter 2021/22

Professional Activities

Journal Referee

ACM Transactions on Design Automation of Electronic Systems, 2023.

Formal Methods in System Design, Springer, 2022.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018.

Conference Referee

Int. Conf. on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023
AAAI Conf. on Artificial Intelligence (AAAI), 2022.
Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering (ESEC/FSE), 2022
Annual NASA Formal Methods Symposium (NFM), 2022.
Design Automation Conference (DAC), 2022.
Int. Conf. on Automated Software Engineering (ASE), 2022
AAAI Conf. on Artificial Intelligence (AAAI), 2021.
Design Automation Conference (DAC), 2021.
Int. Conf. on Computer-Aided Design (ICCAD), 2021.
Int. Conf. on Software Engineering and Formal Methods (SEFM), 2020.

References

1. Dirk Beyer, Professor, LMU Munich, Germany, <https://www.sosy-lab.org/people/beyer/>
2. Jie-Hong Roland Jiang, Professor, NTU, Taipei, Taiwan, <http://cc.ee.ntu.edu.tw/~jhjiang/>
3. Victor N. Kravets, Researcher, IBM Thomas J. Watson Research Center, NY, U.S.A.

Additional references are available on request.