Exploring the Interplay of Hardware and Software Analysis

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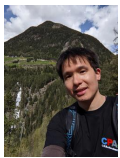

About Me

- 2014: B.Sc. in Electrical Engineering, NTU
- 2021: Ph.D. in Electronics Engineering, NTU
- 2021-2024: PostDoc in Computer Science, LMU Munich, Germany
- From 2025: Assistant Professor, EDA Group, NTU

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- 2021: Ph.D. in Electronics Engineering, NTU
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Research interests: formal methods and verification for computational models (hardware, software, and more)

Formal Verification in a Nutshell

- Does a **computational model** satisfy a **specification**?
  - Model: control-flow automata (software), sequential circuits (hardware), etc.
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  - Specification: temporal-logic formulas
  - Mathematical rigor: prove absence of bugs (cf. testing)
  - Undecidable in theory

Facebook's Software Verifier Infer [1]

```
class Infer {

    String mayReturnNull(int i) {
        if (i > 0) {
            return "Hello, Infer!";
        }
        return null;
    }

    int mayCauseNPE() {
        String s = mayReturnNull(0);
        return s.length();
    }

}
```

Facebook's Software Verifier Infer [1]

```java
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    }

    int mayCauseNPE() {
        String s = mayReturnNull(0);
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    }

}
```

```
Found 1 issue
Infer.java:12: error: NULL_DEREFERENCE
  object s last assigned on line 11 could be null and is dereferenced at line 12
  10.       int mayCauseNPE() {
  11.           String s = mayReturnNull(0);
  12. >         return s.length();
  13.       }
```

*Screenshots from https://fbinfer.com

Overview of Software Verification

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  - Null-pointer dereference
  - Assertion violation
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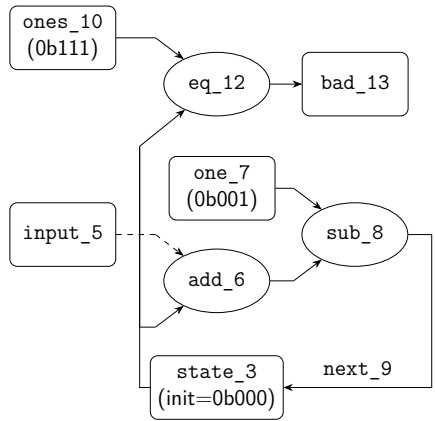
- Annual tool competitions: SV-COMP
  - 59 tools on more than 30 K verification tasks in 2024 [2]
- CPAchecker [3]: found more than 100 bugs (confirmed and fixed) in Linux kernel modules [4]

Example: Sequential Circuit in the BTOR2 Language

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```



Translating BTOR2 Circuits to C Programs

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```

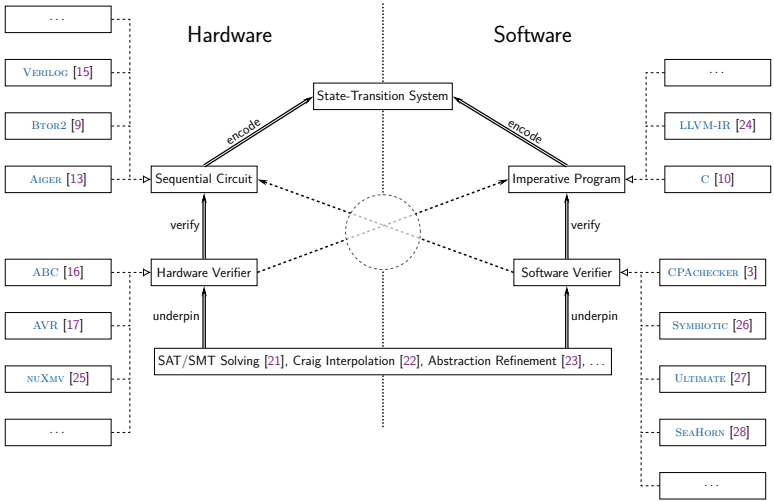
```c
void main() {
  typedef unsigned char SORT_1;
  typedef unsigned char SORT_11;
  const SORT_1 var_2 = 0b000;
  const SORT_1 var_7 = 0b001;
  const SORT_1 var_10 = 0b111;
  SORT_1 state_3 = var_2;
  for (;;) {
    SORT_1 input_5 = nondet_uchar();
    input_5 = input_5 & 0b111;
    SORT_11 var_12 = state_3 == var_10;
    SORT_11 bad_13 = var_12;
    if (bad_13) { ERROR: abort(); }
    SORT_1 var_6 = state_3 + input_5;
    var_6 = var_6 & 0b111;
    SORT_1 var_8 = var_6 - var_7;
    var_8 = var_8 & 0b111;
    state_3 = var_8;
  }
}
```

Circuit-Based Program Verification

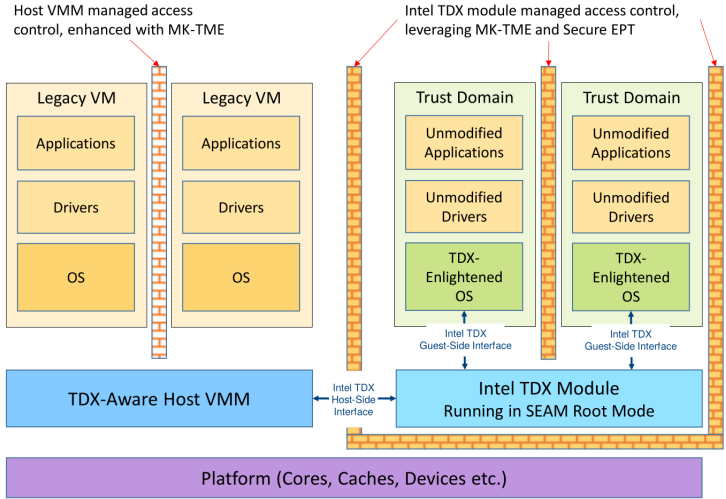
- Sequential circuit as an intermediate representation for program analysis
  - Leveraging hardware verification and logic synthesis

Our circuit-based program verifier, CPV, ranks 6$^{\text{th}}$ out of 26 in the category *ReachSafety* as a first-time participant in SV-COMP 2024!

Exploring the Interplay of Hardware and Software Verification

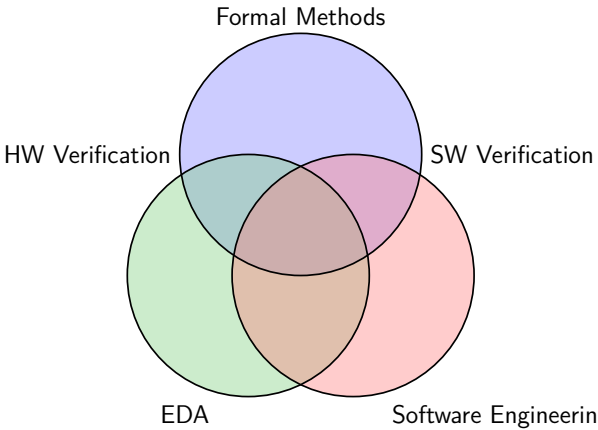


Emerging Paradigms: Confidential Computing in the Cloud



Source: Figure 2.1 in Intel TDX Module v1.5 Base Architecture Specification

We Are Looking for You!



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