



RISC-V Wait-on-Reservation-Set (Zawrs) extension

Ved Shanbhogue

Version 1.0, 6/2022: This document is in development. Assume everything can change. See <http://riscv.org/spec-state> for details.

Table of Contents

Preamble.....	1
Copyright and license information	2
Contributors.....	2
1. Introduction	3
2. Zawrs.....	4

Preamble



This document is in the [Development state](#)

Assume everything can change. This draft specification will change before being accepted as standard, so implementations made to this draft specification will likely not conform to the future standard.

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Contributors

This RISC-V specification has been contributed to directly or indirectly by:

Aaron Durbin, Abel Bernabeu, David Weaver, Greg Favor, Ken Dockser, Paul Donahue, Philipp Tomsich, Tariq Kurd, Ved Shanbhogue

Chapter 1. Introduction

The Zawrs extension defines a pair of instructions to be used in polling loops that allows a core to enter a low-power state and wait on a store to a memory location. Waiting for a memory location to be updated is a common pattern in many use cases such as:

1. Contenders for a lock waiting for the lock variable to be updated.
2. Consumers waiting on the tail of an empty queue for the producer to queue work/data. The producer may be code executing on a RISC-V hart, an accelerator device, an external I/O agent.
3. Code waiting on a flag to be set in memory indicative of an event occurring. For example, software on a RISC-V hart may wait on a "done" flag to be set in memory by an accelerator device indicating completion of a job previously submitted to the device.

Such use cases involve polling on memory locations, and such busy loops can be a wasteful expenditure of energy. To mitigate the wasteful looping in such usages, a **WRS.NTO** (WRS-with-no-timeout) instruction is provided. Instead of polling for a store to a specific memory location, software registers a reservation set that includes all the bytes of the memory location using the **LR** instruction. Then a subsequent **WRS.NTO** instruction would cause the hart to temporarily stall execution in a low-power state until a store occurs to the reservation set.

Sometimes the program waiting on a memory update may also need to carry out a task at a future time or otherwise place an upper bound on the wait. To support such use cases a second instruction **WRS.STO** (WRS-with-short-timeout) is provided that works like **WRS.NTO** but bounds the stall duration to an implementation-define short timeout such that the stall is terminated on the timeout if no other conditions have occurred to terminate the stall. The program using this instruction may then determine if its deadline has been reached.

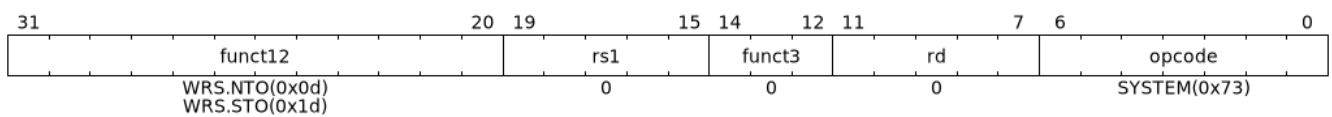
Chapter 2. Zawrs

The **WRS.NTO** and **WRS.STO** instructions cause the hart to temporarily stall execution in a low-power state until one of the following events occur:

1. The reservation set is invalid
2. If **WRS.STO**, an implementation defined short time has passed since the hart stalled execution.
3. An interrupt was observed - even if disabled

These instructions are available in all privilege modes.

Encoding:



Operation:

```

if reservation set is valid
  Stall hart execution until one of the following events occur:
    a) The reservation set is invalid
    b) If WRS.STO, a short time since start of stall has elapsed
    c) An interrupt is observed
  
```

While stalled, an implementation is permitted to occasionally terminate the stall and complete execution for any reason.

These instructions are not supported in a constrained **LR/SC** loop.

*Architecture Comment: **WRS.STO** and **WRS.NTO** are not defined as hints but as having defined behaviors. Implementing as a hint that can be ignored (i.e., executed as a nop) may lead to degradation in the system and/or application performance.*

*Architecture Comment: Since the **WRS.STO** and **WRS.NTO** instructions can complete execution for reasons other than stores to the reservation set, software will likely need a means of looping until the required stores have occurred.*



*Recommendation: The duration of a **WRS.STO** instruction's timeout may vary significantly within and among implementations. In a typical implementation this duration should be long enough to allow meaningful power reduction but short enough to avoid a program using the timeout to meet a deadline from missing it significantly. A duration less than or equal to 10 microseconds is recommended.*

Recommendation: An implementation should try to bound the latency to terminate the stall, from when the conditions to terminate the stall have been observed, to the latency incurred on access to an on-chip cache furthest from the hart or in case of a cache-less system the access to main memory from the hart.

WRS.NTO and **WRS.STO** instructions follow the rules of the **WFI** instruction for resuming execution on a

pending interrupt.

When the **TW** (Timeout Wait) bit in **mstatus** is set and **WRS.NTO** is executed in S or U mode, and it does not complete within an implementation-specific bounded time limit, the **WRS.NTO** instruction will cause an illegal instruction exception.

When executing in VS or VU mode, if the **VTW** bit is set in **hstatus**, the **mstatus TW** bit is clear, and the **WRS.NTO** does not complete within an implementation-specific bounded time limit, the **WRS.NTO** instruction will cause a virtual instruction exception.