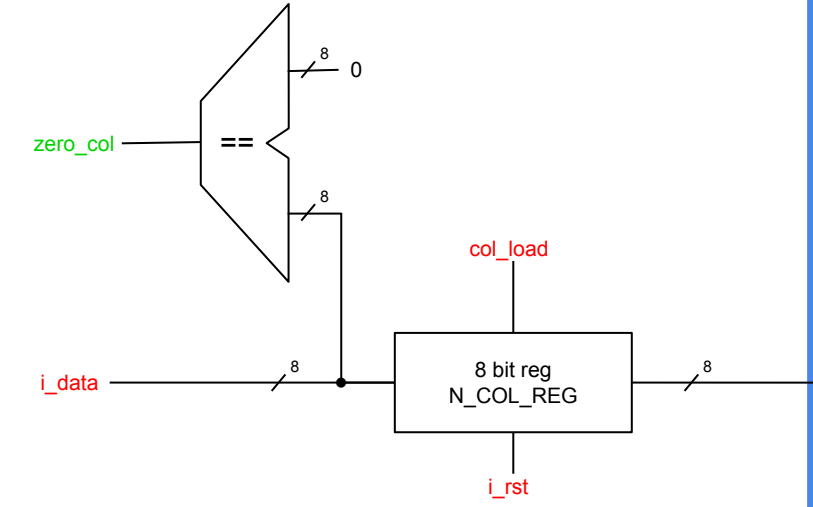


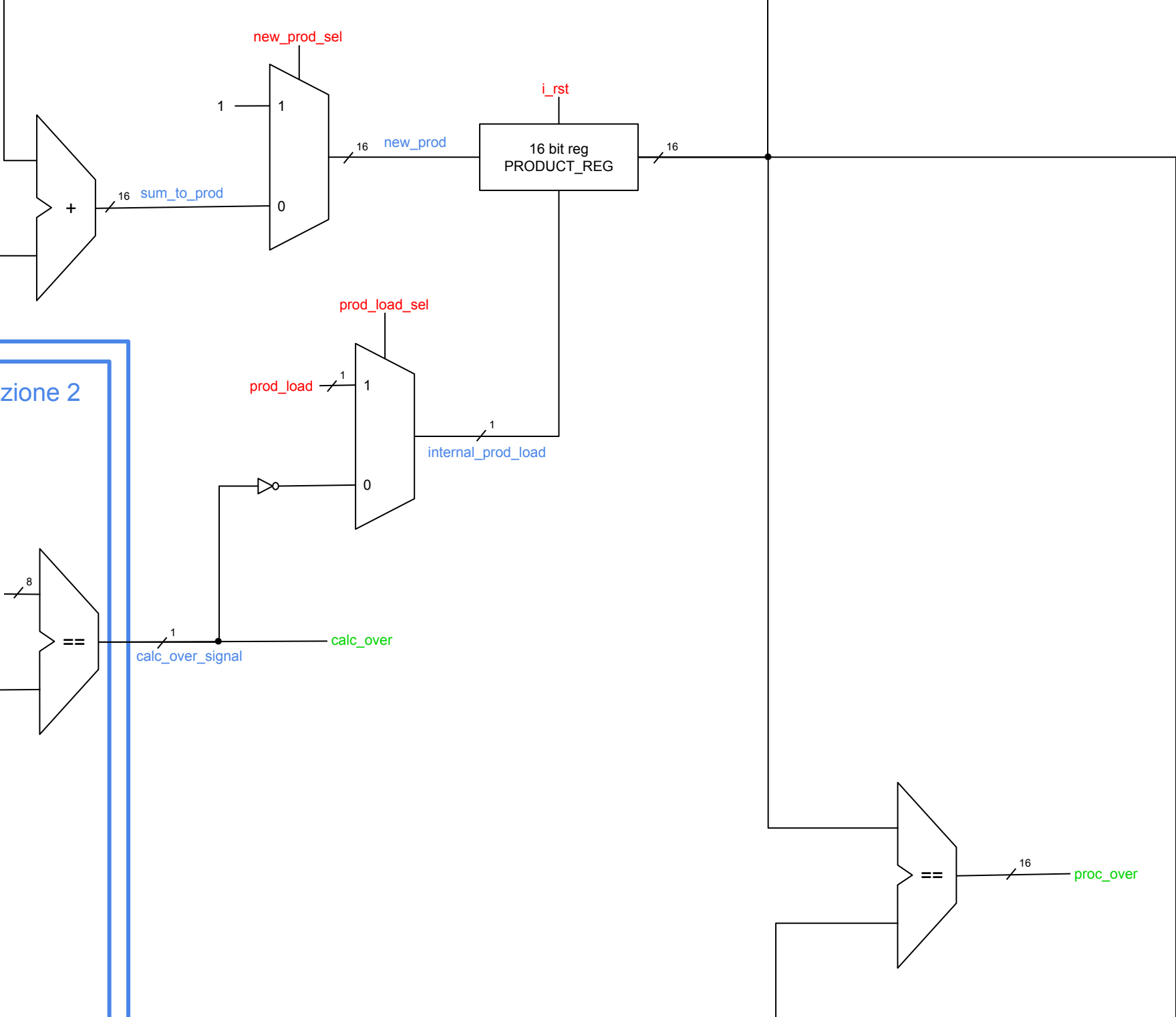
# Sezione 1

The diagram illustrates the first section of a 16-bit register. It features a multiplexer with two 8-bit inputs: `zero_col` (green) and `I_data` (red). The multiplexer's output is an 8-bit bus that connects to the `col_load` input of a `8 bit reg N_COL_REG` block. The register also has a `col_load` input (red) and an `I_rst` input (red). The register's output is an 8-bit bus.



Sezione 2

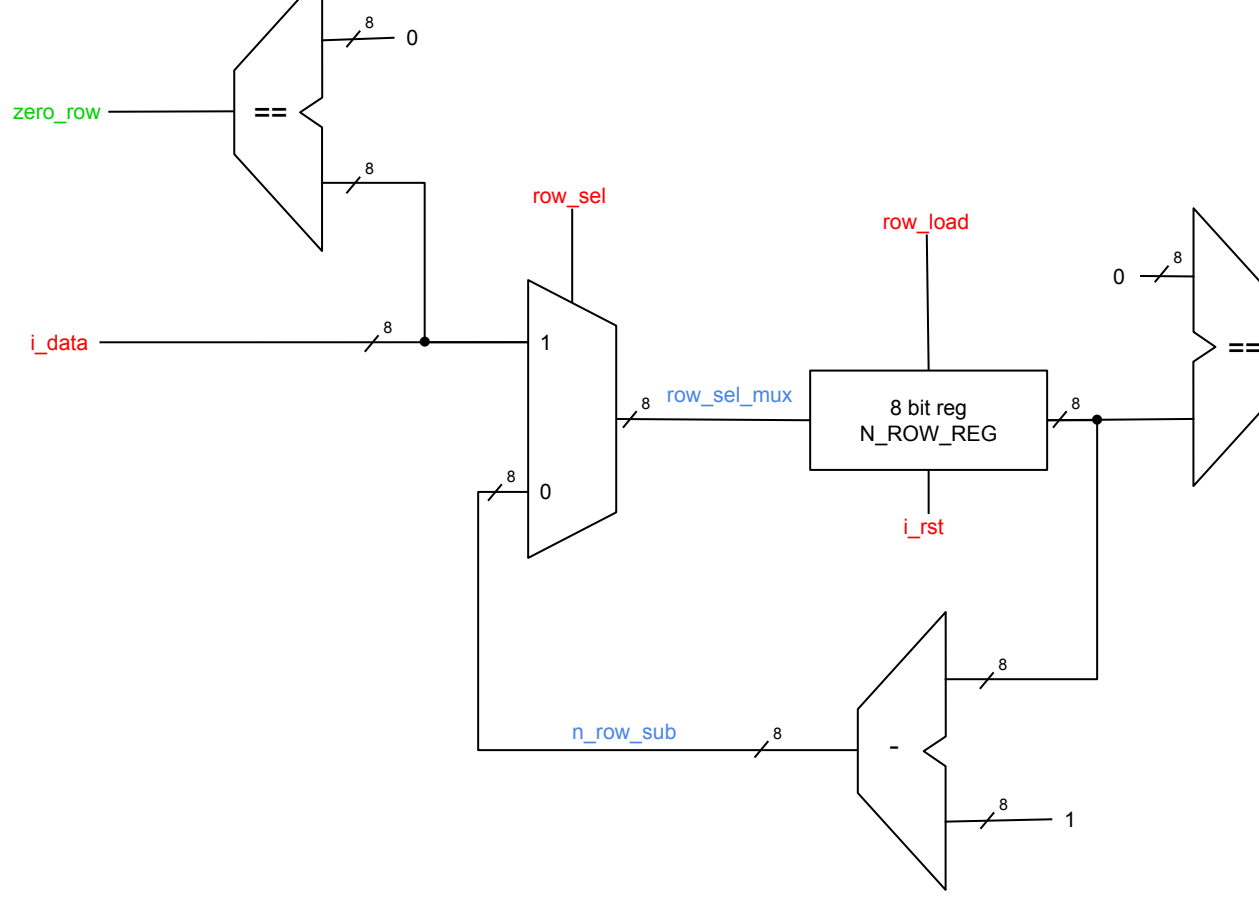
The diagram illustrates a 16-bit multiplier circuit. It includes an 8-bit register `N_ROW_REG` with inputs `row_load` and `i_rst`. The register's output is fed into an 8-bit subtractor, which also takes a constant `1` as input. The subtractor's output is compared to zero using an 8-bit equality comparator. The comparator's output, `calc_over_signal`, is inverted and then ANDed with `prod_load_sel` to generate `internal_prod_load`. This signal, along with `new_prod_sel`, controls a 16-bit multiplexer. The multiplexer selects between the current product and a new product. The new product is calculated by adding the multiplicand (from `N_ROW_REG`) to the current product in a 16-bit adder. The selected product is stored in a 16-bit register `PRODUCT_REG`, which has an `i_rst` input. The final 16-bit output, `proc_over`, is the value in `PRODUCT_REG`.



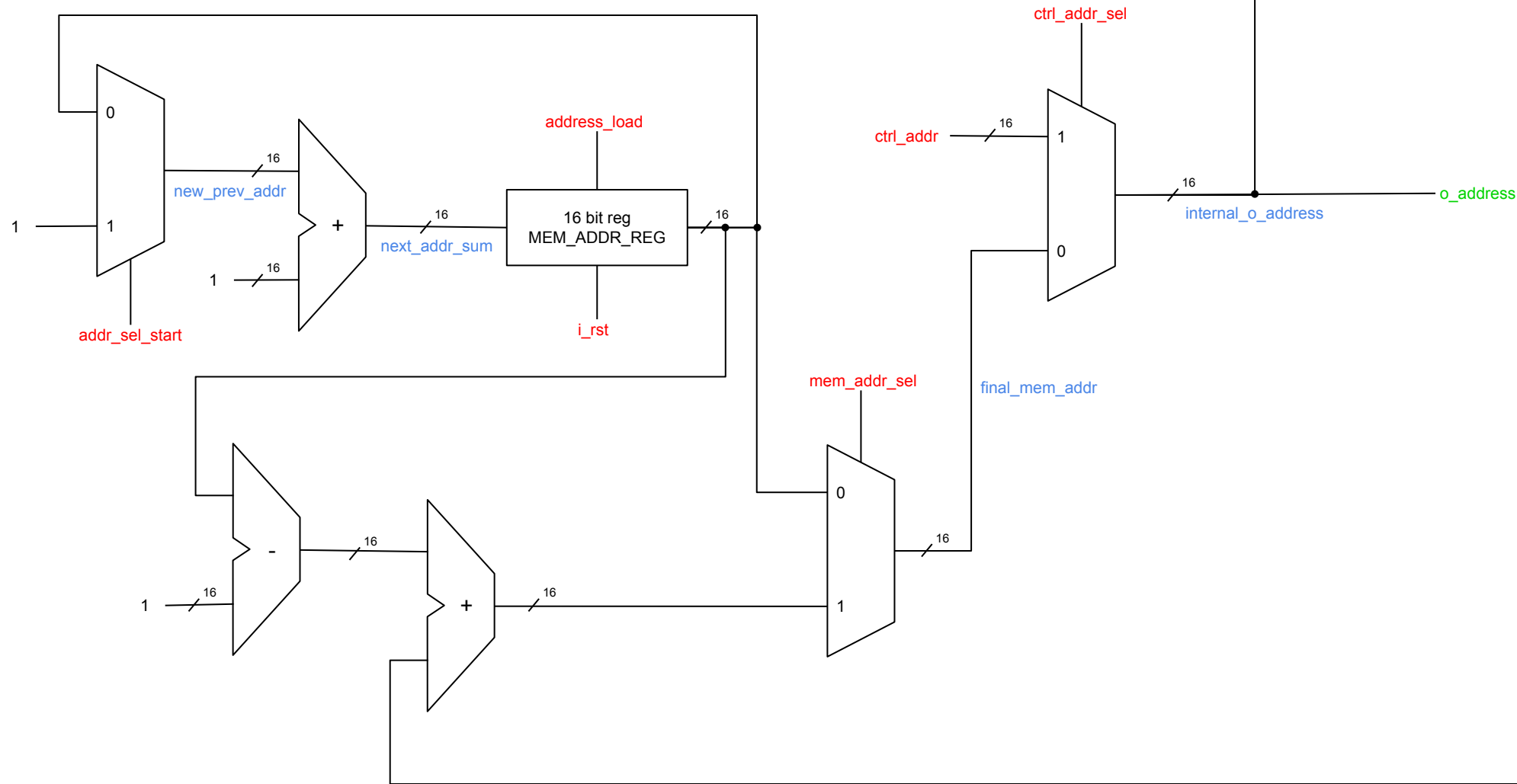
## Sezione 2

The diagram illustrates the logic for a 2D array access. It features several 8-bit components:

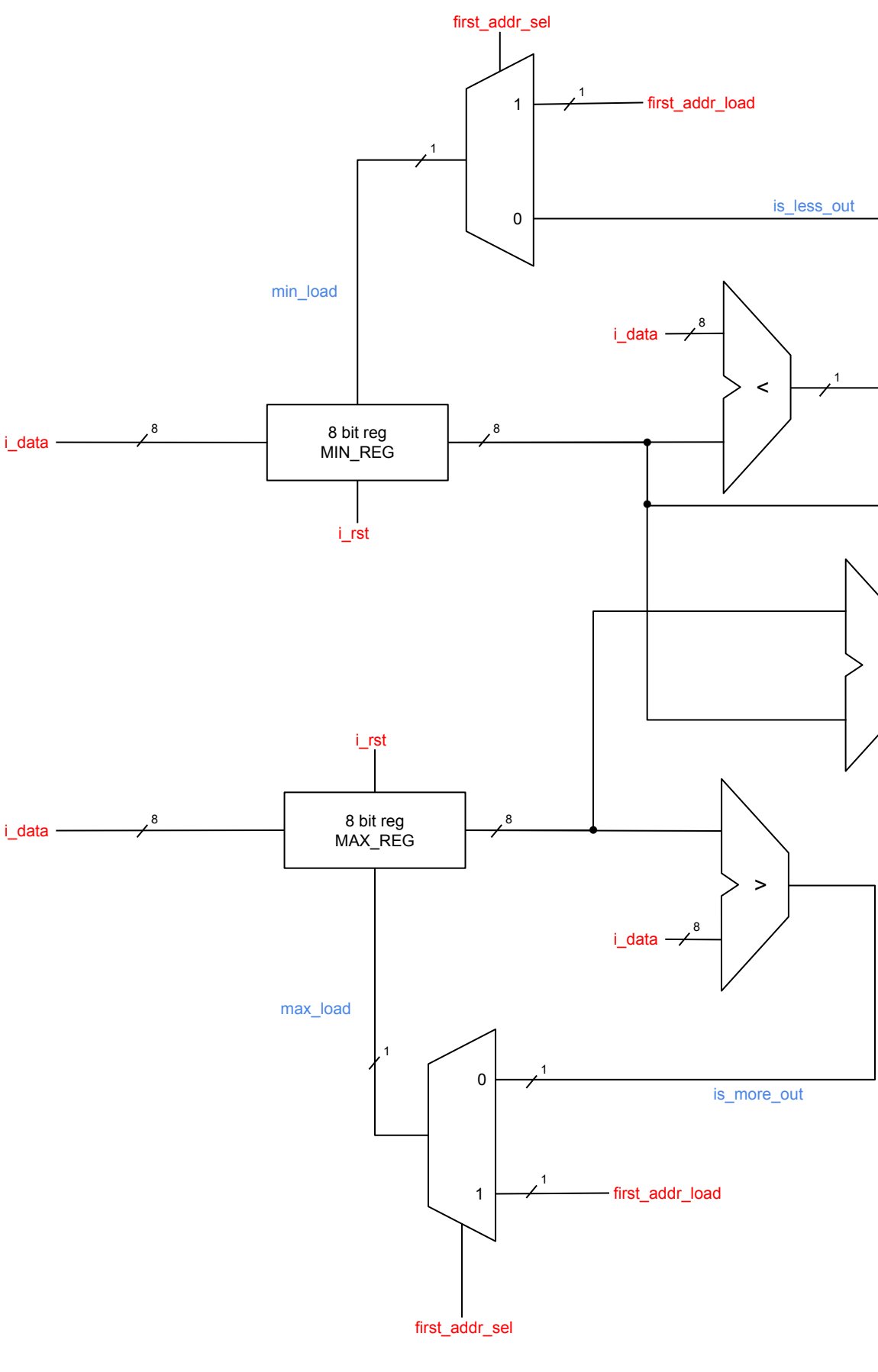
- zero\_row** (green) and **i\_data** (red) are 8-bit inputs.
- A first 8-bit comparator (**==**) compares **zero\_row** with a constant **0** (8-bit). Its output is connected to the **row\_sel** input of a 2-to-1 multiplexer.
- The multiplexer has two data inputs: **i\_data** (connected to input **1**) and the output of a second 8-bit comparator (input **0**). The second comparator compares **i\_data** with a constant **1** (8-bit).
- The multiplexer's output is an 8-bit signal labeled **row\_sel\_mux**, which is connected to the **row\_sel** input of a **8 bit reg N\_ROW\_REG**.
- The register also has a **row\_load** (red) control input and an **i\_rst** (red) reset input.
- The register's output is an 8-bit signal that branches to two comparators:
  - A first comparator (input **0**) compares the register output with a constant **0** (8-bit).
  - A second comparator (input **-**) compares the register output with the output of an 8-bit subtractor.
- The subtractor takes the register output and an 8-bit input **n\_row\_sub** (blue) and outputs the result to the second comparator.
- The output of the second comparator is connected to the **i\_rst** input of the register.



Sezione 4



## Sezione 5



Sezione 6

