Verilog Debug Methodology

This lab demonstrates a methodology for debugging a Verilog design. This will prove useful in later labs.

Procedure

1. Download the lab02.zip archive.
2. Use the template file from Lab 01 and add the Verilog design file *max3sint16b.v* and testbench *tb_max3sint16b.v* to the project. You do not have to add a constraints file. Also copy the test vector file (*max3sint16b_vectors.txt*) into the same directory as your project.
3. The first segment of class on September 8, 2020, discusses the design. The Verilog file has errors and we discuss how to find the errors and correct them. Repeat the steps in the lecture video with your project. As you progress in the video, answer the questions in the *report.docx* file. The *report.docx* file also has you capture some screenshots.
4. To capture screenshots, only capture the relevant portion of the screen. Do not just capture the entire screen. There are several utilities that can do that, including the built-in 'Screen Snip' tool in the Windows 10 menu.

Submission instructions

1. Create a directory named *lab2_myBamaID* (e.g. lab2_taylo019).
2. Copy the corrected *max3sint16b.v* file to this directory.
3. Copy your completed *report.docx* to this directory.
4. From Windows, select the *lab2_myBamaID* folder and, from the right-click menu, use the *Send To Compressed (zip) Folder* command to produce a ZIP archive named *lab2_myBamaID.zip*.
5. Upload your *lab2_myBamaID.zip* file to Blackboard using the Lab 02 assignment link.

Do not submit any other kind of archive than a .zip archive.