Digital Systems Design
ECE 480/580

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Soft-core processors

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System-on-a-chip (SoC)

- A chip that integrates all components of a computer or other embedded system
  - Key feature: everything on one chip
- Typically include:
  - CPU
  - Memory
  - General-purpose and/or dedicated I/O
  - Long-term storage
  - Application-specific hardware
- Examples:
  - Raspberry Pi series main chip is CPU/GPU SoC
  - Main hardware in most cell phones

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System-on-a-programmable-chip (SoPC)

- Implementing an SoC on programmable logic
- Typically includes:
  - An intellectual property (IP) processor core
  - A customized selection of necessary hardware
- IP processor core is classified as either hard or soft
  - Refers to the flexibility or configurability of the core

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Hard-core IP processor

- Less configurable, but higher performance
- Typically manufactured as a dedicated circuit connected to the interconnect matrix of the FPGA
- Examples:
  - Most FPGA manufacturers supply an ARM core on board some of their FPGA development boards
  - DE1-SoC has an ARM Cortex-A9 dual-core processor built into the FPGA fabric

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Soft-core IP processor

- Soft-core processors refer to using existing FPGA logic elements, memory, etc. to implement the processor logic
- Can be feature-rich, allowing specifications of parameters:
  - Memory/datapath width
  - ALU functionality
  - Number and types of peripherals
  - Memory and I/O address space
- These parameters are specified at compile time
- Major disadvantage
  - Soft cores typically have slower clock rates and higher power consumption than their hard-core counterparts

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SoPC development tools

- A CAD tool, specific to each soft processor core, is used to specify these processor options
  - Additional options:
    - Register file size
    - Hardware multiply and divide support
    - Floating-point support
    - Interrupts
    - I/O hardware
    - Custom hardware
- Tool outputs a synthesizable HDL model of the processor
- User adds additional user logic and synthesizes using the CAD suite
- Application programs can be compiled by a custom compiler provided for the processor core

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SoPC design flow

- SoPC processor core synthesis and associated tools are generally provided by traditional CAD tools.
- Various commercial and open-source processor cores
  - NIOS II
  - Microblaze
  - www.opencores.org
  - www.leox.org
- Commercial soft processor cores tend to be more efficiently implemented on FPGAs
  - Typically optimized by the manufacturer for a particular FPGA family
- Hardware and software can be designed concurrently
  - Hardware/Software co-design

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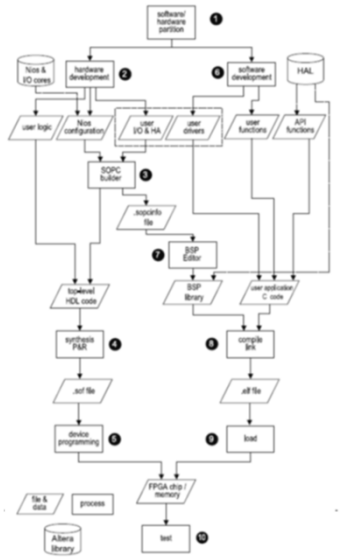
SoPC design flow

1: software/hardware partition
2: hardware development
3: synthesis of soft-core
4: synthesis place-and-route
5: device programming
6: software development
7: BSP generation
8: compile and link
9: load
10: test



Note: this flow chart is for the Intel toolsuite and the NIOS II processor

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Initializing memory

- Once the program/data file has been generated, it must be loaded onto the processor's program and data memories
- Multiple methods
  - On-chip memory
    - For small applications, it might fit in the BRAM of the FPGA
    - Initialization through standard FPGA tools
  - Bootloader
    - A small software program, usually loaded onto on-chip memory or an EEPROM, that is responsible for communicating with another device and downloading an application program into external memory (SRAM, SDRAM, flash, etc.)
    - After download, control transferred to application program
  - External non-volatile storage

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Hardware bootloader

- A hardware bootloader is like a software bootloader
  - Difference: implemented in dedicated logic within the processor core
- On power-up, the hardware bootloader stalls the processor and downloads the application code (typically through a serial interface)
  - Bootloader can start/stop the processor
  - Has access to at least some of the register set
  - Typically has direct access to memory or memory registers
- NIOS II and Microblaze support a hardware bootloader with a JTAG interface
  - What does this mean?
  - You can download new application software without recompiling the soft-core processor hardware

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SoPC design vs. Traditional design

- Traditional design flows:
  - ASIC – application-specific integrated circuit
  - Fixed-processor design
- SoPC design advantages:
  - Reconfigurable nature
  - Short development cycle
- SoPC design disadvantages:
  - Higher unit costs in production
  - Relatively high power consumption

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More on flexible hardware benefits

- Features and specifications are frequently modified throughout the design cycle
  - Marketing detects a shift in demand for additional features
    - Cell phones with/without cameras, MP3 players, etc.
  - A protocol or specification is introduced or updated
    - Introduction of USB 2.0/3.0 standards
- In traditional design modalities (ASICs and fixed processors), these changes could result in changes to:
  - ASIC design
  - Processor selection
  - PCB design
- These changes will increase product time-to-market and unit cost
- Can also affect multiple generations/versions of a single product or multiple product lines
  - Use of a single PCB for multiple product lines
  - Use of a single PCB for multiple versions of a single product

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Comparing design modalities

Feature	SoPC	ASIC	Fixed processor
Software flexibility	Good	Good	Good
Hardware flexibility	Good	Poor	Poor
Development cost/time	Good	Poor	Good
Peripheral equipment costs	Good	Good	Poor
Performance	Average	Good	Good
Production cost	Average	Good	Good
Power efficiency	Poor	Good	Good

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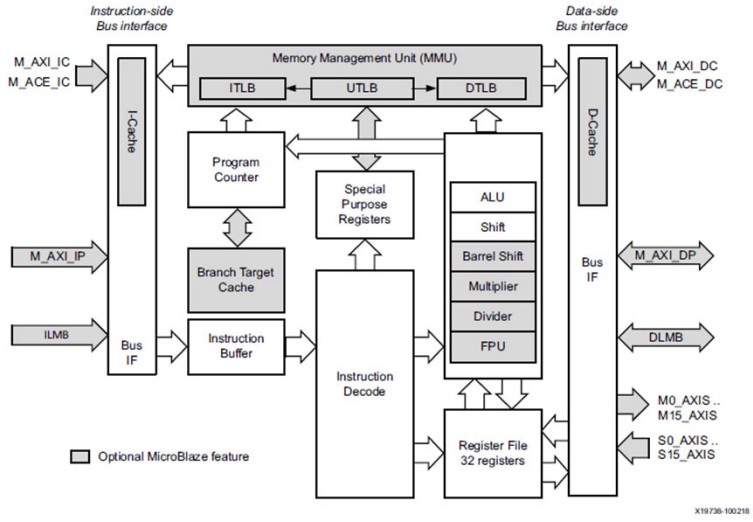
Xilinx Microblaze architecture



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