Midterm 01 Report

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1. Block diagram of the circuit

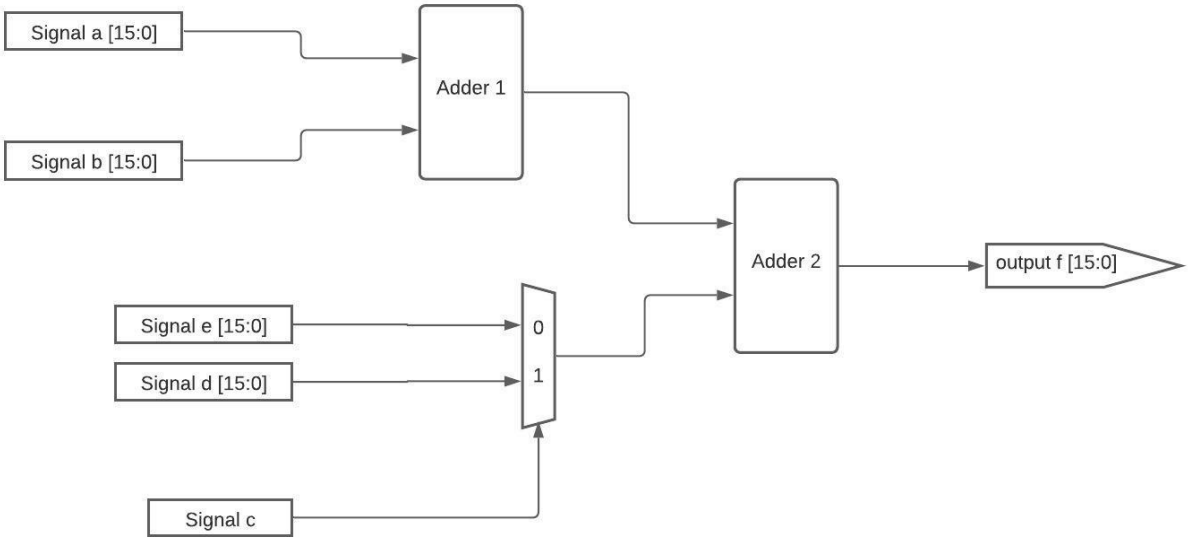

Figure 1. Block Diagram for the circuit

2. Behavioral Simulation Screenshot

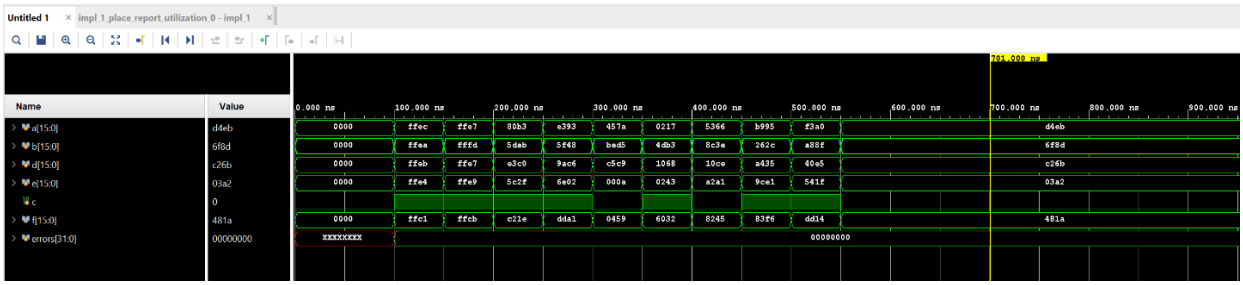

Figure 2. Behavioral Sim screenshot

3. Timing Simulation Screenshot

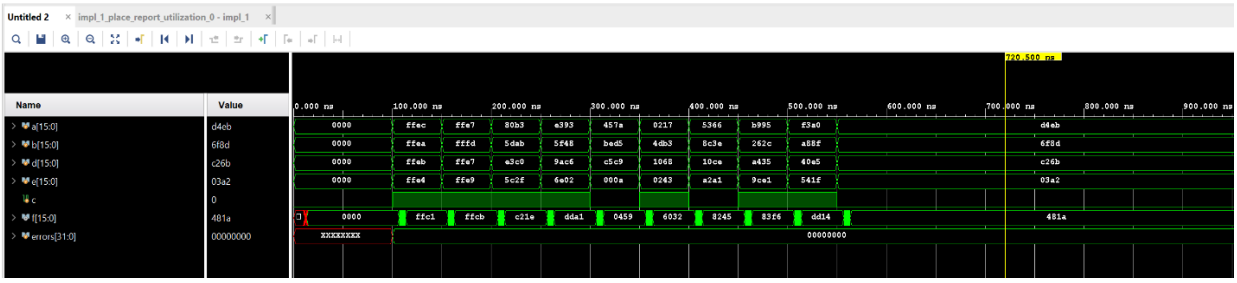

Figure 3. Timing Sim screenshot

4. LUT implementation Table

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1. Slice Logic
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+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs              |   32 |     0 |     20800 |  0.15 |
|   LUT as Logic          |   32 |     0 |     20800 |  0.15 |
|   LUT as Memory         |    0 |     0 |      9600 |  0.00 |
| Slice Registers         |    0 |     0 |     41600 |  0.00 |
|   Register as Flip Flop |    0 |     0 |     41600 |  0.00 |
|   Register as Latch     |    0 |     0 |     41600 |  0.00 |
| F7 Muxes                |    0 |     0 |     16300 |  0.00 |
| F8 Muxes                |    0 |     0 |      8150 |  0.00 |
+-------------------------+------+-------+-----------+-------+
```

Figure 4. LUT implementation table