Digital Systems Design
ECE 480/580

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VGA signal generation

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Driving a VGA Output

A female DE15 socket.

*	Pin 1	RED	Red video
*	Pin 2	GREEN	Green video
*	Pin 3	BLUE	Blue video
	Pin 4	ID2/RES	formerly Monitor ID bit 2, reserved since E-DDC
	Pin 5	GND	Ground (HSync)
	Pin 6	RED_RTN	Red return
	Pin 7	GREEN_RTN	Green return
	Pin 8	BLUE_RTN	Blue return
	Pin 9	KEY/PWR	formerly key, now +5V DC, powers EDID EEPROM chip on some monitors
	Pin 10	GND	Ground (VSync, DDC)
	Pin 11	ID0/RES	formerly Monitor ID bit 0, reserved since E-DDC
	Pin 12	ID1/SDA	formerly Monitor ID bit 1, I²C data since DDC2
*	Pin 13	HSync	Horizontal sync
*	Pin 14	VSync	Vertical sync
	Pin 15	ID3/SCL	formerly Monitor ID bit 3, I²C clock since DDC2

* Signal to drive

Wikipedia – VGA connector

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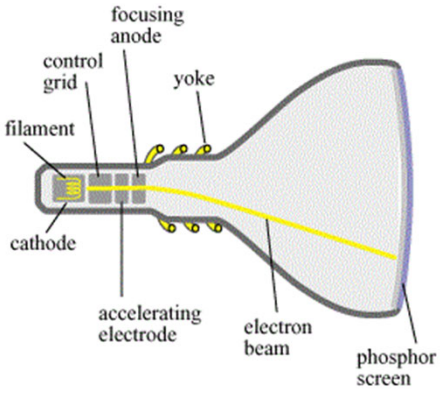
Video Display Technology

- Algorithm initially built for cathode ray tube



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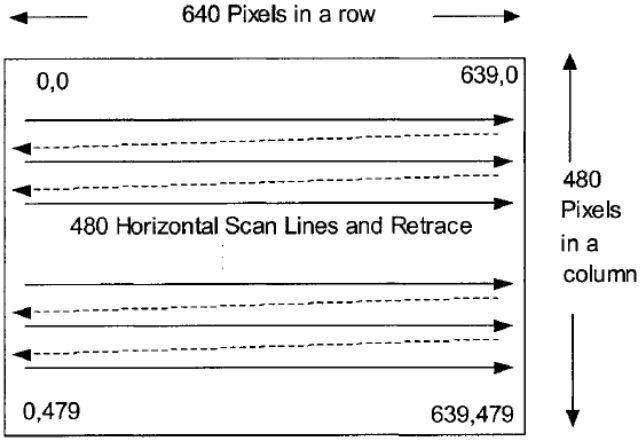
Video Display Technology



- Same timing algorithm in use with LCD, etc.

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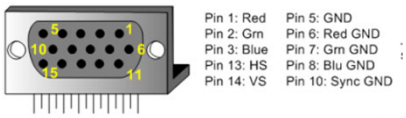
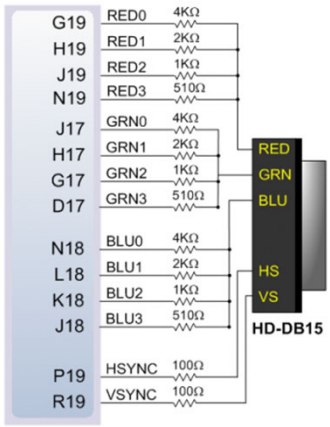
Basys3 VGA peripheral configuration

RGB values are 4-bits each

HSYNC and VSYNC are timing signals





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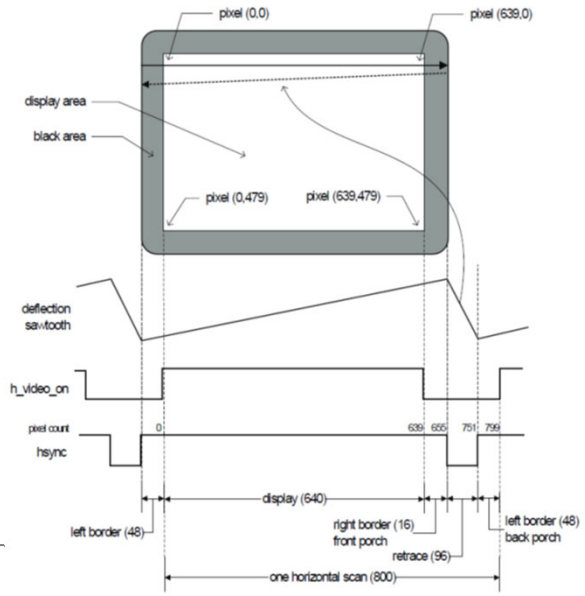
Video Refresh



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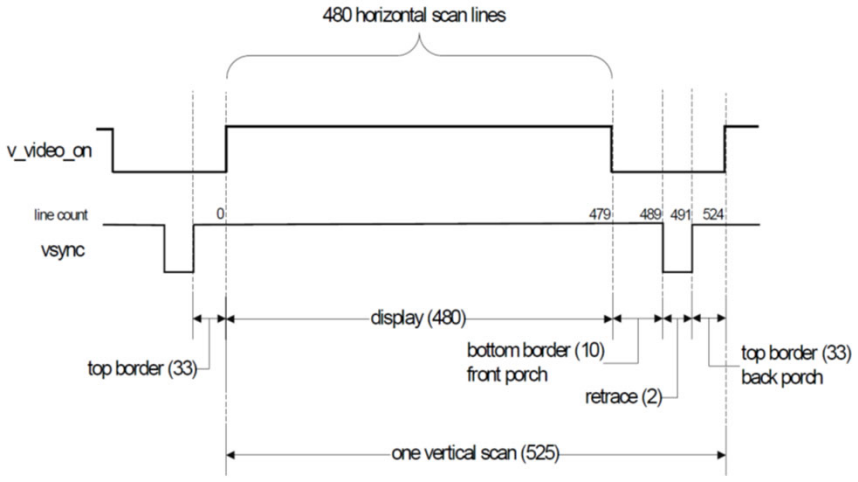
Video Refresh



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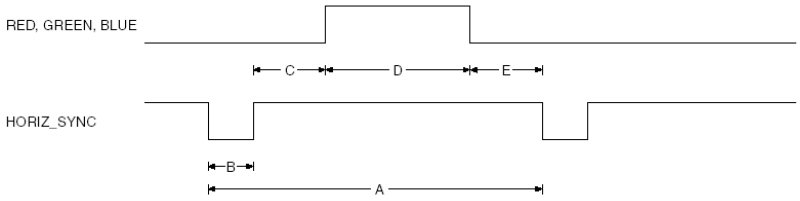
Video Refresh



Parameters	A	B	C	D	E
Time	31.77 µs	3.77 µs	1.89 µs	25.17 µs	0.94 µs

- A – total horizontal refresh time
- B – horizontal synchronization time
- C, E – guardband time
- D – pixel refresh time

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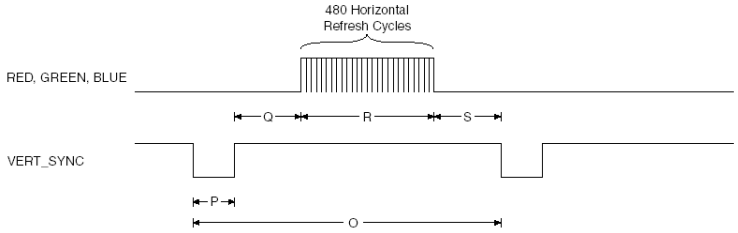
Video Refresh



Parameters	O	P	Q	R	S
Time	16.6 ms	64 µs	1.02 ms	15.25 ms	0.35 ms

- O – total vertical refresh time
- P – vertical synchronization time
- Q, S – guardband time
- R – horizontal refresh cycles

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Video Display Technology

- In a digital system, with which signal should we begin?
  - The clock!
- How fast should it be?
  - How many “pixels” need to be updated per second?
  - Per row: 640 + 160 (front/back porch, etc.)
  - Per screen: 480 rows + 45
  - Per second: 60 transitions
  - $(640 + 160) \times (480 + 45) \times 60 = 25{,}200{,}000$
  - 25.2 MHz
  - VGA industry standard is 25.175 MHz
  - Typical tolerance of 5% (23.94 MHz to 26.46 MHz)

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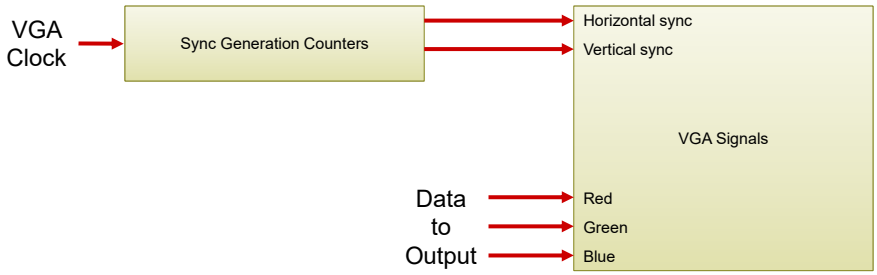
Driving a VGA Output



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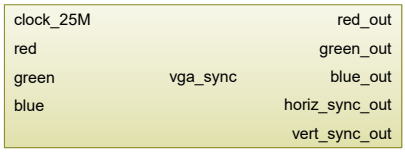
Sync Generation Counter … Generation



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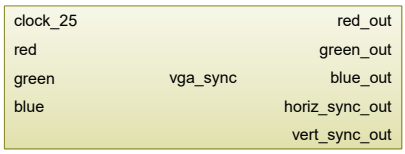
simple_vga Project

Simple task: have the screen toggle between red and black with SW[0].



Find simple_vga_verilog on Blackboard.

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Video Data Options

- Simple video games have a background color with a few simple moving images
  - No need to store the default background color in video memory
  - Hardware comparators track the row and column counts as the video signal is generated and detect when another image, other than the background, is to be displayed
    - When the comparator signals that the row and column count matches the image location, the image color data is switched into the RGB output using a multiplexor
  - The image can be made to move if its current row and column location is stored in registers and used as a comparator input
  - Additional logic can change the image's location producing movement
  - Multiple comparators can be used to support several fixed and moving images (often referred to as sprites)

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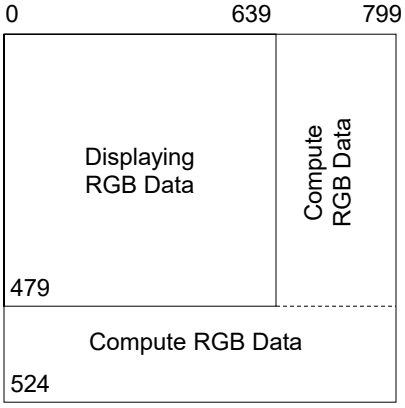
Updating Video Data



- When RGB data is being displayed, pixel memory should be in 'read' mode
  - To avoid flicker and memory access conflicts, designs should update pixel RAM (or other hardware that produces the RGB output) during the time that RGB data is not being displayed
- Use the horizontal and vertical guardband times (front and back porches!) to update pixel data

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Character-Based Video Design (Font Data)

- For a video display that contains textual data
- A pixel pattern (font) is needed for each character to be displayed
- Font data can be stored in a ROM
  - Initialization works the same with ROM
  - tcgrom.mif

```
Depth = 512;
Width = 8;
Address_radix = oct;
Data_radix = bin;
% Character Generator ROM Data %
Content
  Begin
000  : 00111100 ; %    ****     %
001  : 01100110 ; %   **  **    %
002  : 01101110 ; %   ** ***    %
003  : 01101110 ; %   ** ***    %
004  : 01100000 ; %   **        %
005  : 01100010 ; %   **   *    %
006  : 00111100 ; %    ****     %
007  : 00000000 ; %             %

010  : 00011000 ; %     **      %
011  : 00111100 ; %    ****     %
012  : 01100110 ; %   **  **    %
013  : 01111110 ; %   ******    %
014  : 01100110 ; %   **  **    %
015  : 01100110 ; %   **  **    %
016  : 01100110 ; %   **  **    %
017  : 00000000 ; %             %
```

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