Name_____ **Student ID**_____ **Colleges & Schools**_____ **Department**_____

Pretest

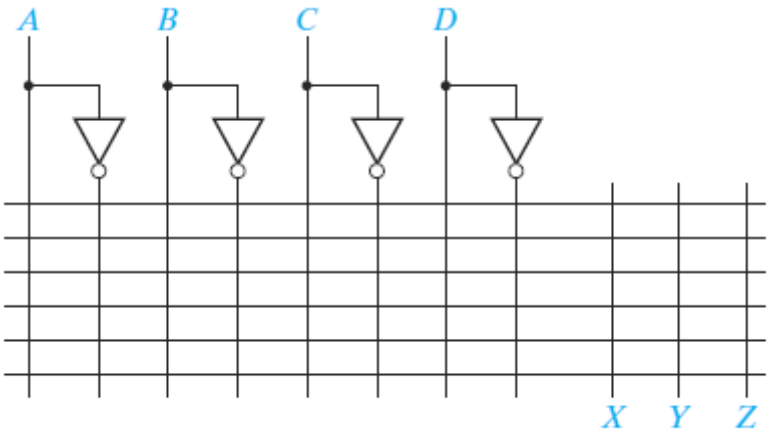
1. The following PLA will be used to implement the following equations:

   X = AB′D + A′C′ + BC + C′D′

   Y = A′C′ + AC + C′D′

   Z = CD + A′C′ + AB′D

   (a) Indicate the connections that will be made to program the PLA to implement these equations.



   (b) Specify the truth table for a ROM which realizes these same equations.

2. A U-V flip-flop behaves as follows:

   If *UV* = 00, the flip-flop does not change state.

   If *UV* = 10, the flip-flop is set to Q = 0.

   If *UV* = 11, the flip-flop changes states.

   The input combination UV = 01 is not allowed.

   (a) Give the characteristic (next state) equation for this flip-flop.

   (b) Complete the following table, using don't-cares where possible.

Q	Q^+	U	V
0	0		
0	1		
1	0		
1	1		

   (c) Realize the following next-state equation for Q using a U-V flip-flop: $Q^+ = A + BQ$. Find equations for U and V.

3. Design a 3-bit counter which counts in the sequence:

   001, 100, 101, 111, 110, 010, 011, (repeat) 001, ...

   (a) Use D flip-flops.

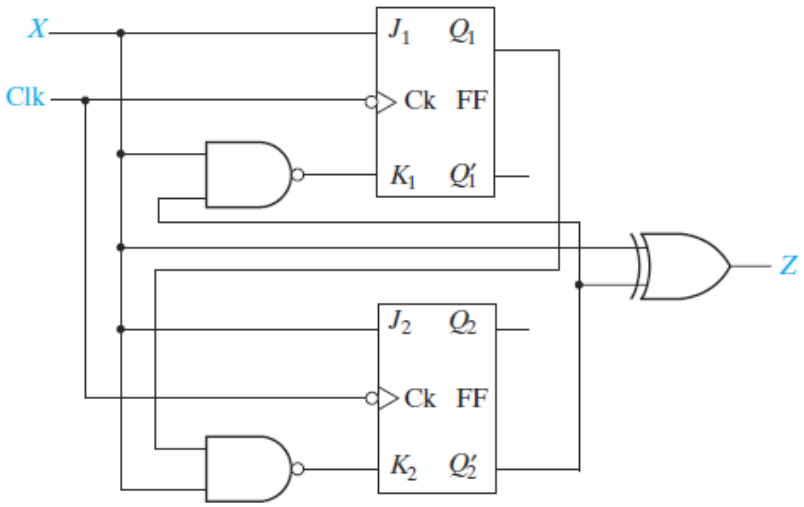
   (b) Use J-K flip-flops.

   (c) Use T flip-flops.

   (d) Use S-R flip-flops.

   (e) What will happen if the counter of (a) is started in state 000?

4. (a) Construct a transition table and state graph for the circuit shown below.



(b) Construct a timing chart for the circuit for an input sequence X = 10111. (Assume that initially Q1 = Q2 = 0 and that X changes midway between the rising and falling clock edges.)

(c) List the output values produced by the input sequence.