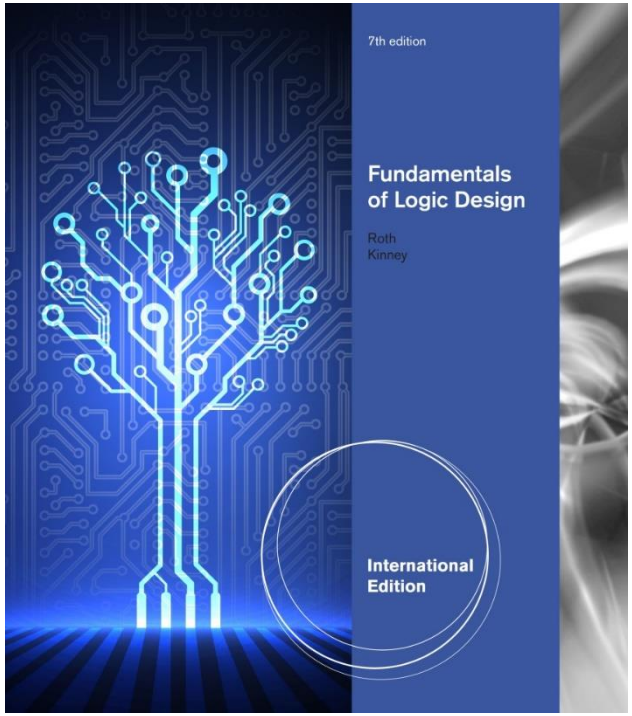

Course Introduction

Introduction

Prof. Hyun Seok Oh

- Semiconductor 400316
- Tel: 031-299-4922
- E-mail: bluesky96@skku.edu
- Office hours
  - ✓ 14:00-16:00 Thursday
  - ✓ 14:00-16:00 Tuesday
- Class hours
  - ✓ 09:00-10:15 Tuesday
  - ✓ 10:30-11:45 Thursday

NYU TANDON SCHOOL OF ENGINEERING

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Overall Schedule

Week	Contents	Tue	Thu	Quiz/Homework/Pre-Test
1st Week	Unit 1. Number Systems and Conversion	09/04	09/06	5 min. Quiz and Homework
2nd Week	Unit 2. Boolean Algebra Unit 3. Boolean Algebra (Continued)	09/11	09/13	5 min. Quiz and Homework
3rd Week	Unit 4. Minterm and Maxterm Expansions	09/18	09/20	5 min. Quiz and Homework
4th Week	Unit 5. Karnaugh Maps	09/25	09/27	Quiz (hand out) and Homework
5th Week	Unit 5. Karnaugh Maps Unit 6. Quine-McCluskey Method	10/02	10/04	5 min. Quiz and Homework
6th Week	Unit 7. Multi-Level Gate Circuits	10/09	10/11	Quiz and Pre-Test (hand out)
7th Week	Unit 8. Combinational Circuit Design and Simulation Using Gates	10/16	10/18	Solve the Pre-Test in class
8th Week	Midterm Exam	10/23	10/25	Midterm Examination
9th Week	Unit 9. Multiplexers, Decoders, and Programmable Logic Devices	10/30	11/01	5 min. Quiz and Homework
10th Week	Unit 11. Latches and Flip-Flops	11/06	11/08	Quiz (hand out) and Homework
11th Week	Unit 12. Registers and Counters	11/13	11/15	5 min. Quiz and Homework
12th Week	Unit 13. Analysis of Clocked Sequential Circuits	11/20	11/22	Logic Circuit Design
13th Week	Unit 14. Derivation of State Graphs and Tables	11/27	11/29	5 min. Quiz and Homework
14th Week	Unit 15. Reduction of State Tables	12/04	12/06	Quiz and Pre-Test (hand out)
15th Week	Unit 16. Sequential Circuit Design	12/11	12/13	Solve the Pre-Test in class
16th Week	Final Exam	12/18	12/20	Final Examination

Evaluation

Key Evaluation Process

- Attendance: 10%
- Homework: 10%
- Midterm Examination: 30%
  - ✓ One sheet of paper (A4 size) is allowed for the exam, but no cheating allowed
- Final Examination: 35%
  - ✓ One sheet of paper (A4 size) is allowed for the exam, but no cheating allowed
- Quiz and Term Project: 15%
  - ✓ Pick up the best five scores out of 14 Quizzes.
  - ✓ Simple logic circuit design project utilizing flip-flop and combinational/sequential circuit design

	Attendance	Homework	Midterm	Final	Quiz and Project	Total
Percentage	**10%**	**10%**	**30%**	**35%**	**15%**	**100%**
Comments	Attend at least 3 quarters	Based on Text Book	Based on Quiz and Homework One sheet of paper is allowed	Based on Quiz and Homework One sheet of paper is allowed	Quiz: 5% Term Project: 10%	