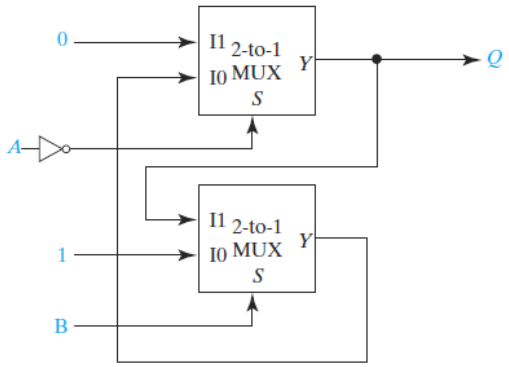
Name_____ **Student ID**_____ **Colleges & Schools**_____ **Department**_____

Homework Unit 11 Solutions

1. Analyze the latch circuit shown below.



(a) Construct a state table for this circuit and identify the stable states of the circuit.

Sol.) A state table is shown below and the circle represents the stable states.

Present State Q	Next State Q^+ AB 0 0	AB 0 1	AB 1 1	AB 1 0
0	(0)	(0)	(0)	1
1	0	0	(1)	(1)

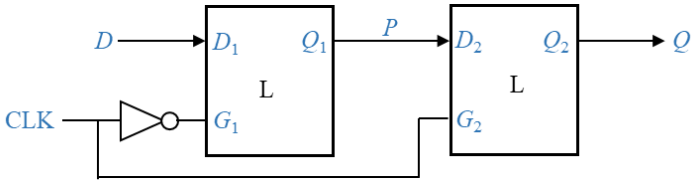
(b) Derive a Boolean algebra equation for the next value of the output Q in terms of Q, A and B.

Sol.) Q+ = A(B'+Q)

(c) Analyze the behavior of the circuit. Is it a useful circuit?

Sol.) This is a reset dominant latch where A' acts a reset and B' acts as a set.

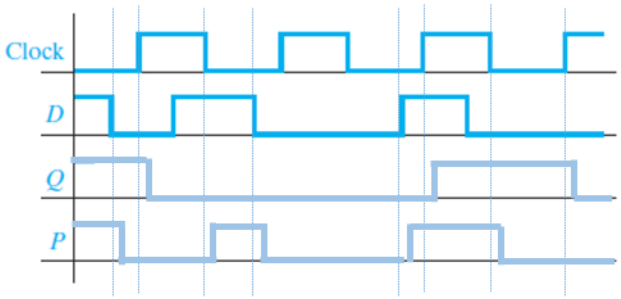
2. Complete the following diagrams for the rising-edge-triggered D flip-flop shown below.



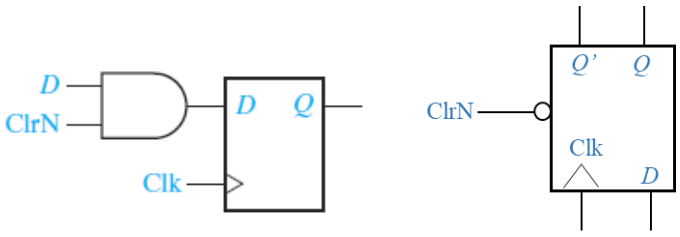
(a) First draw Q based on the behavior of a D flip-flop.

(b) Draw in the internal signal P.

Sol.)



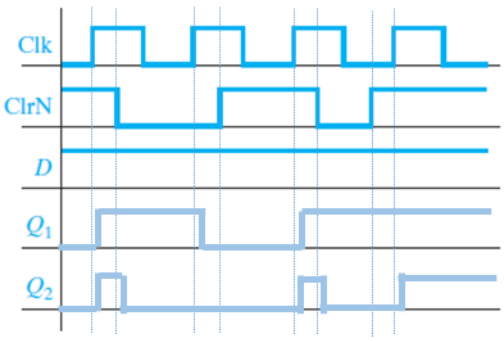
3. The ClrN and PreN inputs are called asynchronous because they operate independently of the clock (i.e., they are not synchronized with the clock). We can also make flip-flops with synchronous clears or preset inputs. A D-flip-flop with an active-low synchronous ClrN input may be constructed from a regular D flip-flop as follows.



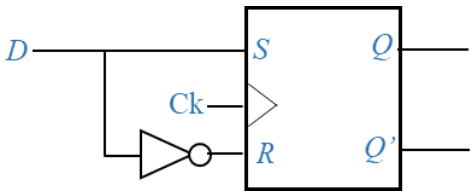
(a) (b)

Fill in the timing diagram. For Q_1, assume a synchronous ClrN as in Figure (a), and for Q_2, assume an asynchronous ClrN as in Figure (b). Assume $Q_1 = Q_2 = 0$ at the beginning.

Sol.)



4. (a) Construct a D flip-flop using an inverter and an S-R flip-flop. (Hint: When D = 0, $Q^+ = 0$, and when D = 1, $Q^+ = 1$, i.e., $Q^+ = D$)



Sol.) When D = 0, then S = 0, R = 1, so $Q^+ = 0$.

When D = 1, then S = 1, R = 0, so $Q^+ = 1$.

(b) If the propagation delay and setup time of the S-R flip-flop in (a) are 2.5ns and 1.5ns, respectively, and if the inverter has a propagation delay of 1ns, what are the propagation delay and setup time of the D flip-flop of part (a)?

Sol.)

R will not be ready until D goes through the inverter, so we must add the delay of the inverter to the setup time. Thus, Setup time = 1.5 + 1 = 2.5ns.

Propagation delay for the D flip-flop is 2.5ns which is same as for the S-R flip-flop, since the propagation delay is measured with respect to the clock.