Name_____ **Student ID**_____ **Colleges & Schools**_____ **Department**_____

Pretest Solutions

1. The following PLA will be used to implement the following equations:

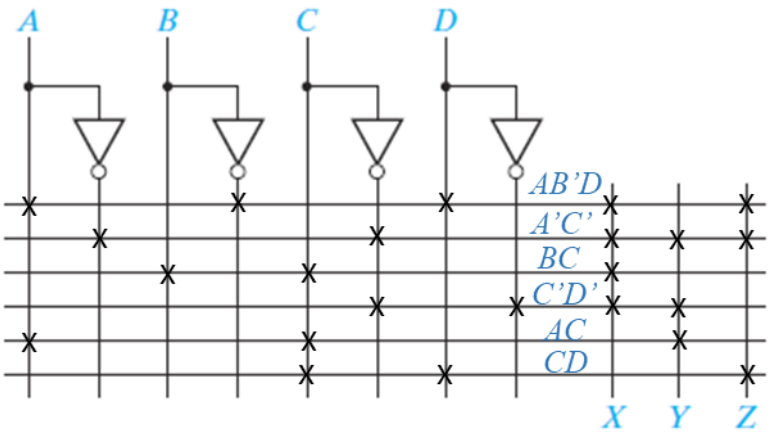
   X = AB′D + A′C′ + BC + C′D′

   Y = A′C′ + AC + C′D′

   Z = CD + A′C′ + AB′D

   (a) Indicate the connections that will be made to program the PLA to implement these equations.

   Sol.)



   (b) Specify the truth table for a ROM which realizes these same equations.

   Sol.)

A B C D	X Y Z
0 0 0 0	1 1 1
0 0 0 1	1 1 1
0 0 1 0	0 0 0
0 0 1 1	0 0 1
0 1 0 0	1 1 1
0 1 0 1	1 1 1
0 1 1 0	1 0 0
0 1 1 1	1 0 1
1 0 0 0	1 1 0
1 0 0 1	1 0 1
1 0 1 0	0 1 0
1 0 1 1	1 1 1
1 1 0 0	1 1 0
1 1 0 1	0 0 0
1 1 1 0	1 1 0
1 1 1 1	1 1 1

2. A U-V flip-flop behaves as follows:

If *UV* = 00, the flip-flop does not change state.

If *UV* = 10, the flip-flop is set to Q = 0.

If *UV* = 11, the flip-flop changes states.

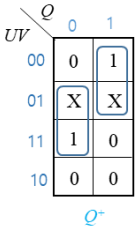
The input combination UV = 01 is not allowed.

(a) Give the characteristic (next state) equation for this flip-flop.

Sol.)

Q	UV = 00	UV = 01	UV = 11	UV = 10
0	0	x	1	0
1	1	x	0	0

$Q^+ = U'Q + VQ'$



(b) Complete the following table, using don't-cares where possible.

(Sol.)

Q Q^+	U V
00	x 0
01	1 1
10	1 x
11	0 0

(c) Realize the following next-state equation for Q using a U-V flip-flop: $Q^+ = A + BQ$. Find equations for U and V.

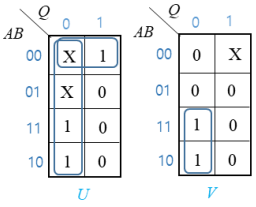
Sol.)

Q	Q^+ AB = 00	AB = 01	AB = 11	AB = 10
0	0	0	1	1
1	0	1	1	1

Q	U V AB = 00	AB = 01	AB = 11	AB = 10
0	x0	x0	11	11
1	1x	00	00	00

$U = A'B' + Q'$

$V = AQ'$



3. Design a 3-bit counter which counts in the sequence:

001, 100, 101, 111, 110, 010, 011, (repeat) 001, …

Sol.)

A B C	$A^+B^+C^+$
0 0 0	X X X
0 0 1	1 0 0
0 1 0	0 1 1
0 1 1	0 0 1
1 0 0	1 0 1
1 0 1	1 1 1
1 1 0	0 1 0
1 1 1	1 1 0

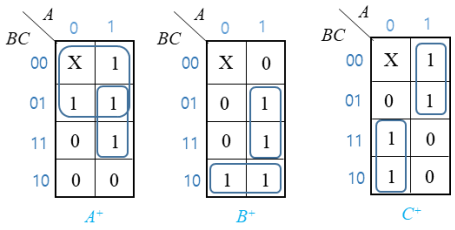
TABLE 12-9 Determination of Flip-Flop Input Equations from Next-State Equations Using Karnaugh Maps

Type of Flip-Flop	Input	$Q = 0$		$Q = 1$		Rules for Forming Input Map From Next-State Map*	
		$Q^+ = 0$	$Q^+ = 1$	$Q^+ = 0$	$Q^+ = 1$	$Q = 0$ Half of Map	$Q = 1$ Half of Map
Delay	D	0	1	0	1	no change	no change
Toggle	T	0	1	1	0	no change	complement
Set-Reset	S	0	1	0	X	no change	replace 1's with X's**
	R	X	0	1	0	replace 0's with X's**	complement
J-K	J	0	1	X	X	no change fill	fill in with X's
	K	X	X	1	0	in with X's	complement

Q^+ means the next state of Q
X is a don't-care
*Always copy X's from the next-state map onto the input maps first.
**Fill in the remaining squares with 0's.

(a) Use D flip-flops.

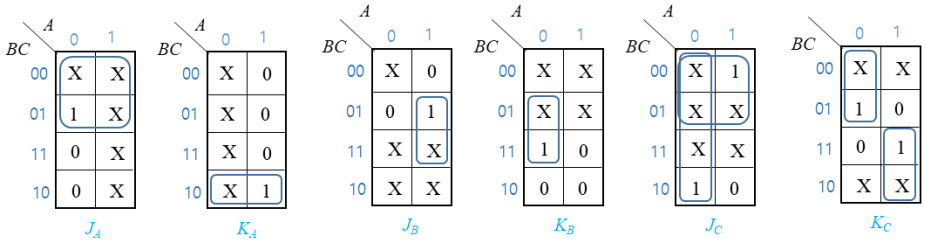
Sol.)



$$D_A = B' + AC;\ D_B = AC + BC';\ D_C = A'B + AB'$$

(b) Use J-K flip-flops.

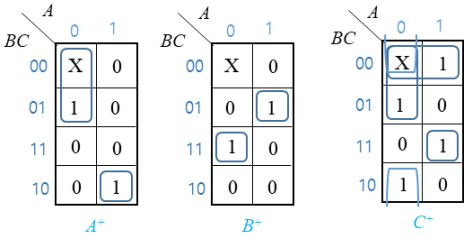
Sol.)



$$J_A = B',\ K_A = BC';\ J_B = AC,\ K_B = A'C;\ J_C = A' + B',\ K_C = A'B' + AB$$

(c) Use T flip-flops.

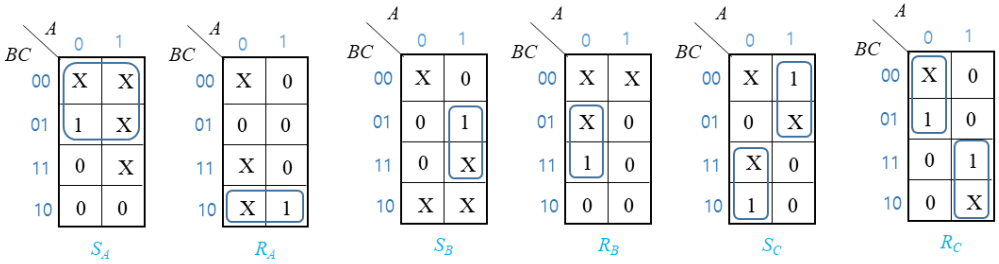
Sol.)



$$T_A = A'B' + ABC';\ T_B = A'BC + AB'C;\ T_C = A'B' + A'C' + B'C' + ABC$$

(d) Use S-R flip-flops.

Sol.)



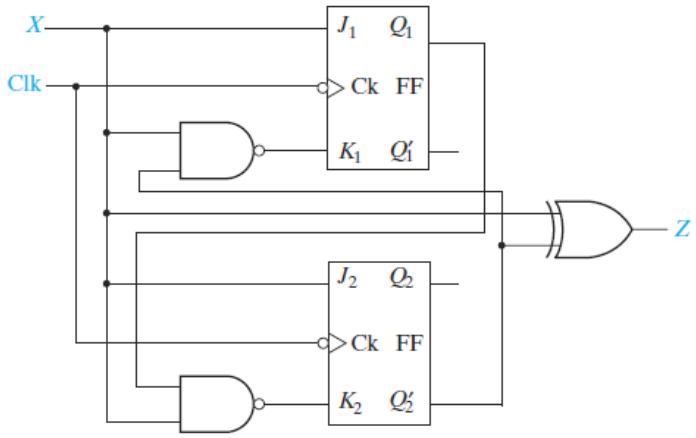
$$S_A = B',\ R_A = BC';\ S_B = AC,\ R_B = A'C;\ S_C = A'B + AB',\ R_C = A'B' + AB$$

(e) What will happen if the counter of (a) is started in state 000?

Sol.)

State 000 goes to 100, because $D_A D_B D_C$ = 100.

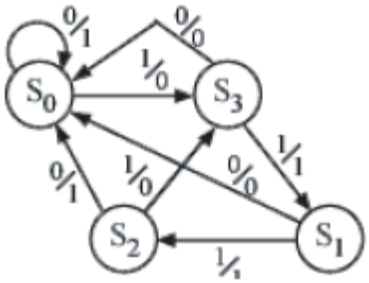
4. (a) Construct a transition table and state graph for the circuit shown below.



Sol.)

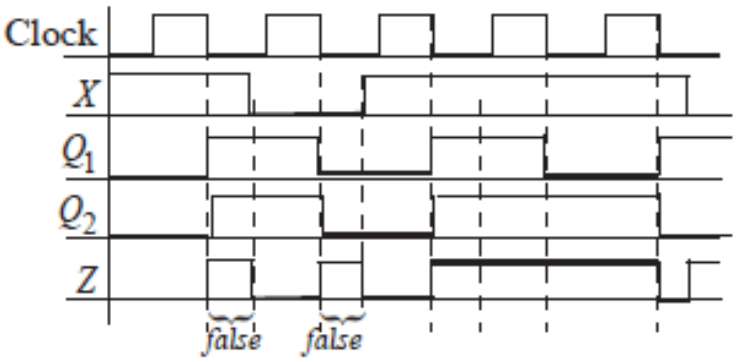
$$Q_1^+ = J_1Q_1' + K_1'Q_1 = XQ_1' + XQ_2'Q_1$$
$$Q_2^+ = J_2Q_2' + K_2'Q_2 = XQ_2' + XQ_1Q_2$$
$$Z = X'Q_2' + XQ_2$$

Present State	Next State $Q_1^+Q_2^+$		Z	
Q_1Q_2	$X=0$	$X=1$	$X=0$	$X=1$
00	00	11	1	0
01	00	10	0	1
11	00	01	0	1
10	00	11	1	0



(b) Construct a timing chart for the circuit for an input sequence X = 10111. (Assume that initially Q1 = Q2 = 0 and that X changes midway between the rising and falling clock edges.)

(Sol.)



(c) List the output values produced by the input sequence.

Sol.) Z = 00011