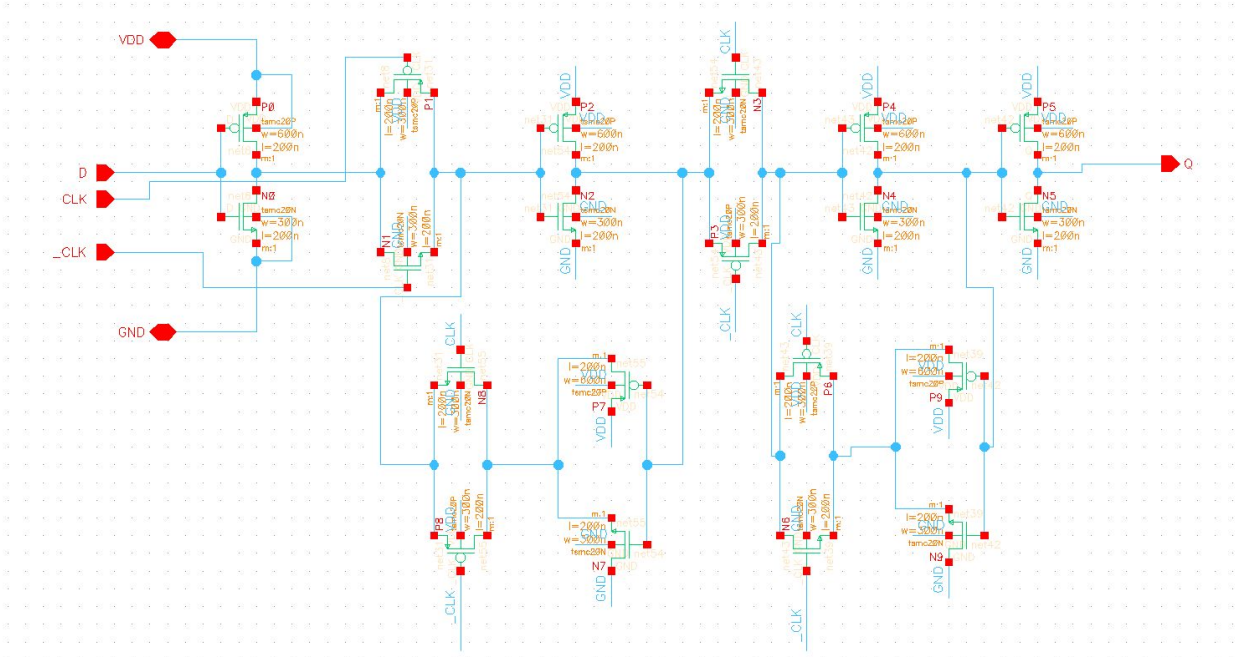
ECEN 454-508

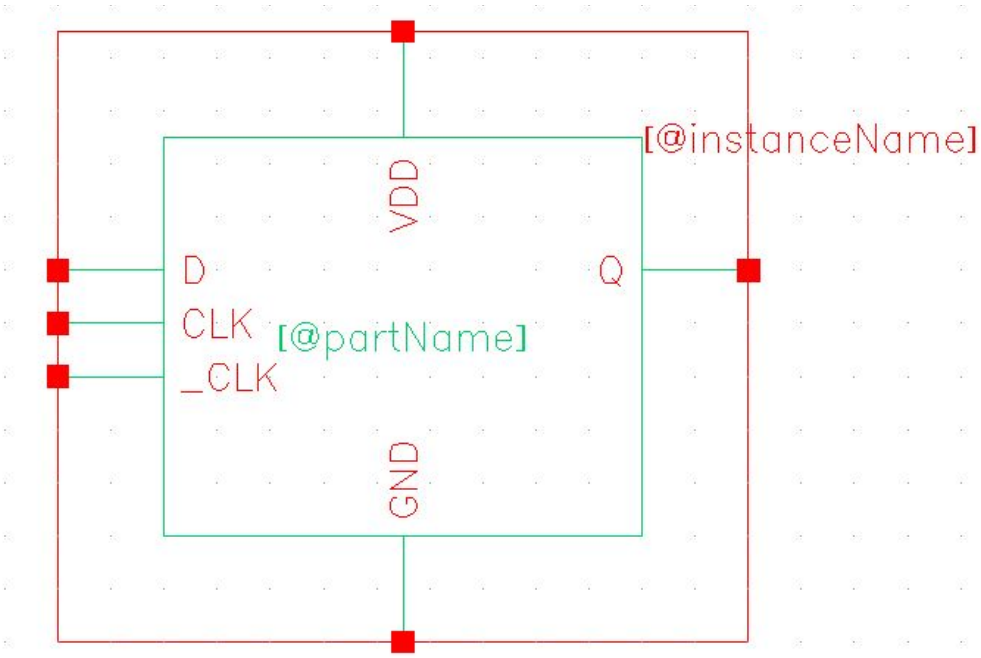
Lab 6

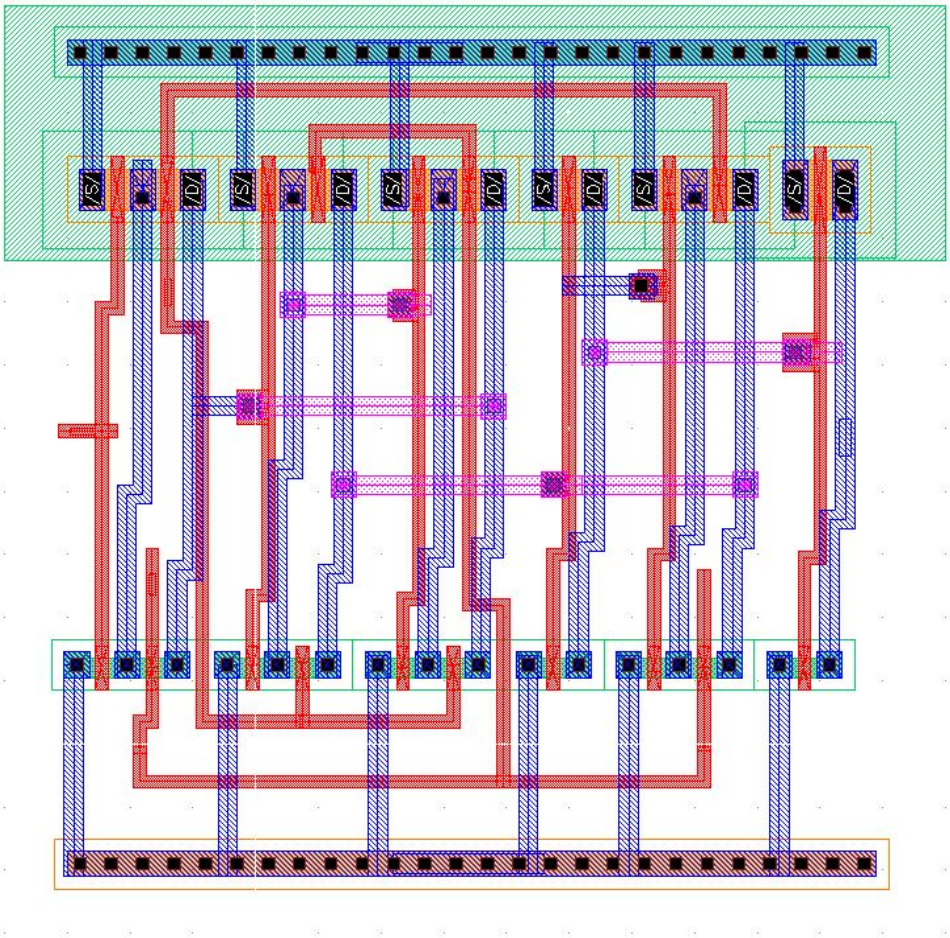
Nicholas Tann

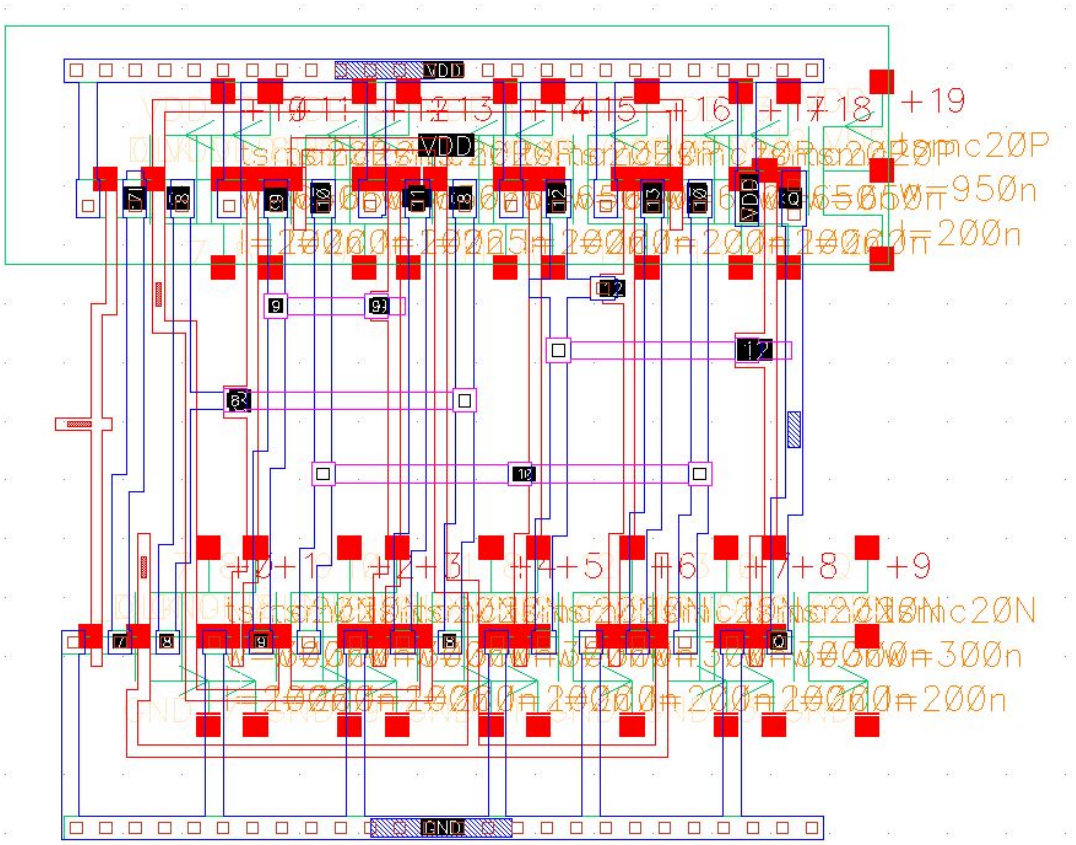
3/1/2020

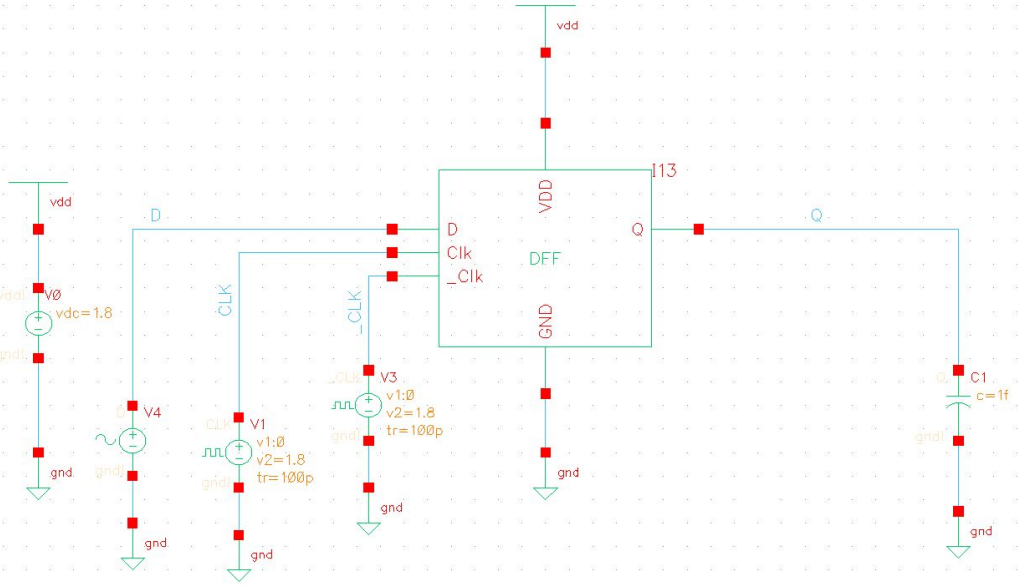
Flip-Flop:

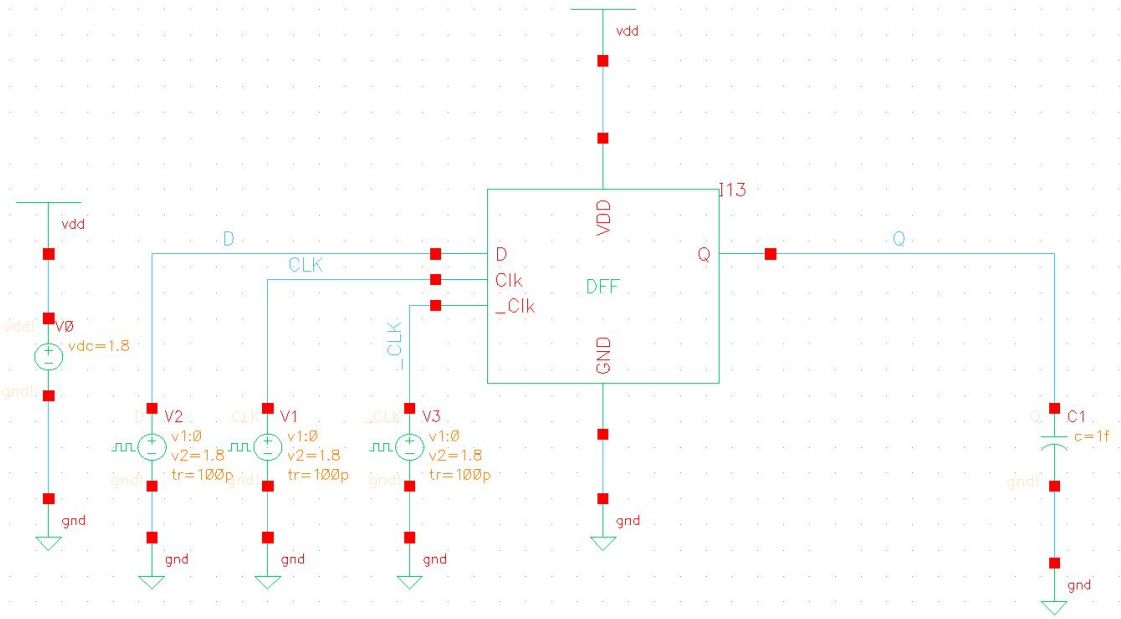


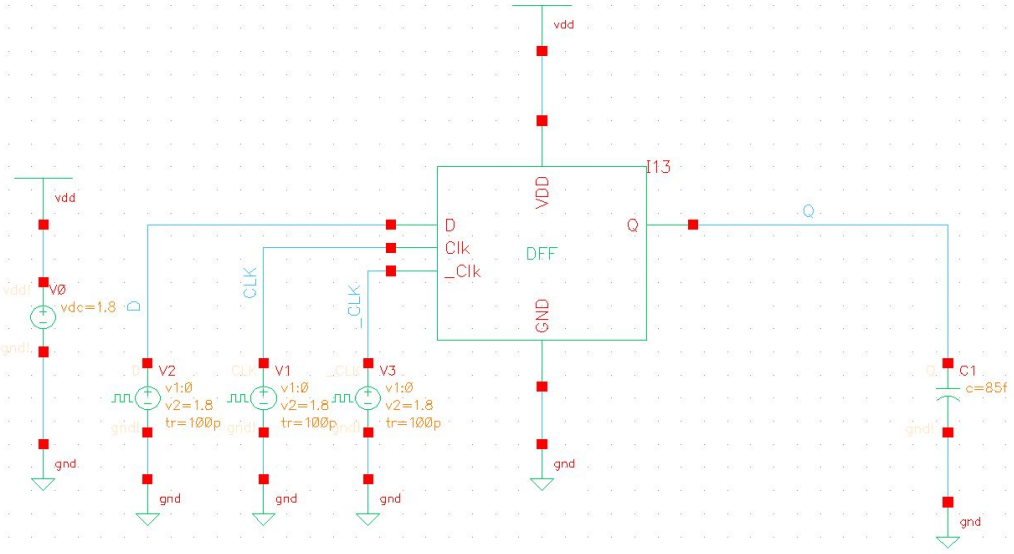



/S
/D
/S
/D
/S
/D
/S
/D
/S
/D
/S
/D

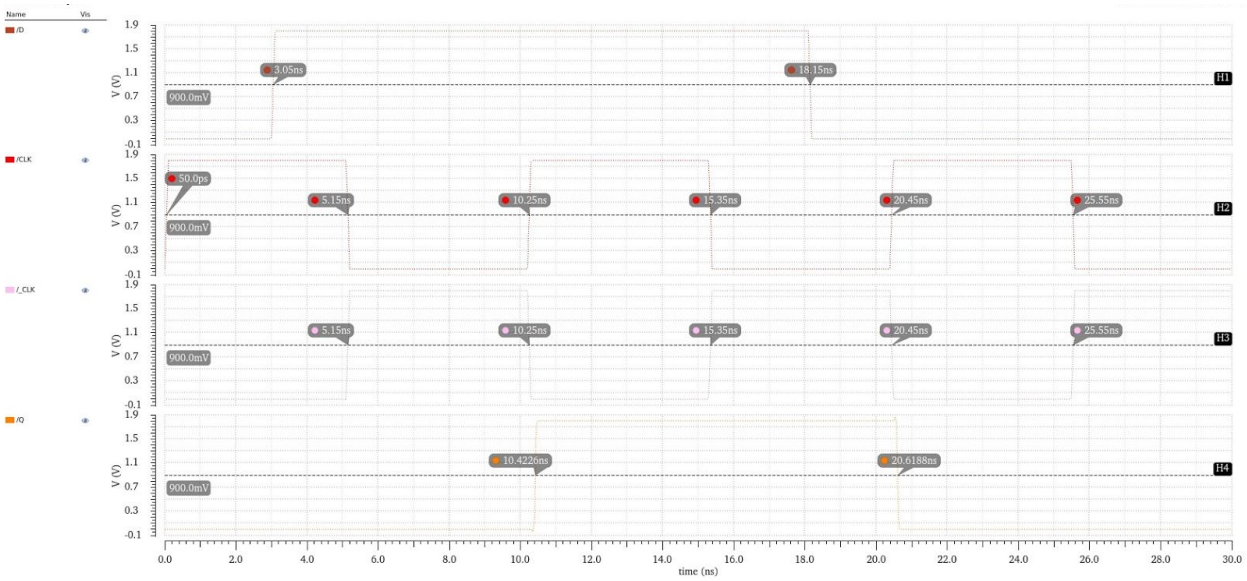

VDD
GND
+19
+9
950n
200n
300n
200n


vdd
D
Clk
_Clk
DFF
Q
GND
I13
V0
vdc=1.8
V4
V1
v1:0
v2=1.8
tr=100p
V3
v1:0
v2=1.8
tr=100p
C1
c=1f
gnd

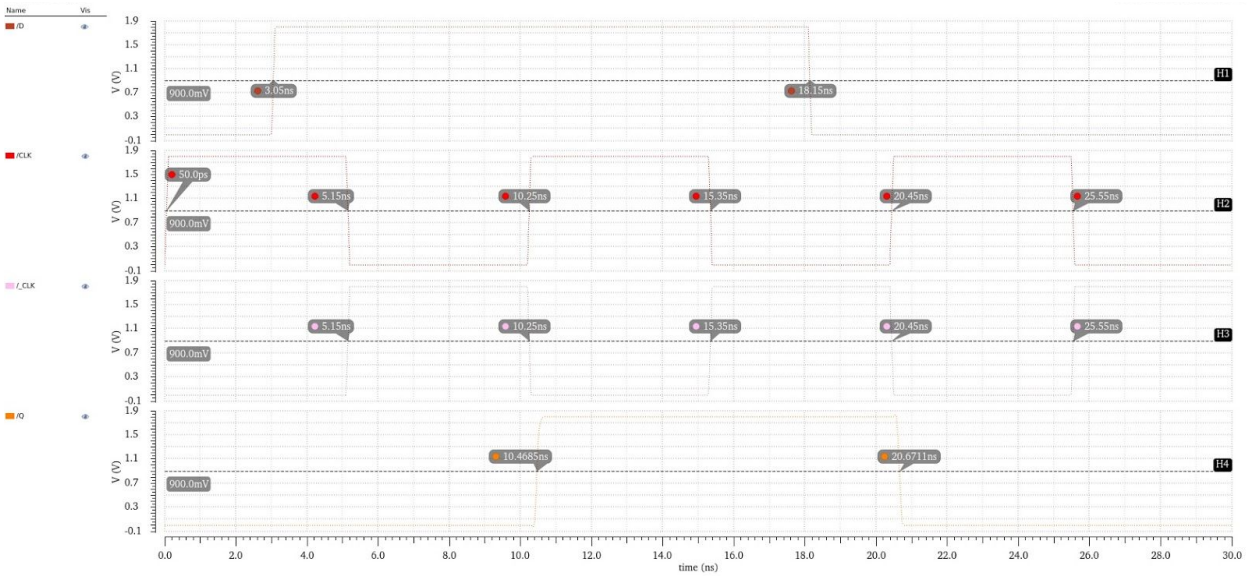

vdd
I13
VDD
D
Clk
_Clk
DFF
Q
GND
Q
D
CLK
_CLK
VØ
vdc=1.8
V2
v1:Ø
v2=1.8
tr=100p
V1
v1:Ø
v2=1.8
tr=100p
V3
v1:Ø
v2=1.8
tr=100p
C1
c=1f
gnd


vdd
I13
VDD
D
Clk
_Clk
DFF
Q
GND
Q
D
CLK
_CLK
VØ
vdc=1.8
V2
v1:Ø
v2=1.8
tr=100p
V1
v1:Ø
v2=1.8
tr=100p
V3
v1:Ø
v2=1.8
tr=100p
C1
c=85f
gnd

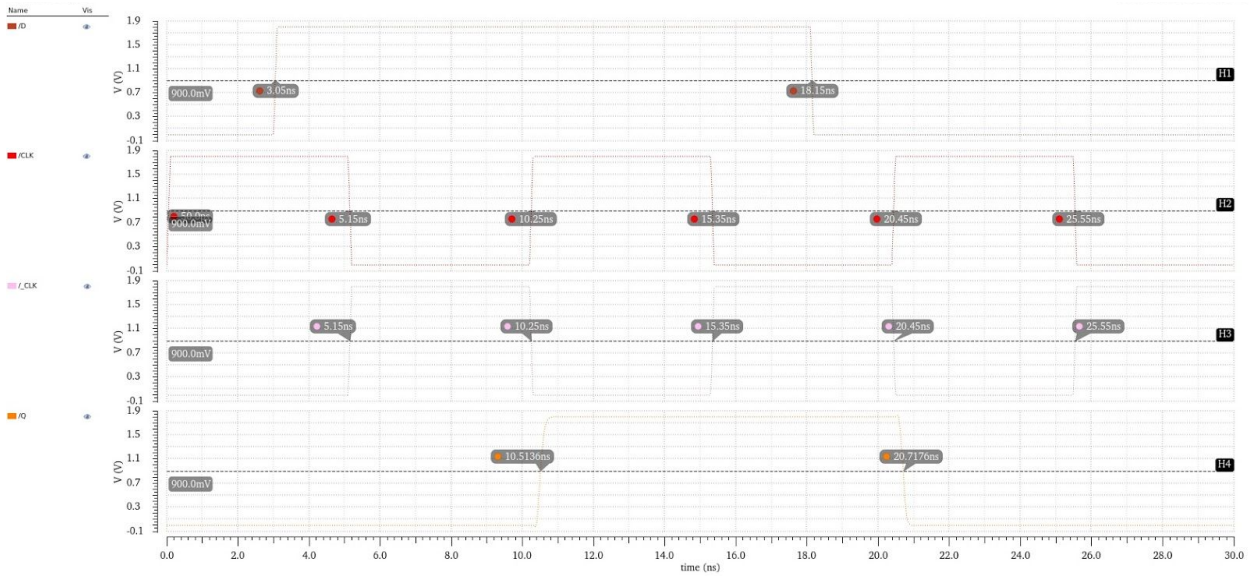
1f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
3.05ns
18.15ns
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
10.4226ns
20.6188ns
900.0mV
H1
H2
H3
H4

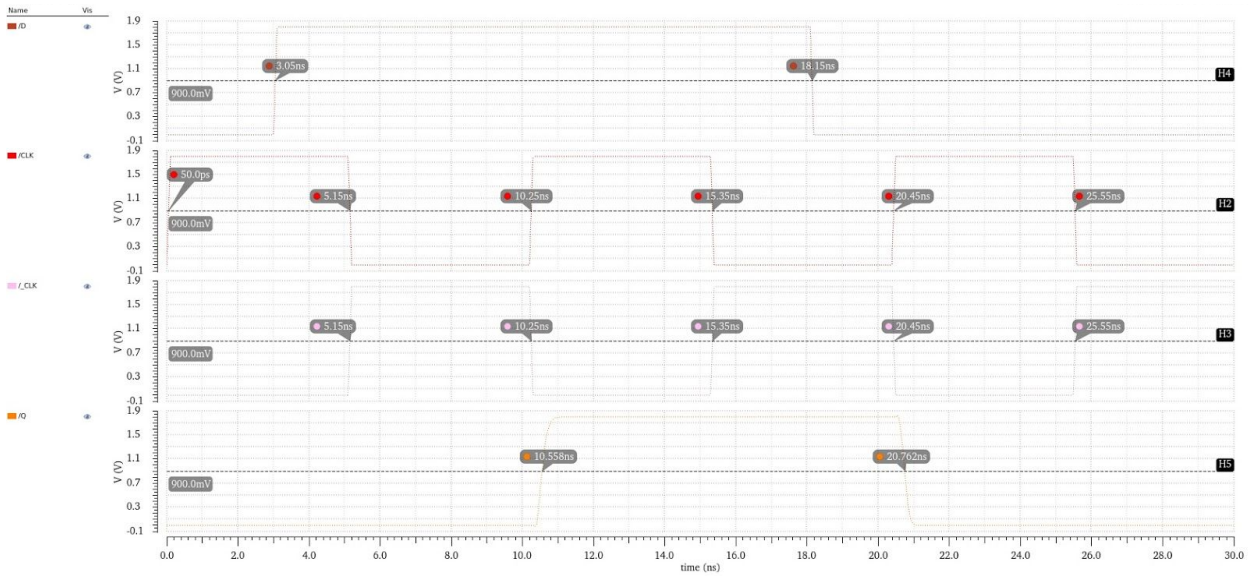
10f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
3.05ns
18.15ns
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
10.4685ns
20.6711ns
900.0mV
H1
H2
H3
H4

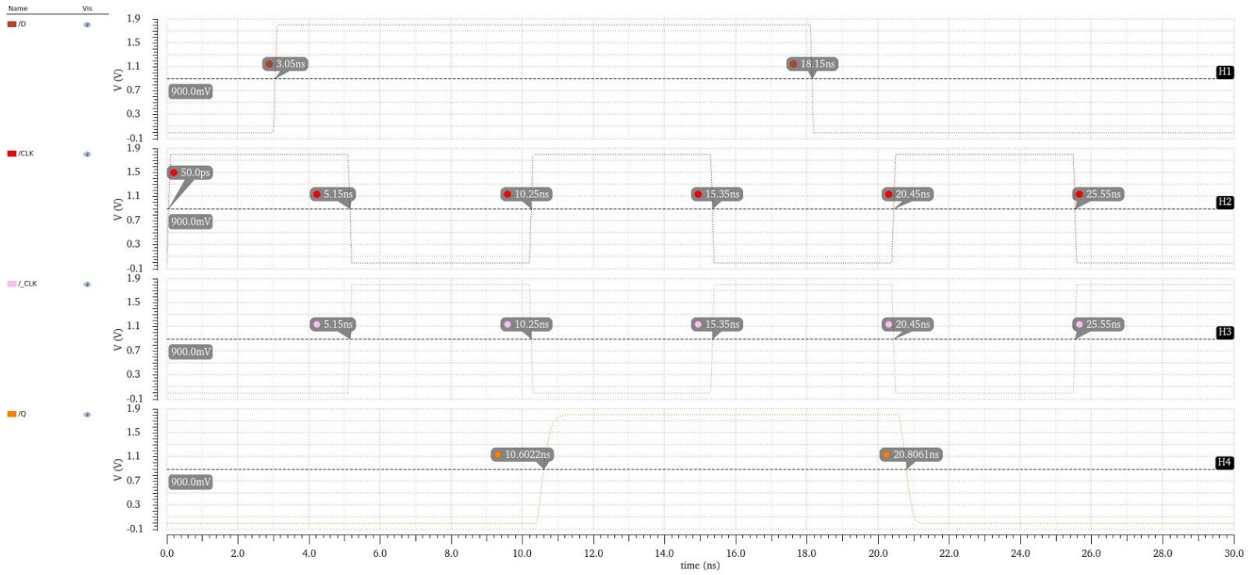
20f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
900.0mV
3.05ns
18.15ns
H1
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.5136ns
20.7176ns
H4

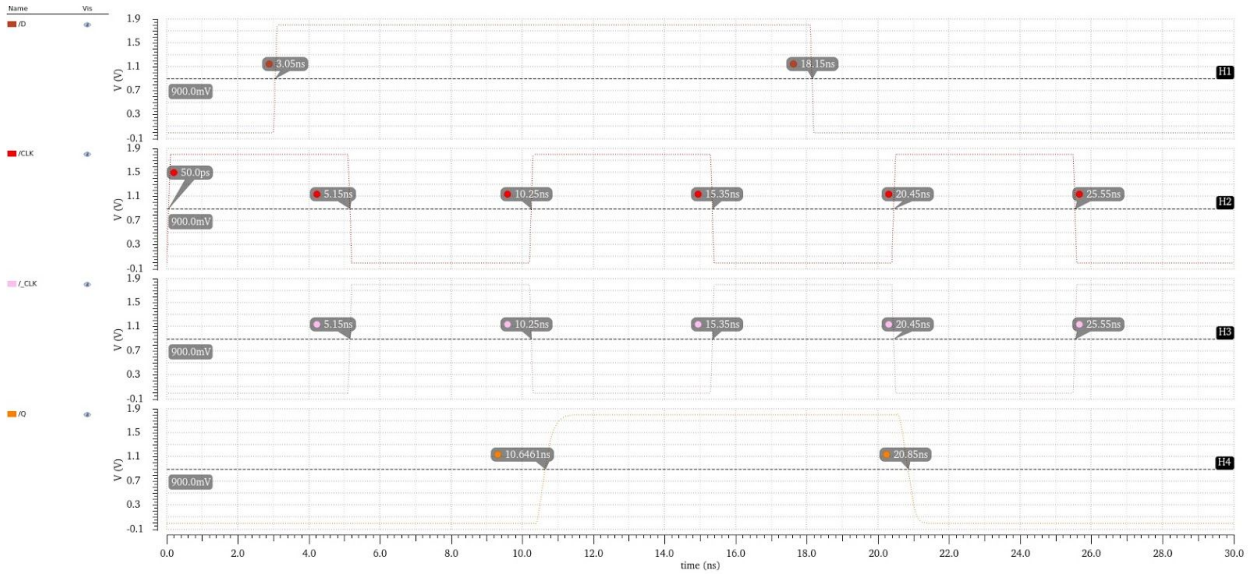
30f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
900.0mV
3.05ns
18.15ns
H4
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.558ns
20.762ns
H5

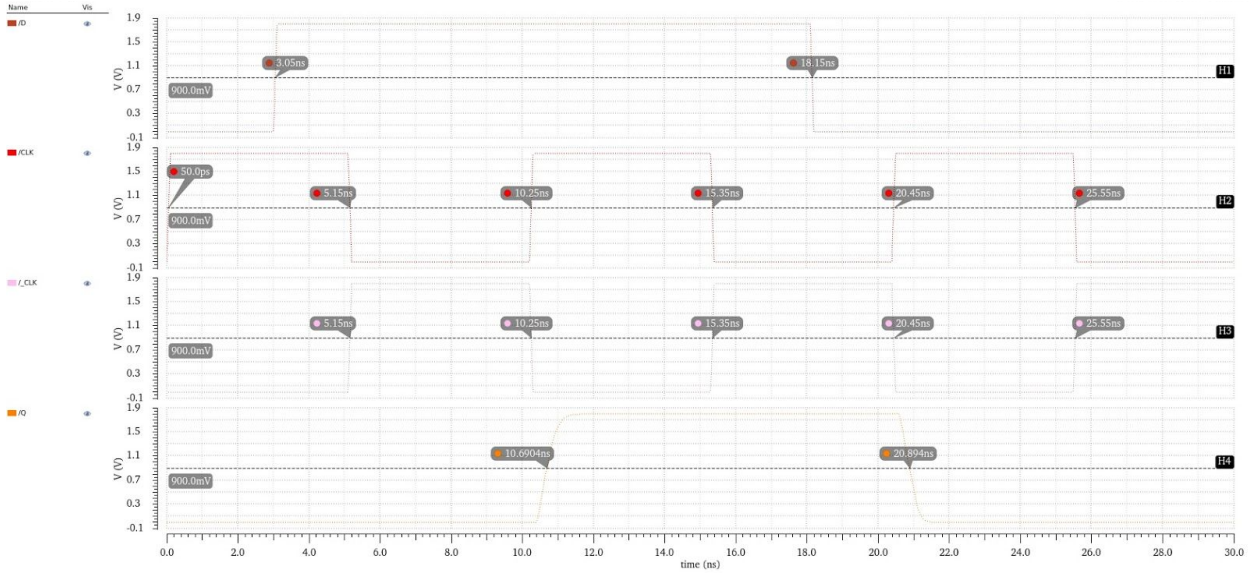
40f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
3.05ns
18.15ns
H1
900.0mV
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.6022ns
20.8061ns
H4
time (ns)

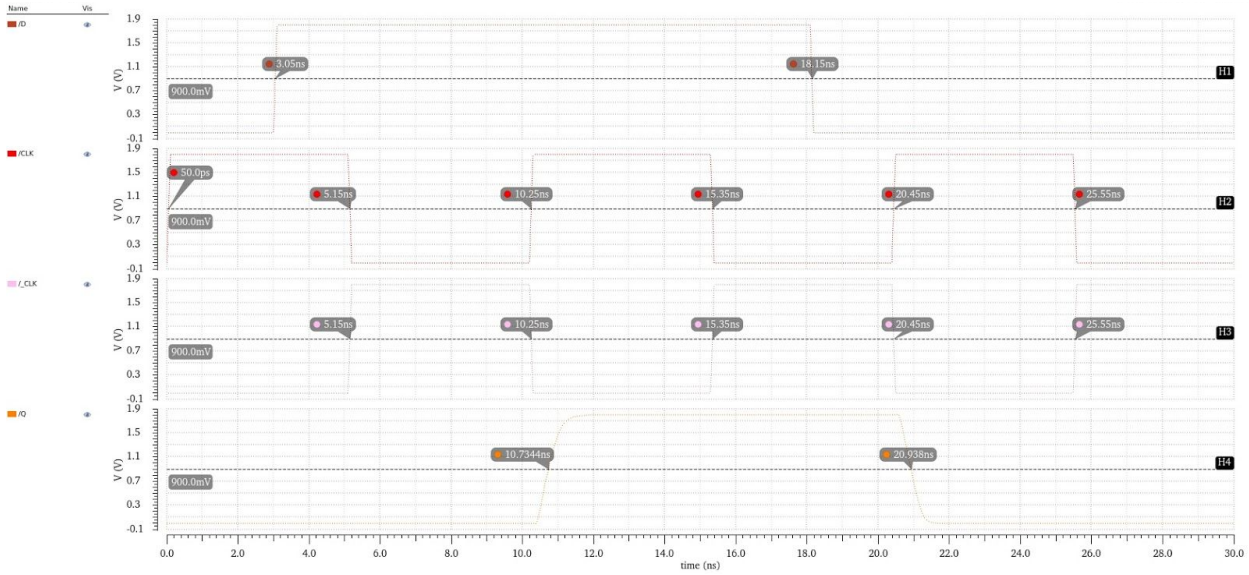
50f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
3.05ns
18.15ns
H1
900.0mV
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.6461ns
20.85ns
H4
time (ns)

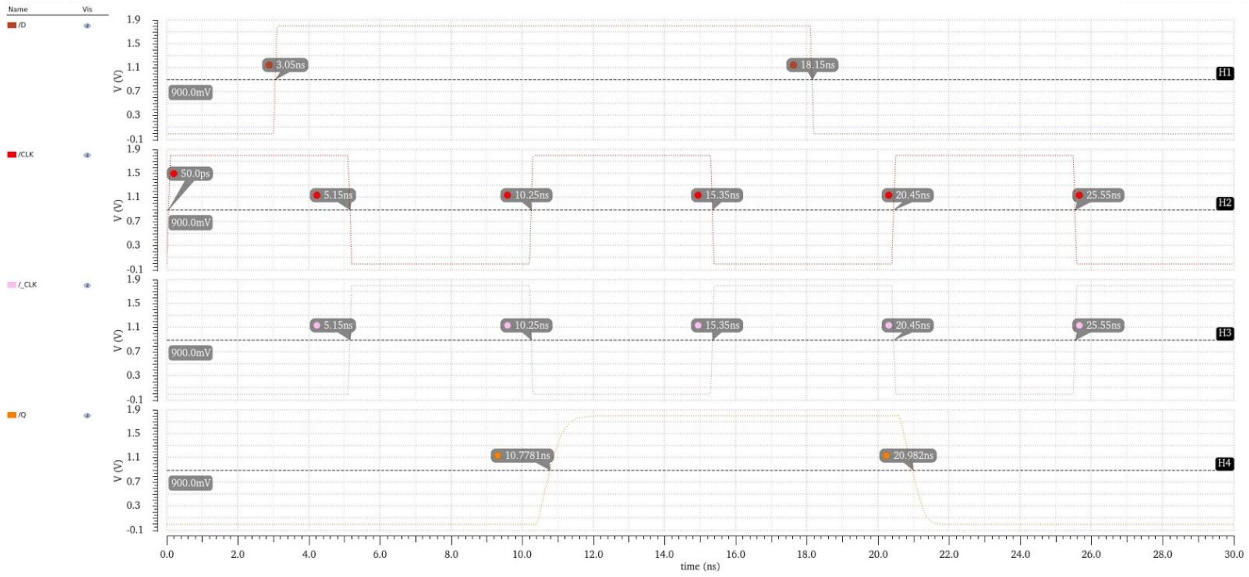
60f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
3.05ns
18.15ns
H1
900.0mV
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.6904ns
20.894ns
H4

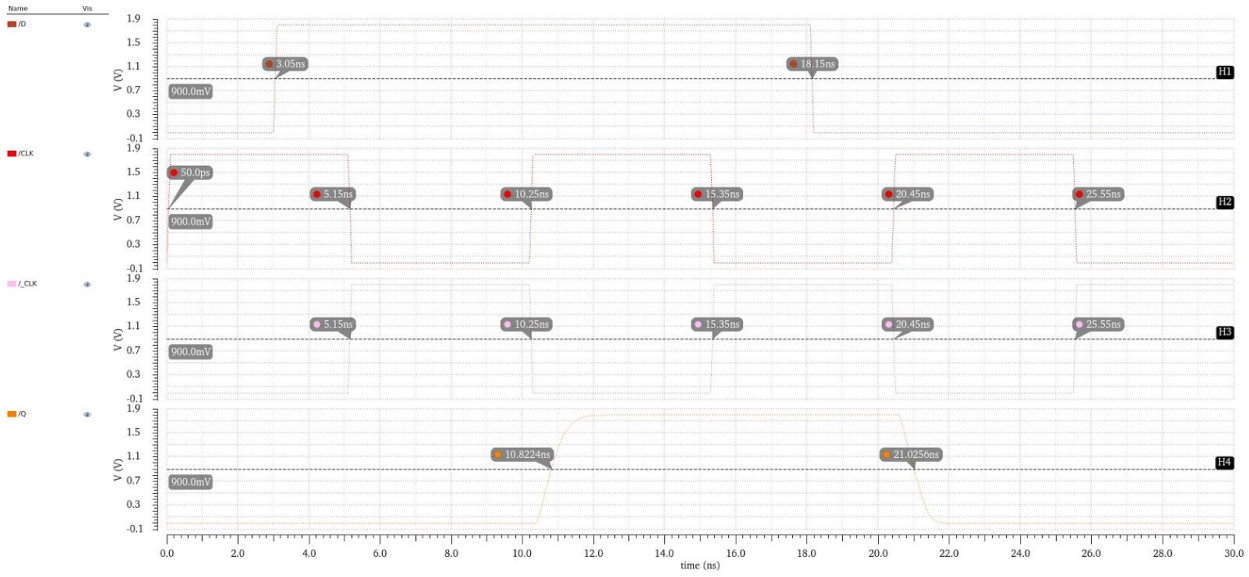
70f


Name
Vis
/D
/CLK
/_CLK
/Q
V (V)
time (ns)
3.05ns
18.15ns
H1
900.0mV
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.7344ns
20.938ns
H4

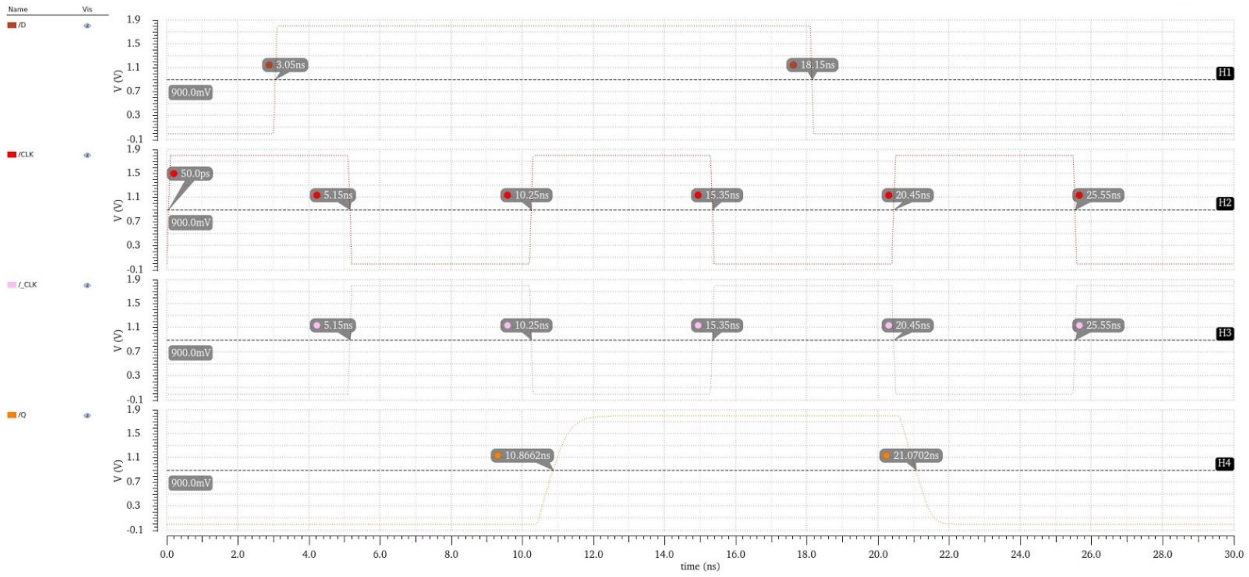
80f


Name
Vis
/D
/CLK
/_CLK
/Q
3.05ns
18.15ns
H1
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.7781ns
20.982ns
H4
900.0mV
V (V)
time (ns)

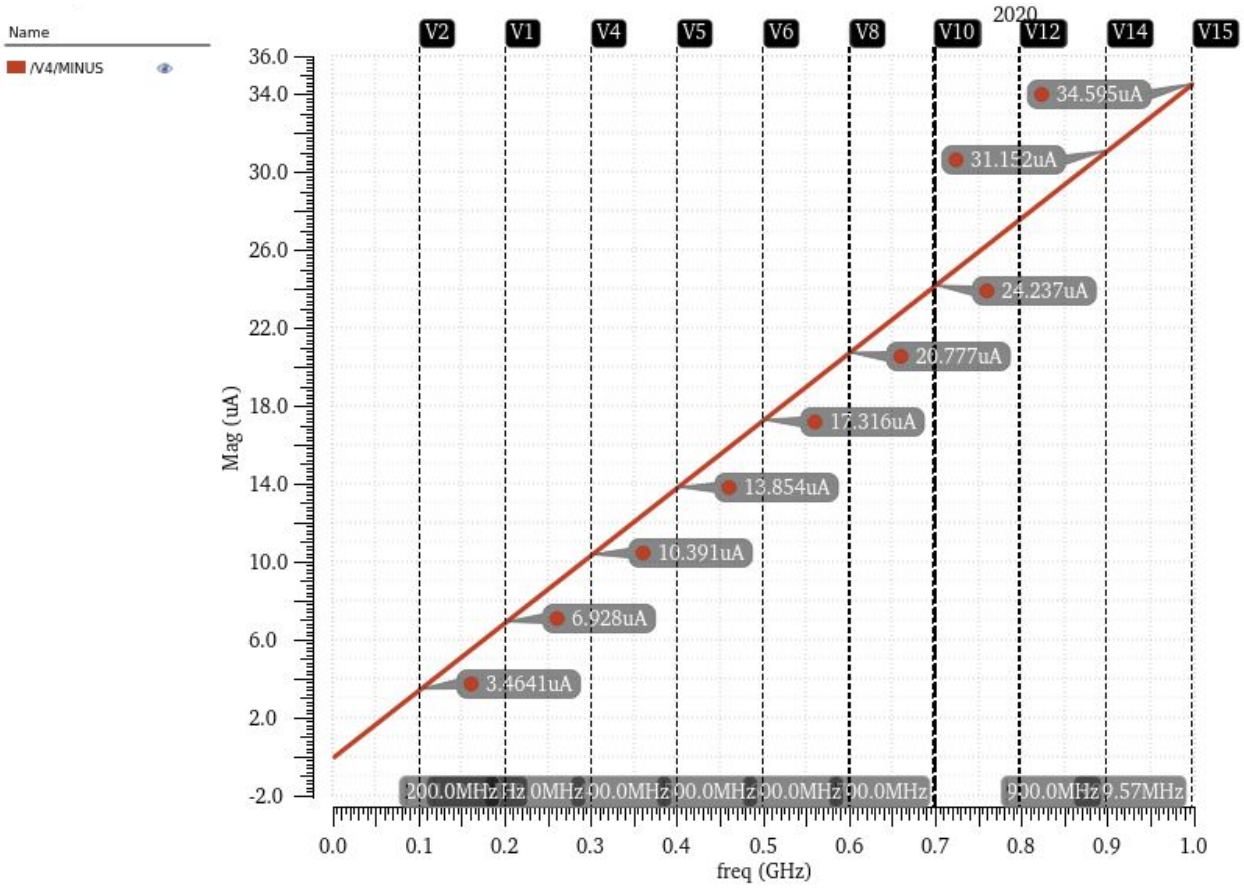
90f


Name
Vis
/D
/CLK
/_CLK
/Q
3.05ns
18.15ns
H1
50.0ps
5.15ns
10.25ns
15.35ns
20.45ns
25.55ns
H2
H3
10.8224ns
21.0256ns
H4
900.0mV
V (V)
time (ns)

100f



	Rising Delay (ps)	**Falling Delay** (ps)
1f	172.6	168.8
10f	218.5	221.1
20f	263.6	267.6
30f	308	312
40f	352.2	356.1
50f	396.1	400
60f	440.4	444
70f	484.4	488
80f	528.1	532
90f	572.4	575.6
100f	616.2	620.2


Name
/V4/MINUS
2020
V2
V1
V4
V5
V6
V8
V10
V12
V14
V15
36.0
34.0
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
Mag (uA)
34.595uA
31.152uA
24.237uA
20.777uA
17.316uA
13.854uA
10.391uA
6.928uA
3.4641uA
200.0MHz
0.0MHz
00.0MHz
00.0MHz
00.0MHz
00.0MHz
900.0MHz
9.57MHz
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
freq (GHz)

	I (uA)	C (f)
200MHz	3.464	.00275
300MHz	6.928	.00368
400MHz	10.391	.00414
500MHz	13.854	.00441
600MHz	17.316	.00459
700MHz	20.777	.00473
800MHz	24.237	.00482
900MHz	31.152	.00551
1000MHz	34.595	.00551

Avg Capacitance = .00445f

D (ns)	Q (ns)	D - Q (ns)
2.800000	2.80000	0
2.807143	2.807143	0
2.814286	2.814286	0
2.821429	2.821429	0
2.828571	2.828571	0
2.835714	2.835714	0
2.842857	2.842859	.000002
2.850000	2.850031	.000031
2.857143	2.857166	.000023
2.864286	2.864300	.000014
2.874290	2.874310	.000020

2.878572	2.878607	.000035
2.885715	2.885771	.000056
2.892858	2.892938	.000080
2.900000	2.900094	.000094
2.907143	2.908225	.000182
2.914286	2.914989	.000703

Setup time is the time difference between the D input and clock input when the FF reaches a meta-stable state. This can be observed when either The D input does not cause a change in output in the present clock cycle or the clock-to-Q delay increases drastically or there are oscillations in the output between 0 and 1.

In that case setup time = .000703 ns

Net-list summary for /home/ugrads/n/ntann/ECEN454/Lab6/LVS/layout/netlist

count	
13	nets
6	terminals
10	pmos
10	nmos

Net-list summary for /home/ugrads/n/ntann/ECEN454/Lab6/LVS/schematic/netlist

count	
13	nets
6	terminals
10	pmos
10	nmos

Terminal correspondence points

N10	N2	CLK
N11	N11	D
N7	N5	GND
N8	N12	Q

N12 N8 VDD
N9 N10 _CLK

Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	20	20
total	20	20
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	13	13
total	13	13
terminals		
un-matched	0	0
matched but different type	0	0
total	6	6

Probe files from /home/ugrads/n/ntann/ECEN454/Lab6/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/ugrads/n/ntann/ECEN454/Lab6/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

DRC started.....Sat Feb 29 15:15:20 2020
completed ....Sat Feb 29 15:15:20 2020
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "dff0 layout" *********
Total errors found: 0