ECEN 454-508
Lab 3

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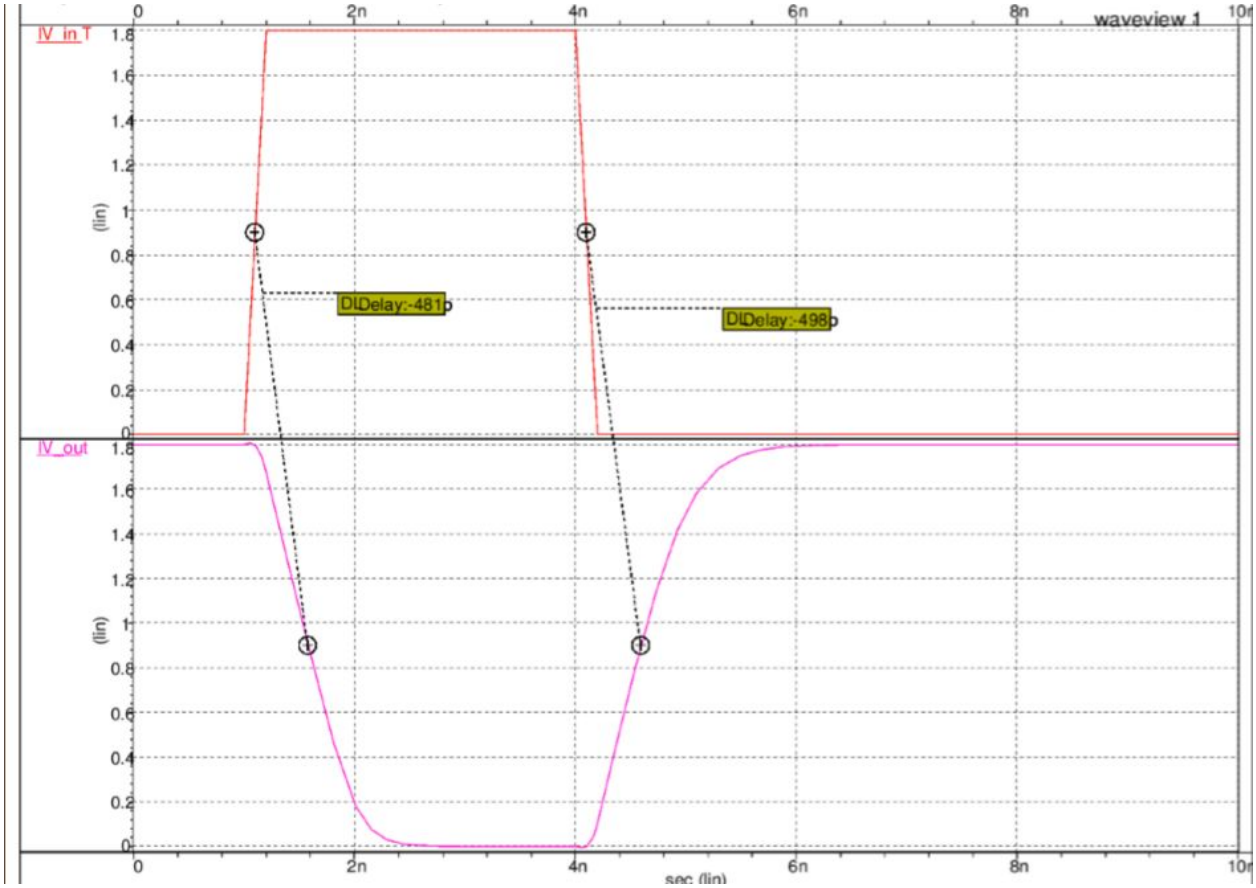
Inverter:



Delays

Rising - 498ps
Falling - 481ps

Delay Table

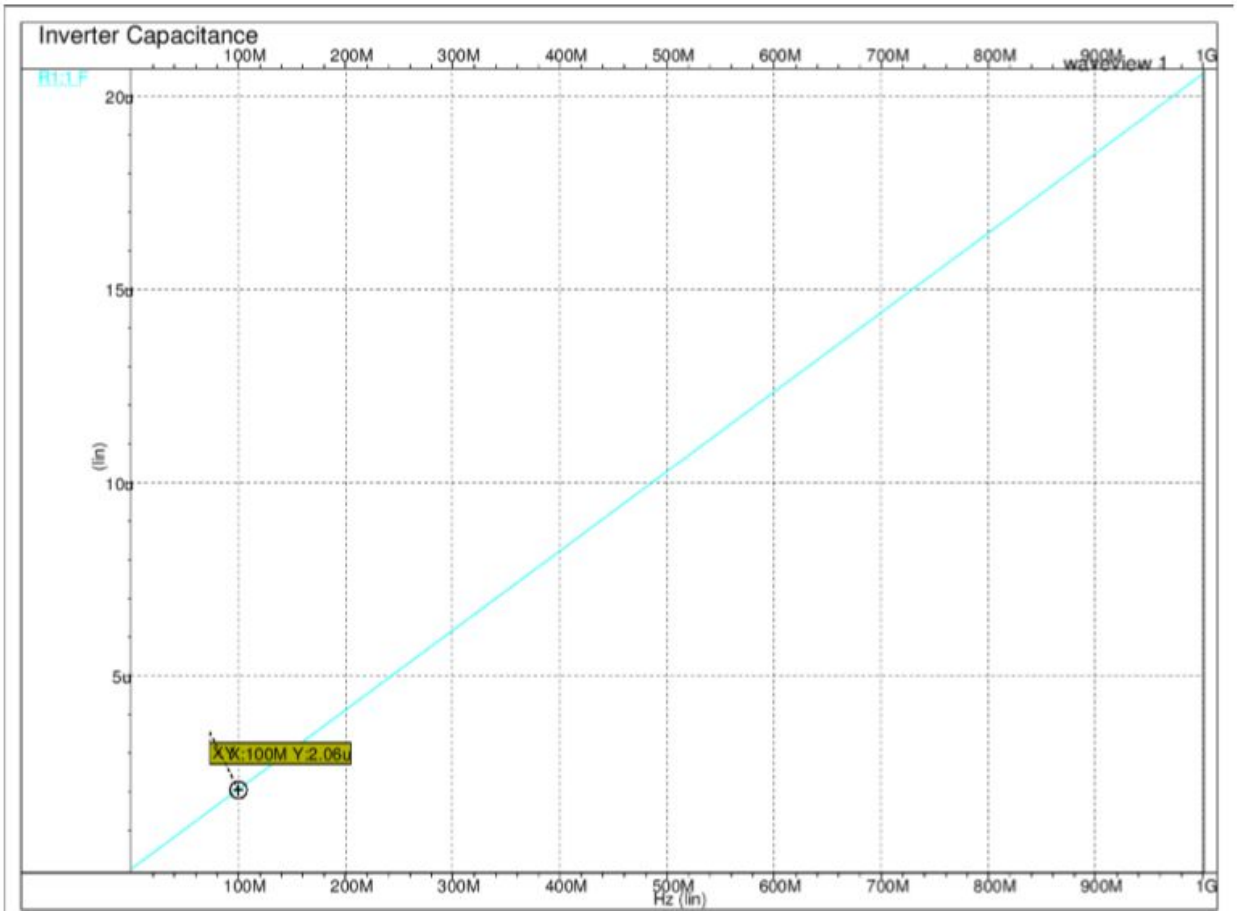
Capacitance (f)	Rising Delay (ps)	Falling Delay (ps)	Error %
1	45.2	27.1	66.78
10	101	85.8	17.71
20	144	131	9.92
30	188	175	7.42

40	232	219	5.93
50	277	262	5.72
60	321	306	4.90
70	368	351	4.84
80	410	393	4.32
90	451	439	2.73
100	498	481	3.53

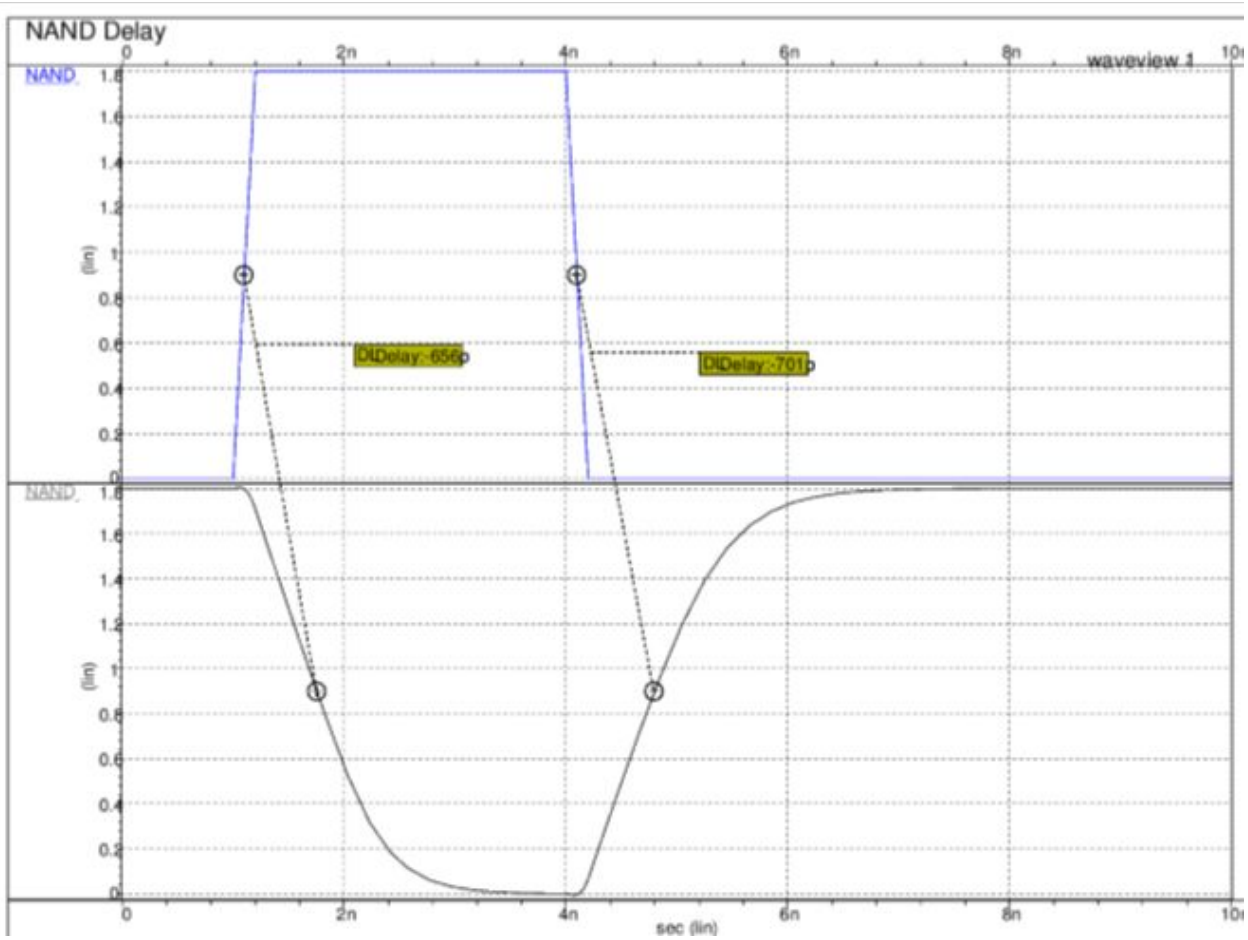
Capacitance

Frequency (MHz)	**Current (uA)**	**Capacitance (fF)**
100	2.06	3.279
200	4.11	3.271
300	6.18	3.279
400	8.24	3.279
500	10.3	3.279
600	12.3	3.263
700	14.4	3.274
800	16.5	3.283
900	18.5	3.272
1000	20.6	3.279

Average Capacitance = 3.2758fF


Inverter Capacitance
100M
200M
300M
400M
500M
600M
700M
800M
900M
1G
waveview 1
R1:1:F
20u
15u
10u
5u
(lin)
X:100M Y:2.06u
Hz (lin)

NAND:



Delays

Rising- 701ps
Falling - 650ps

Delay Table

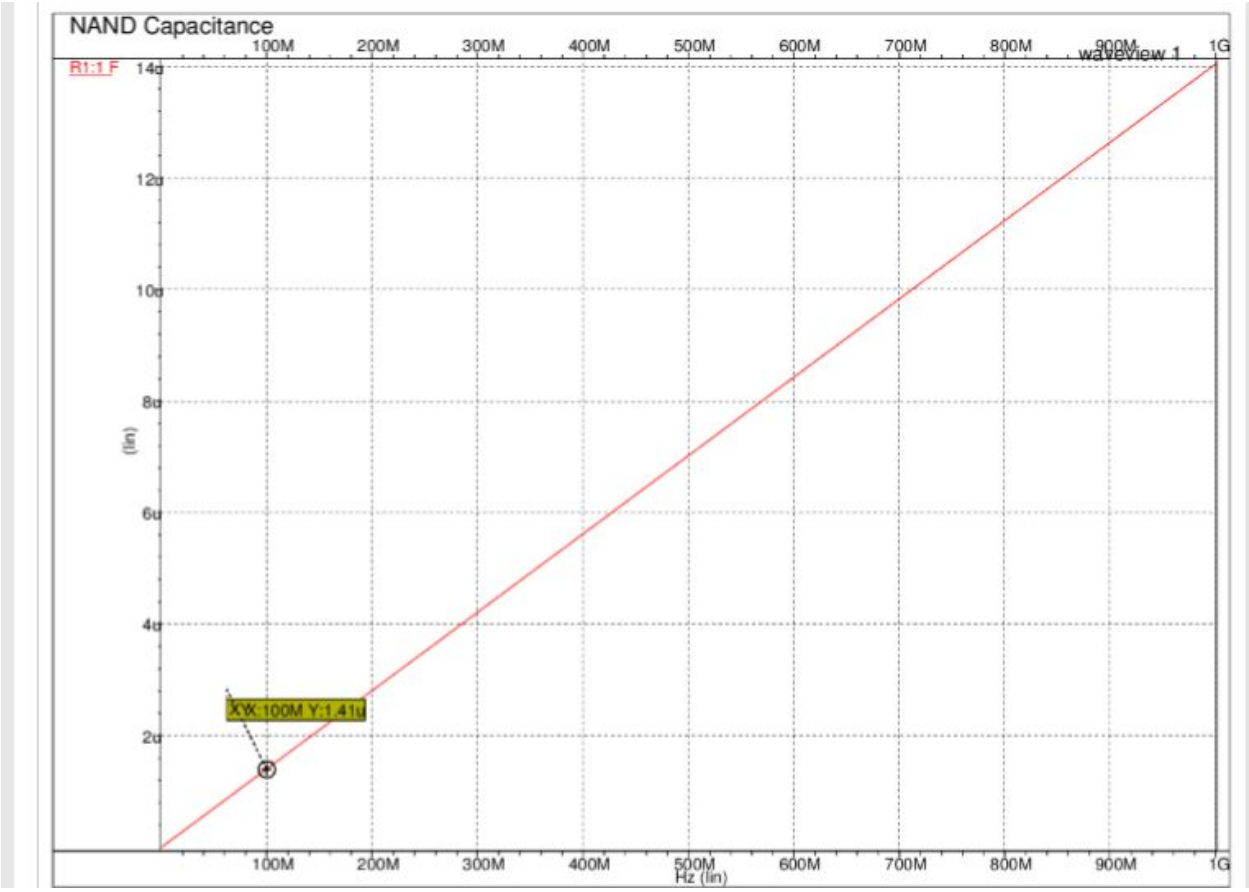
Capacitance (f)	Rising Delay (ps)	Falling Delay (ps)	Error %
1	57.7	35.4	62.99
10	125	107	16.82
20	190	168	13.09
30	254	229	10.91
40	320	291	9.96

50	383	351	9.11
60	447	414	7.97
70	511	474	7.80
80	575	533	7.87
90	637	595	7.05
100	701	656	6.85

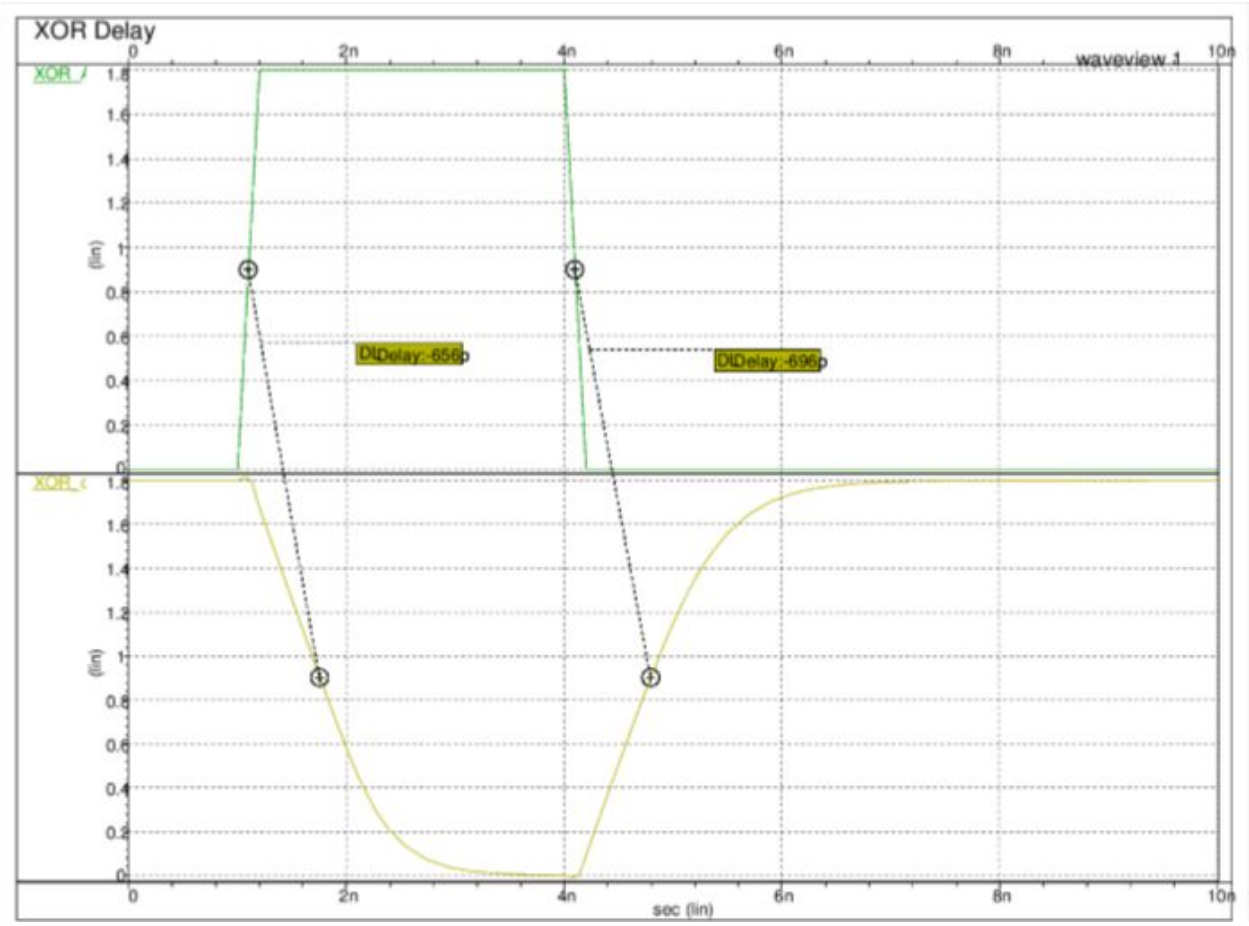
Capacitance Table

Frequency (MHz)	**Current (uA)**	**Capacitance (fF)**
100	1.4	2.228
200	2.81	2.2366
300	4.21	2.335
400	5.62	2.36
500	7.02	2.235
600	8.42	2.233
700	9.83	2.235
800	11.2	2.228
900	12.6	2.228
1000	14.0	2.228

Average Capacitance = 2.2322fF


NAND Capacitance
R1:1 F
waveview 1
14u
12u
10u
8u
6u
4u
2u
(lin)
X:100M Y:1.41u
100M
200M
300M
400M
500M
600M
700M
800M
900M
1G
Hz (lin)

XOR:



Delays

Rising - 696ps
Falling - 656ps

Delay Table

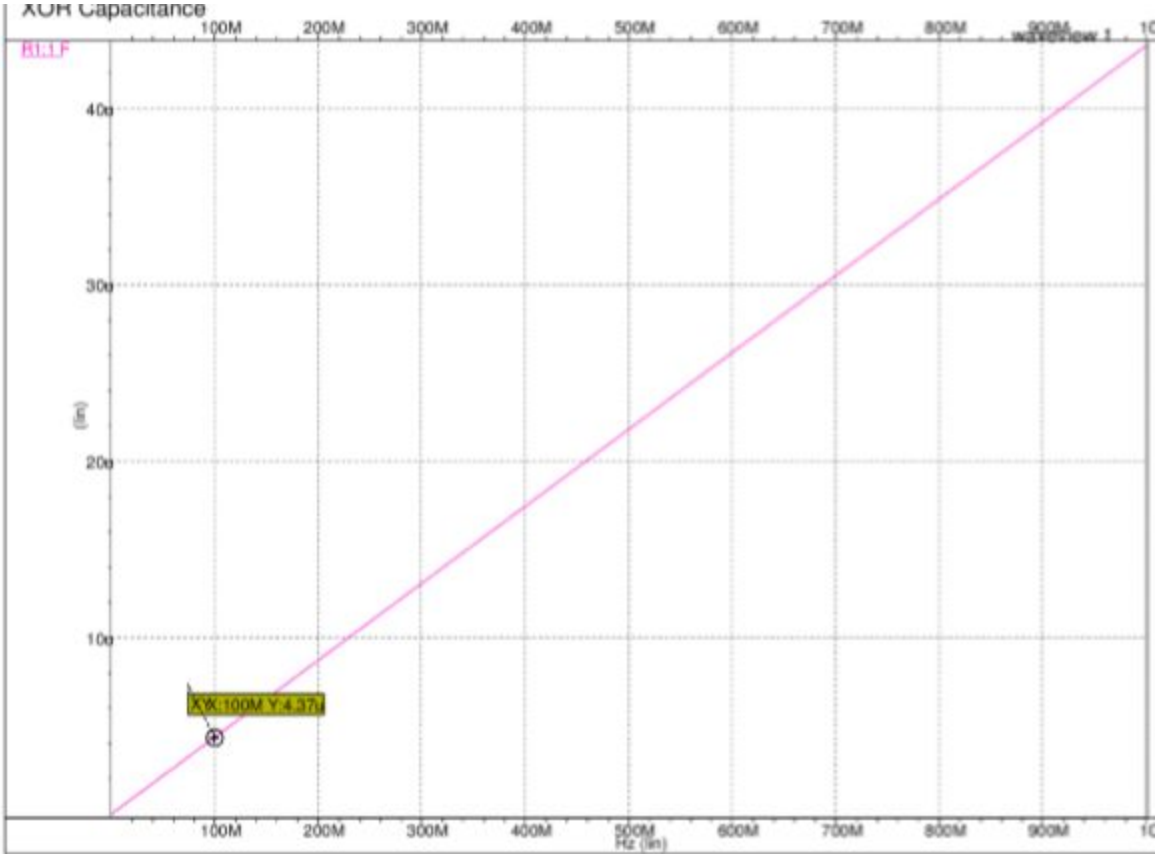
Capacitance (f)	Rising Delay (ps)	Falling Delay (ps)	Error %
1	52.9	39.8	32.91
10	116	103	12.62
20	181	166	9.03
30	247	228	8.33
40	310	290	6.89

50	374	351	6.55
60	439	412	6.55
70	506	474	6.75
80	566	535	5.79
90	633	596	6.20
100	696	656	6.09

Capacitance

Frequency (MHz)	**Current (uA)**	**Capacitance (fF)**
100	4.38	6.971
200	8.74	6.955
300	13.1	6.950
400	17.5	6.963
500	21.8	6.939
600	26.2	6.950
700	30.5	6.935
800	34.9	6.943
900	39.2	6.932
1000	43.6	6.939

Average Capacitance = 6.9477 fF


XOR Capacitance
100M
200M
300M
400M
500M
600M
700M
800M
900M
R1:1 F
40p
30p
20p
10p
(F)
X:100M Y:4.37p
Hz (lin)

Cell18.spi

//Spice netlist for an inverter simulator lang=spectre subckt IV (input output VDD VSS) parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u M1 output input VDD VDD tsmc18P w=wp l=lp M2 output input VSS VSS tsmc18N w=wn l=ln ends IV

//Spice netlist for NAND subckt NAND (A B output VDD VSS) parameters wp=0.6u lp=0.2u wn=0.3u ln=0.2u M1 output A VDD VDD tsmc18P w=wp l=lp M2 output B VDD VDD tsmc18P w=wp l=lp M3 output A w1 VSS tsmc18N w=wn l=ln M4 w1 B VSS VSS tsmc18N w=wn l=ln ends NAND

//Spice netlist for an XOR subckt XOR (A B output VDD VSS) parameters wp=1.2u lp=0.2u wn=0.3u ln=0.2u

inv1(A A_not VDD VSS) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u inv2(B B_not VDD VSS) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u M1 w1 B VDD VDD tsmc18P w=wp l=lp M2 output A_not w1 VDD tsmc18P w=wp l=lp M3 w2 B_not VDD VDD tsmc18P w=wp l=lp M4 output A w2 VDD tsmc18P w=wp l=lp

M5 w3 A_not output VSS tsmc18N w=wn l=ln M6 VSS B_not w3 VSS tsmc18N w=wn l=ln M7 w4 A output VSS tsmc18N w=wn l=ln M8 VSS B w4 VSS tsmc18N w=wn l=ln ends XOR

inverter.spi & inverter_delaytable.spi

```
;Spice netlist for an inverter and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1 C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save IV_in IV_out
```

inverter_simcap.spi

;Spice netlist for an inverter and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9 save R1:currents

NAND.spi & NAND_delaytable.spi

```
;Spice netlist for NAND and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8 vvd (NAND_B 0) vsource dc=1.8

vpwl (NAND_A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND_A NAND_B NAND_OUT vdd gnd) NAND wp=0.6u lp=0.2u wn=0.3u ln=0.2u

R1 (NAND_OUT 1) resistor r=1 C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save NAND_A NAND_B NAND_OUT
```

NAND_simcap.spi

;Spice netlist for an inverter and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8 vvd (NAND_B 0) vsource dc=1.8

acinput (NAND_A 0) vsource dc=0 mag=1

R1 (NAND_A NAND_A1) resistor r=0

X1 (NAND_A1 NAND_B NAND_out vdd gnd) NAND wp=0.6u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9 save R1:currents

XOR.spi & XOR_delaytable.spi

;Spice netlist for an inverter and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8 vvd (XOR_B 0) vsource dc=1.8

vpwl (XOR_A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR_A XOR_B XOR_out vdd gnd) XOR wp=1.2u lp=0.2u wn=0.3u ln=0.2u

R1 (XOR_out 1) resistor r=1 C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save XOR_A XOR_out

XOR_simcap.spi

;Spice netlist for an inverter and a capacitor simulator lang=spectre

include "~/ECEN454/Lab1/spectre/model18.spi" include "~/ECEN454/Lab1/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0 vvdd (vdd 0) vsource dc=1.8 vvd (XOR_B 0) vsource dc=1.8

acinput (XOR_A 0) vsource dc=0 mag=1

R1 (XOR_A XOR_A1) resistor r=0

X1 (XOR_A1 XOR_B XOR_out vdd gnd) XOR wp=1.2u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9 save R1:currents