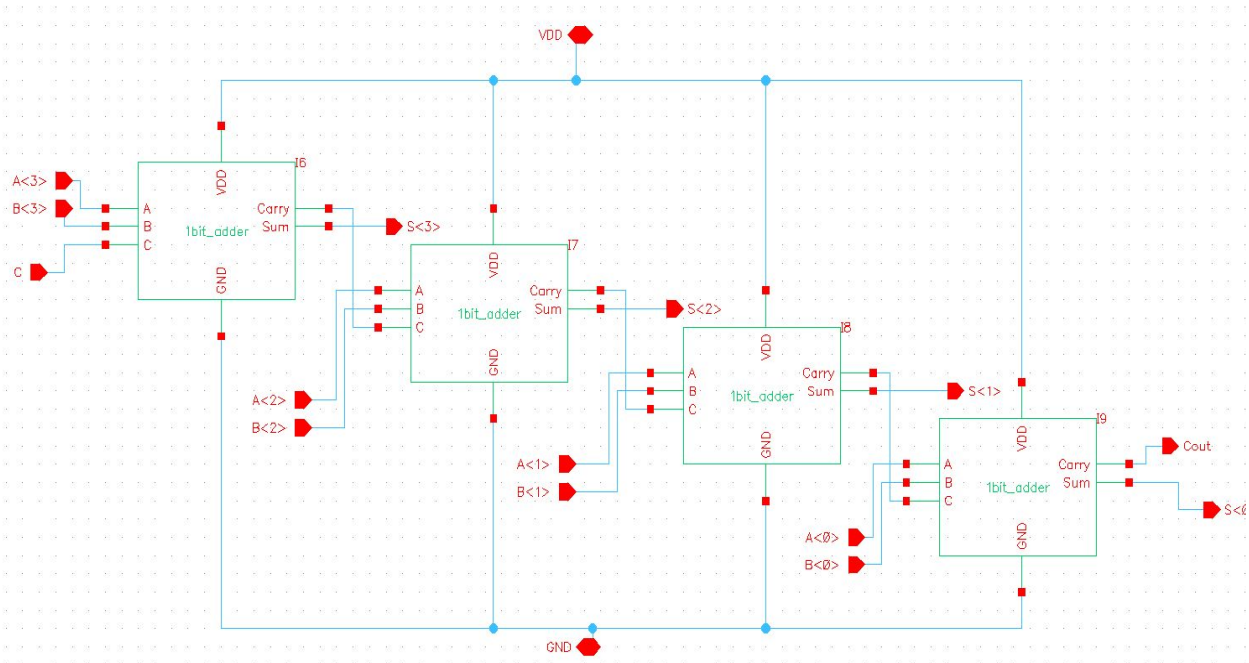
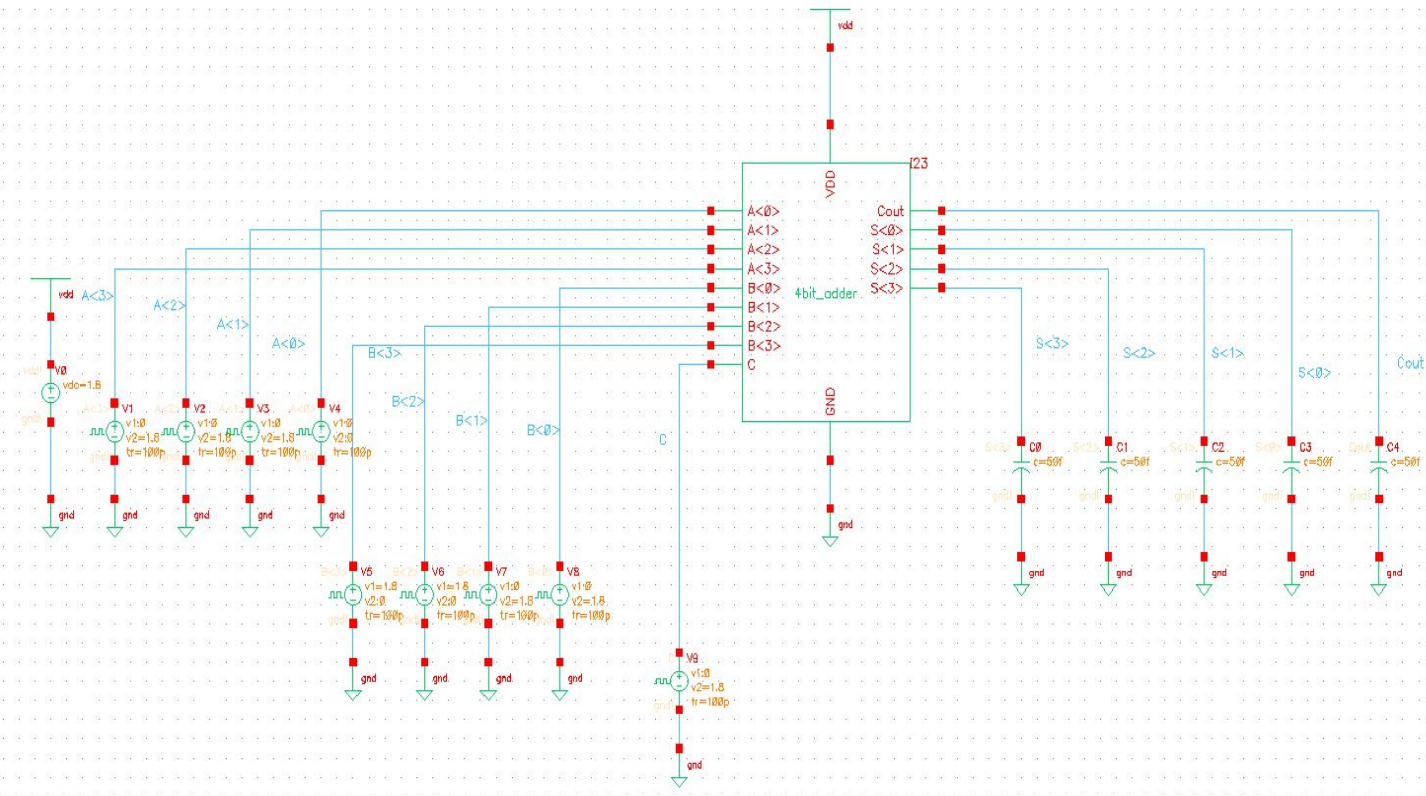
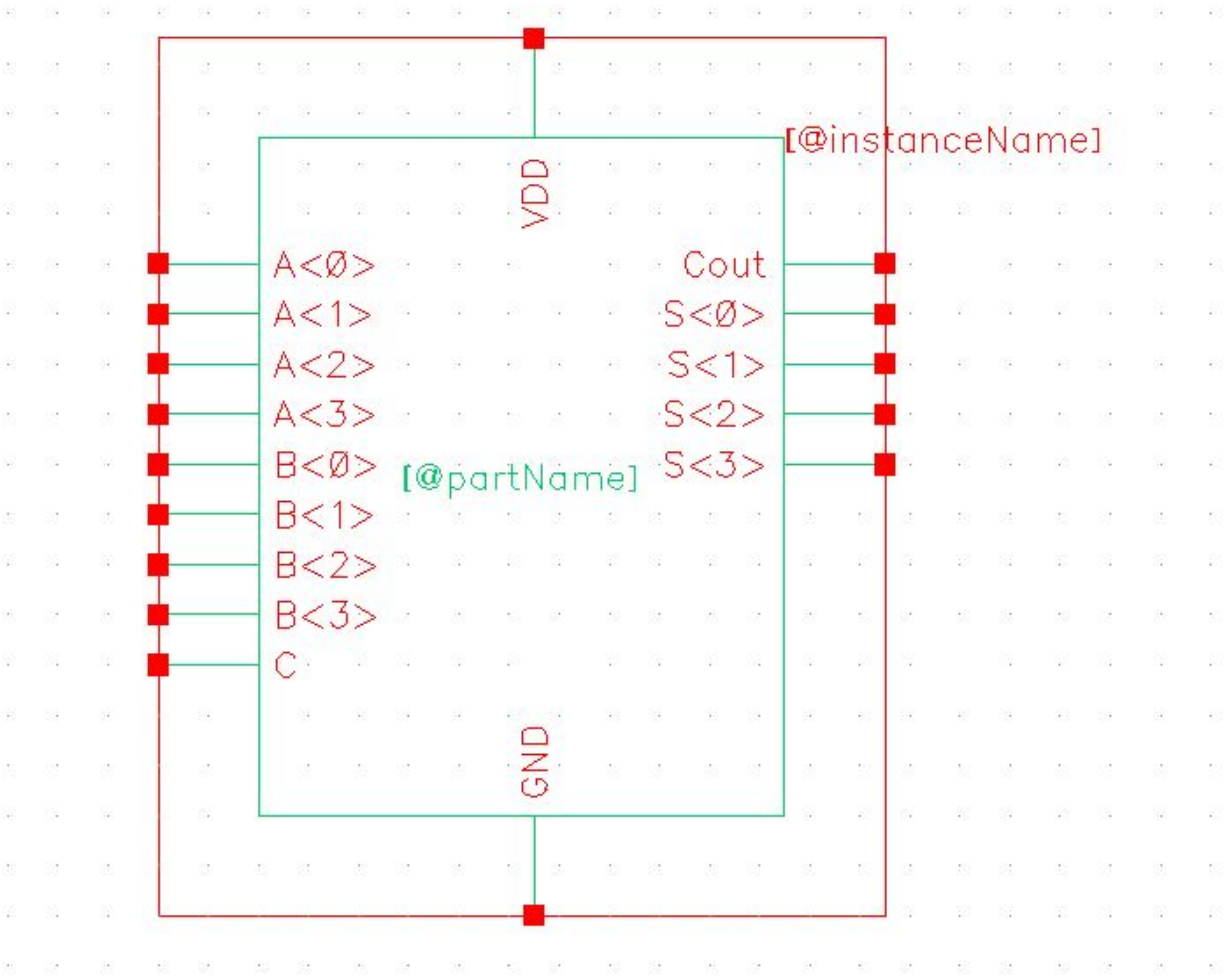
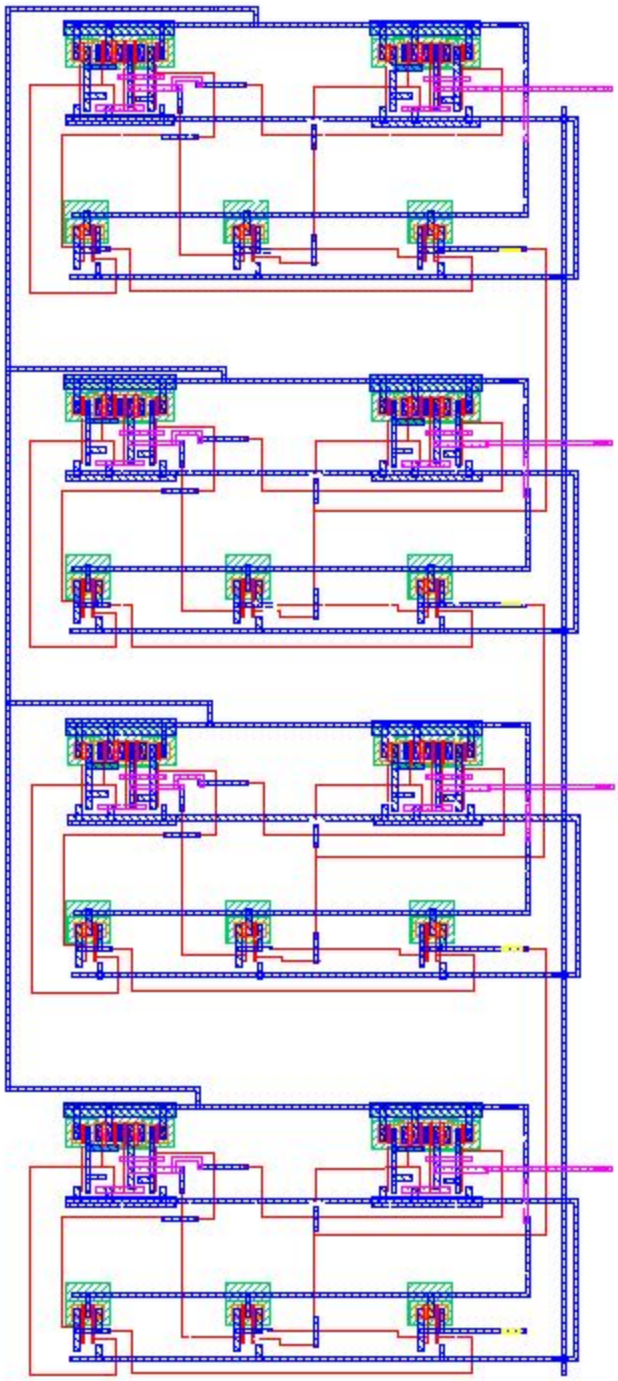
ECEN 454-508
Lab 5
Nicholas Tann
2/23/2020

4 Bit Adder:


VDD
A<3>
B<3>
C
I6
1bit_adder
Carry
Sum
S<3>
I7
S<2>
A<2>
B<2>
I8
S<1>
A<1>
B<1>
I9
Cout
A<0>
B<0>
GND


vdd
I23
4bit_adder
Cout
S<0>
S<1>
S<2>
S<3>
A<0>
A<1>
A<2>
A<3>
B<0>
B<1>
B<2>
B<3>
C
GND
V0
vdc=1.8
V1
V2
V3
V4
V5
V6
V7
V8
V9
C0
C1
C2
C3
C4
c=50f
gnd


[@instanceName]
VDD
A<Ø>
A<1>
A<2>
A<3>
B<Ø>
B<1>
B<2>
B<3>
C
[@partName]
Cout
S<Ø>
S<1>
S<2>
S<3>
GND



A=0000 B=1111 C = 1	S3	S2	S1	S0	C
Rising (ns)	1129	963.2	697.6	396.6	1196
Falling (ns)	1213	964.7	716.8	434.3	1288
Error (%)	6.92	.15	2.68	8.66	7.14

Vdd (V)	Iavg (uA)	Pavg (uW)
1.8	9.93	17.88

A=1010 B=0101 C = 0	S3	S2	S1	S0	C
Rising (ns)	1218	962.1	698.7	504.2	1196
Falling (ns)	1212	963.3	725.6	525.4	1287
Error (%)	.49	.12	3.85	4.20	7.61

Vdd (V)	Iavg (uA)	Pavg (uW)
1.8	21.35	38.43

A=1010 B=0101 C = 1	S3	S2	S1	S0	C
Rising (ns)	1228	961.9	696	500.4	1195
Falling (ns)	1212	963.7	715.6	545.4	1287
Error (%)	1.3	.19	2.74	8.25	7.14

Vdd (V)	Iavg (uA)	Pavg (uW)
1.8	21.49	38.68

A=1100 B=1000 C = 0	S3	S2	S1	S0	C
Rising (ns)	1009	767.6	676.7	565.7	434
Falling (ns)	1015	753	722.8	586.6	436.5
Error (%)	.59	1.9	6.38	3.73	.6

Vdd (V)	Iavg (uA)	Pavg (uW)
1.8	21.45	38.61

Net-list summary for /home/ugrads/n/ntann/ECEN454/Lab5/LVS/layout/netlist

count	
91	nets
16	terminals
72	pmos
72	nmos

Net-list summary for /home/ugrads/n/ntann/ECEN454/Lab5/LVS/schematic/netlist

count	
91	nets
16	terminals
72	pmos
72	nmos

Terminal correspondence points

N83	N9	A<0>
N80	N8	A<1>
N77	N7	A<2>
N75	N5	A<3>
N90	N18	B<0>
N88	N0	B<1>
N86	N12	B<2>
N85	N15	B<3>
N82	N2	C
N87	N3	Cout
N78	N13	GND
N84	N10	S<0>
N81	N14	S<1>
N79	N17	S<2>
N76	N11	S<3>
N89	N16	VDD

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	144	144
total	144	144
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	91	91
total	91	91
terminals		
un-matched	0	0
matched but different type	0	0
total	16	16

Probe files from /home/ugrads/n/ntann/ECEN454/Lab5/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/ugrads/n/ntann/ECEN454/Lab5/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

********* Summary of rule violations for cell "4bit_adder layout" *********
# errors Violated Rules
17 (SCMOS Rule 5.5.b) poly contact to poly spacing: 0.50 um
12 (SCMOS Rule 7.2) metal1 spacing: 0.30 um
13 (SCMOS_SUBM Rule 3.2) poly spacing: 0.30 um
4 (SCMOS_SUBM Rule 9.2.b) metal2 spacing: 0.30 um
46 Total errors found