

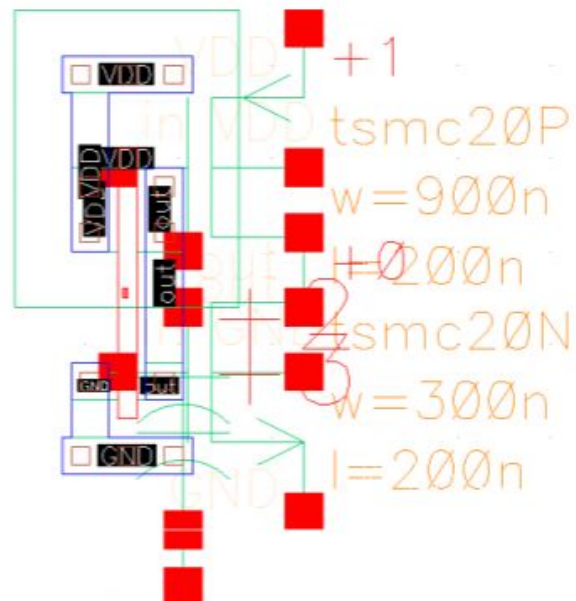
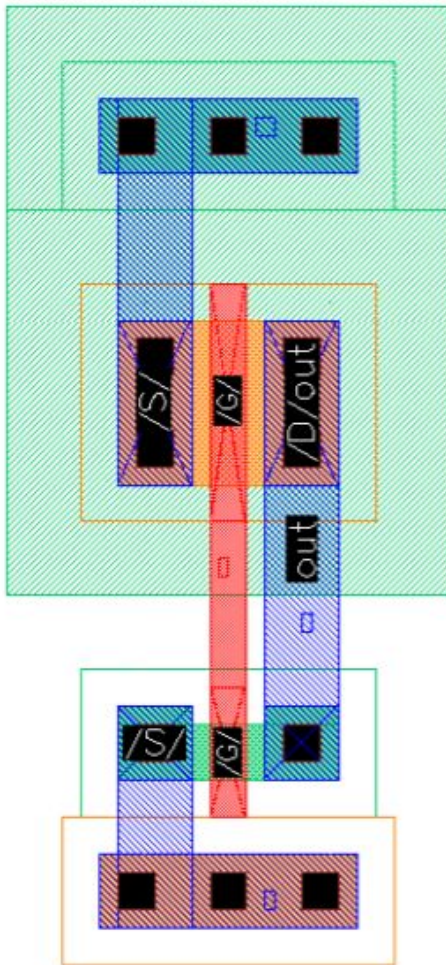
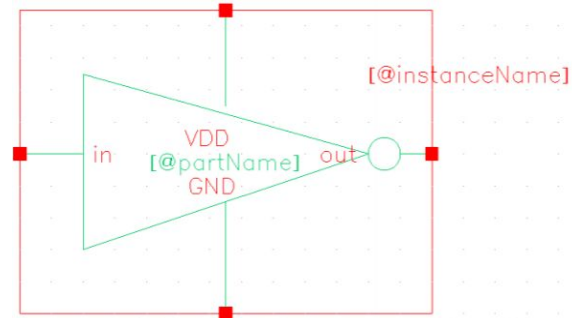
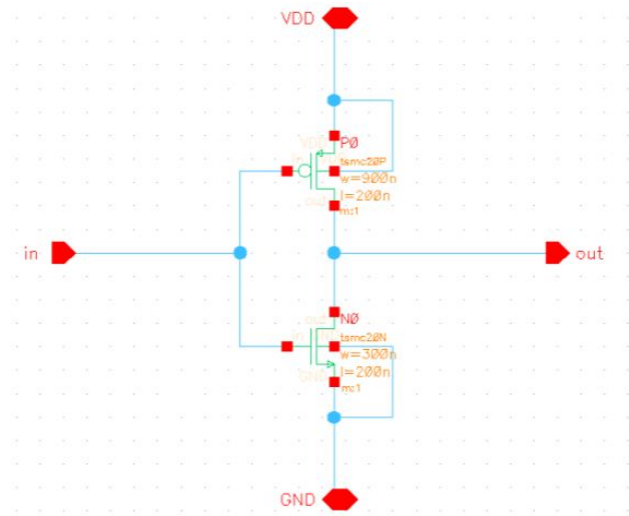
ECEN 454-508

Lab 2

Nicholas Tann

2/2/2020

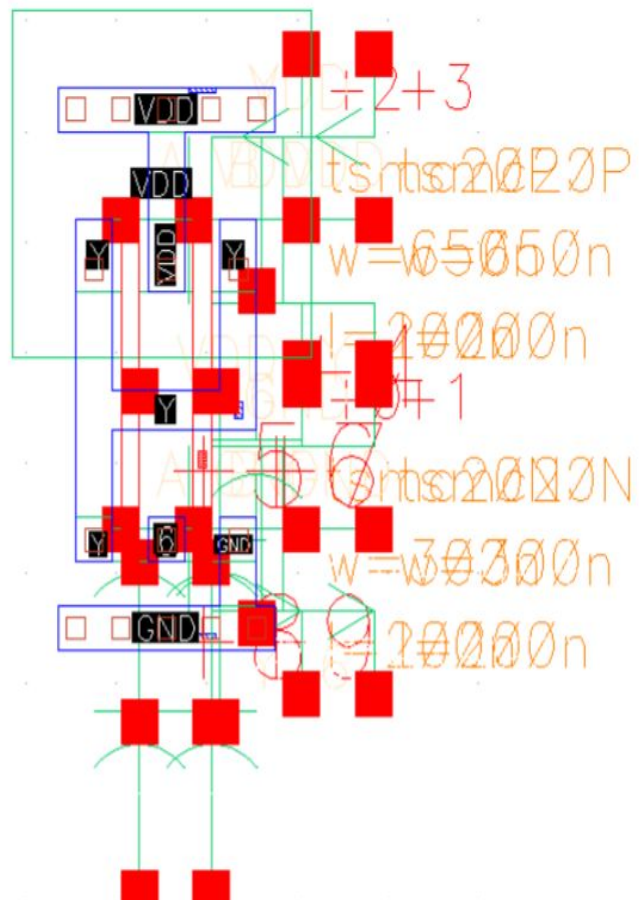
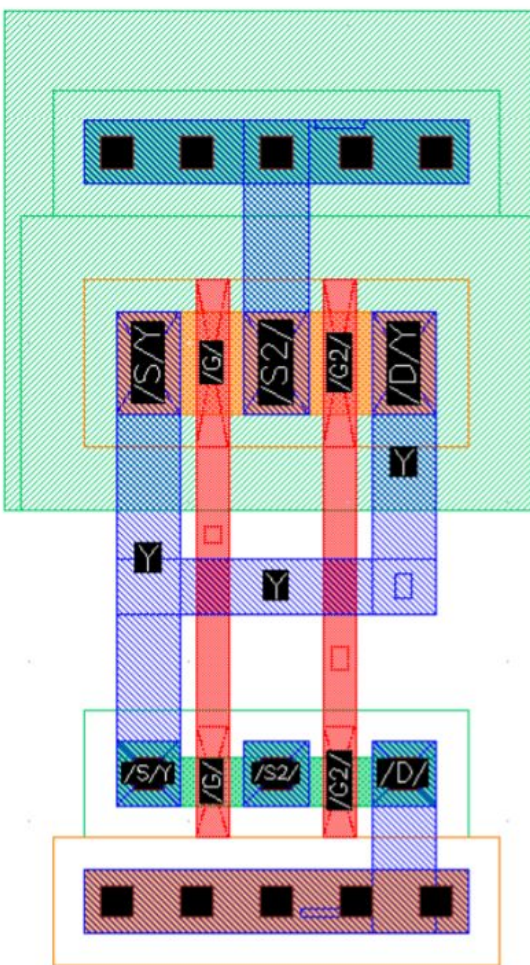
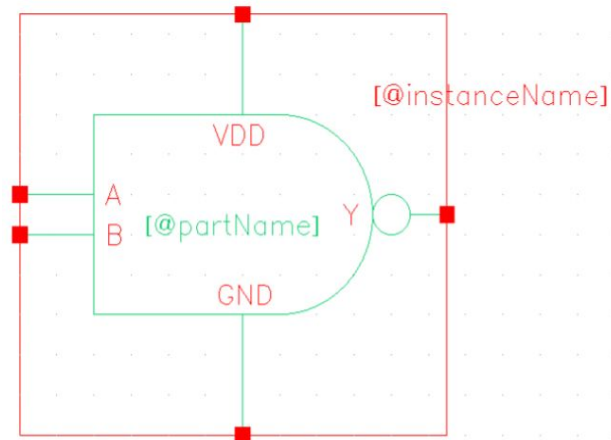
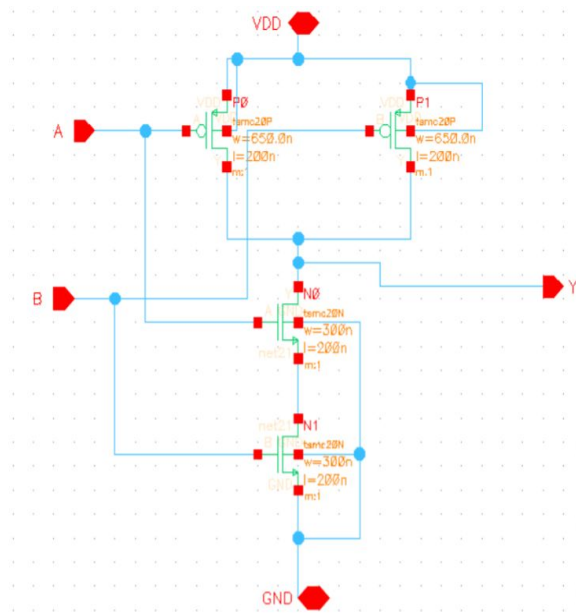
Inverter



LVS:

count 4 nets 4 terminals 1 pmos 1 nmos Terminal correspondence points N0 N1 GND N3 N0
VDD N2 N2 in N1 N3 out Devices in the netlist but not in the rules: pcapacitor Devices in the
rules but not in the netlist: cap nfet pfet nmos4 pmos4 The net-lists match. layout schematic
instances un-matched 0 0 rewired 0 0 size errors 0 0 pruned 0 0 active 2 2 total 2 2 nets
un-matched 0 0 merged 0 0 pruned 0 0 active 4 4 total 4 4 terminals un-matched 0 0 matched but
different type 0 0 total 4 4 Probe files
from/home/ugrads/a/ntann/ECEN454/Lab1/LVS/schematic devbad.out: netbad.out:
mergenet.out: termbad.out: prunenet.out: prunedev.out: audit.out: Probe files from
/home/ugrads/a/ntann/ECEN454/Lab1/LVS/layout devbad.out: netbad.out: mergenet.out:
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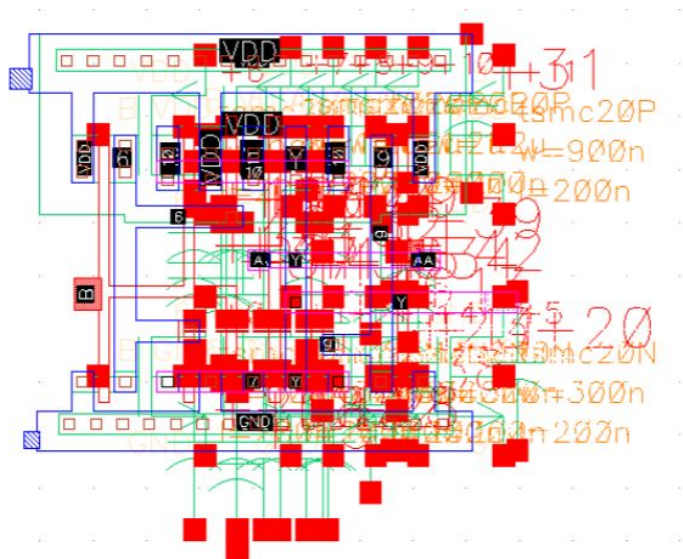
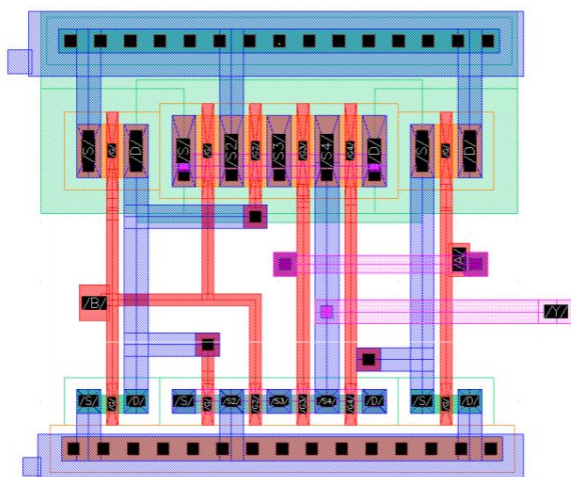
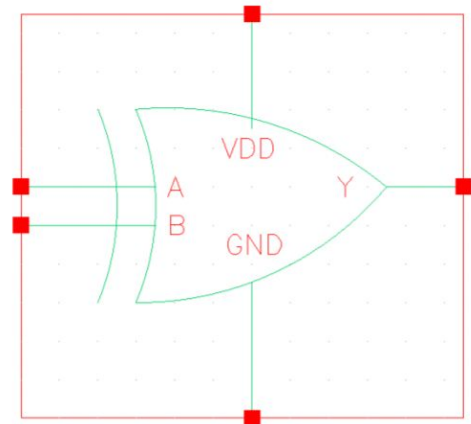
NAND



LVS:

count 6 nets 5 terminals 2 pmos 2 nmos Terminal correspondence points N4 N4 A N3 N5 B N2
N1 GND N5 N0 VDD N1 N2 Y Devices in the netlist but not in the rules: pcapacitor Devices in
the rules but not in the netlist: cap nfet pfet nmos4 pmos4 The net-lists match. layout schematic
instances un-matched 0 0 rewired 0 0 size errors 0 0 pruned 0 0 active 4 4 total 4 4 nets
un-matched 0 0 merged 0 0 pruned 0 0 active 6 6 total 6 6 terminals un-matched 0 0 matched but
different type 0 0 total 5 5 Probe files from
/home/ugrads/a/ntann/ECEN454/Lab1/LVS/schematic devbad.out: netbad.out: mergenet.out:
termbad.out: prunenet.out: prunedev.out: audit.out: Probe files from
/home/ugrads/a/ntann/ECEN454/Lab1/LVS/layout devbad.out: netbad.out: mergenet.out:
termbad.out: prunenet.out: prunedev.out: audit.out:

XOR



LVS:

count 11 nets 5 terminals 6 pmos 6 nmos Terminal correspondence points N9 N3 A N8 N10 B
N7 N7 GND N10 N8 VDD N6 N5 Y Devices in the netlist but not in the rules: pcapacitor
Devices in the rules but not in the netlist: cap nfet pfet nmos4 pmos4 The net-lists match. layout
schematic instances un-matched 0 0 rewired 0 0 size errors 0 0 pruned 0 0 active 12 12 total 12
12 nets un-matched 0 0 merged 0 0 pruned 0 0 active 11 11 total 11 11 terminals un-matched 0 0
matched but different type 0 0 total 5 5 Probe files from
/home/ugrads/a/ntann/ECEN454/Lab1/LVS/schematic devbad.out: netbad.out: mergenet.out:
termbad.out: prunenet.out: prunedev.out: audit.out: Probe files from
/home/ugrads/a/ntann/ECEN454/Lab1/LVS/layout devbad.out: netbad.out: mergenet.out:
termbad.out: prunenet.out: prunedev.out: audit.out: