ECEN 454-508
Lab 7
Nicholas Tann
3/24/2020

Purpose:

Understand the basics of synthesis using Design Vision through a simple example "cruise control design". This includes pre-layout static timing analysis of the synthesized design, defining design constraints and timing of all the paths in the design. Finally, the synthesized Verilog netlist generated for the cruise control logic will be placed and routed on a circuit on a die.

Procedure:

1. pre-layout static timing analysis of the synthesized design
2. defining design constraints
3. timing of all the paths in the design
4. synthesized Verilog netlist placed and routed on a circuit on a die

Results:

Complete results which includes:

- cruise control logic
- register_count
- Verilog netlist
- Max_paths.txt
- Min_paths.txt
- Innovus.txt
- results

Are attached in .zip file