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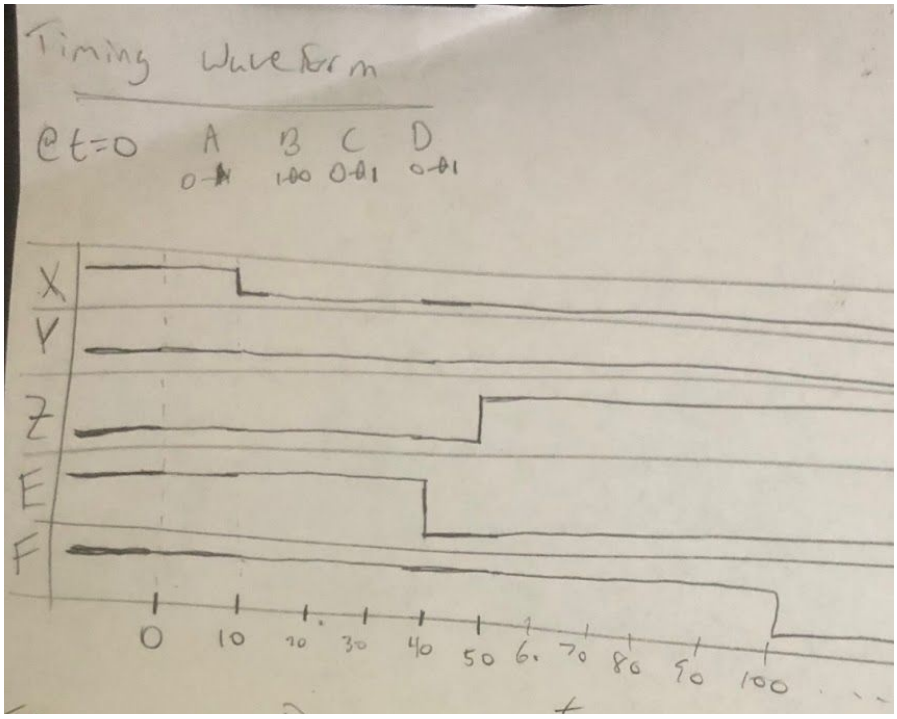
HW 1

ECEN 449-503

2/9/2020

Problem #1:

Waveform



Structural Verilog

```
module QOneStructural (input A, input B, input C, input D,
                       output E, output F              );
    wire X, Y, Z;
//explicitly creating the gates by initiating them as their names from the diagram, io corresponds to io from diagram
    not not2 (X, A);
```

```
        and and2 (Y, A, B);

        or or2 (Z, Y, C);

        or or1 (E, X, Z);

        nand nand2 (F, Z, D);

endmodule
```

Data Flow Verilog

```
module QOneDataflow (input A, input B, input C, input D,
                output E, output F                );


        wire X, Y, Z;


        assign X = ~A; //output of NOT2

        assign Y = A & B; //output of AND2

        assign Z = Y | C;  //output of OR2

        assign E = X | Z; //output of OR1
```

```
        assign F = Z ~& D; //output NAND2


endmodule
```

Behavioral Verilog

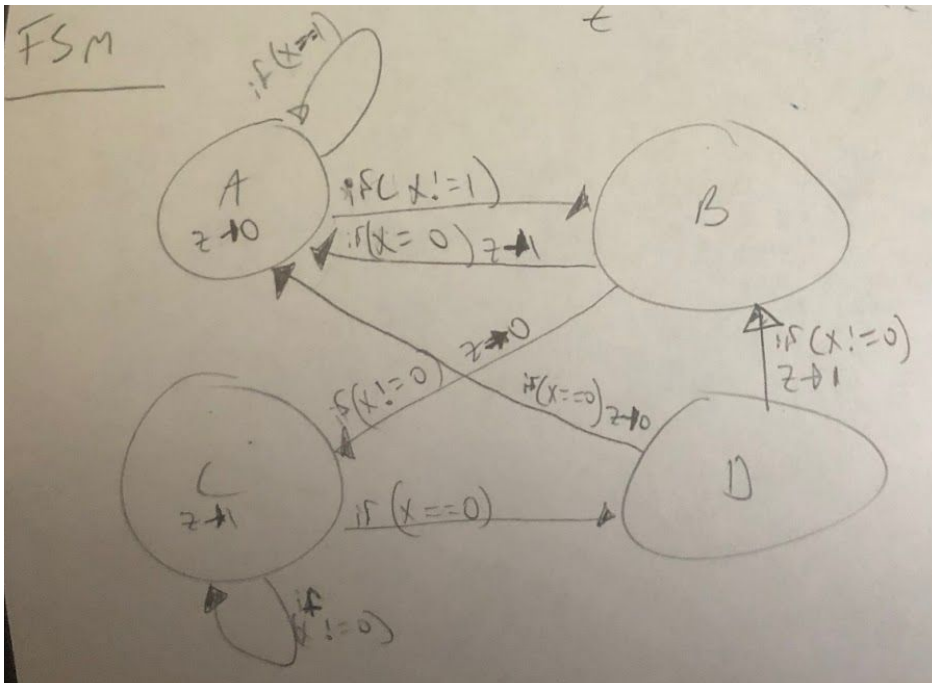
```
module QOneBehavioral (input A, input B, input C, input D,
                       output E, output F               );


        reg E, F;


        always @(A or B or C or D)
                //boolean algebra output for E given A,B,C,D
                if (A == 0) E = 1;
                else if (C == 1) E = 1;
                else if (B == 1) E = 1;
                else E = 0;
```

```
        //boolean algebra output for F given A,B,C,D
        if (D == 0) F = 1;
        else if (A == 0) begin
            if (C == 0) F = 1;
            else F = 0;
        end
        else if (B == 0) begin
            if (C == 0) F = 1;
            else F = 0;
        end
        else F = 0;
    end
endmodule
```

FSM


FSM
A
z=0
B
C
z=1
D
if(x==1)
if(x!=1)
if(x==0) z=1
if(x!=0) z=0
if(x==0) z=0
if(x!=0) z=1
if(x==0)
if(x!=0)