

ECEN 454-508

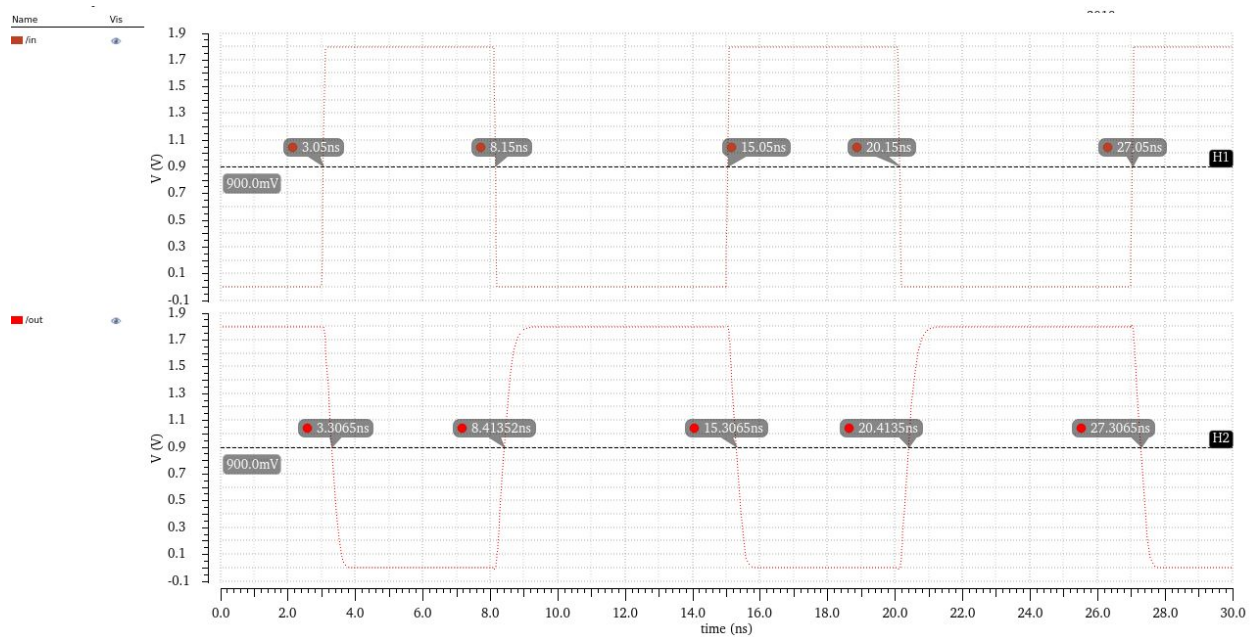
Lab 4

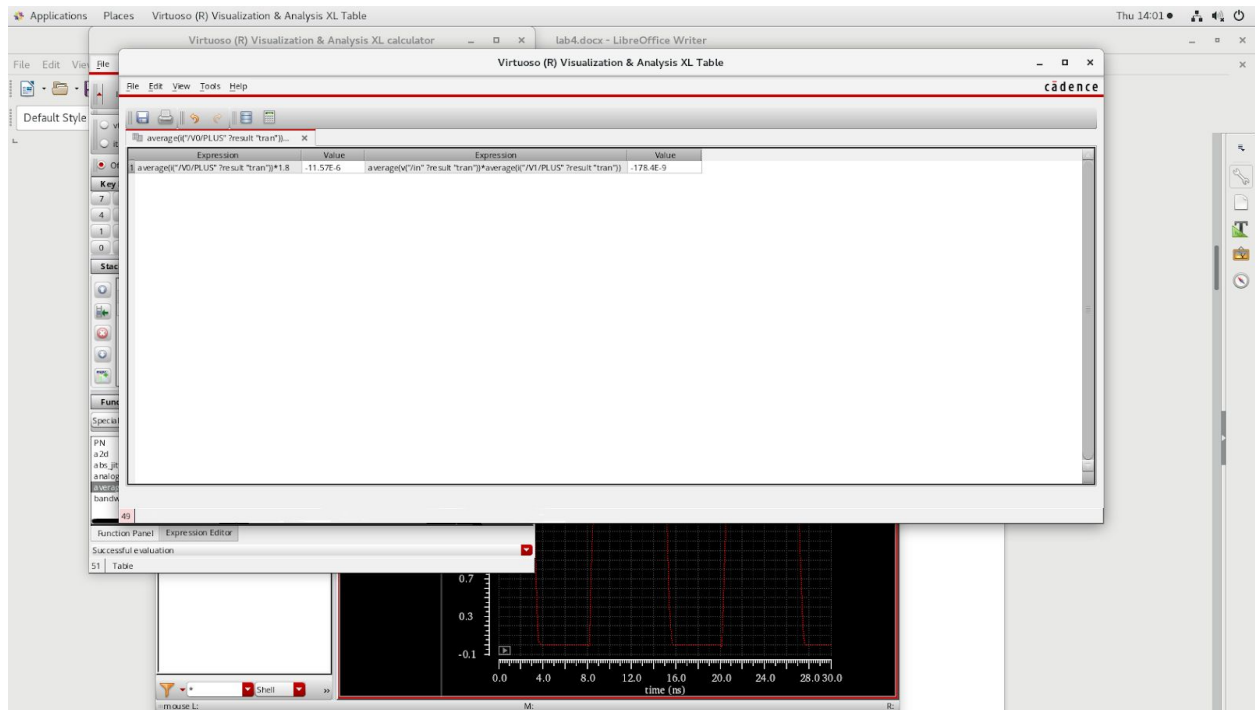
Nicholas Tann

2/16/2020

Inverter:

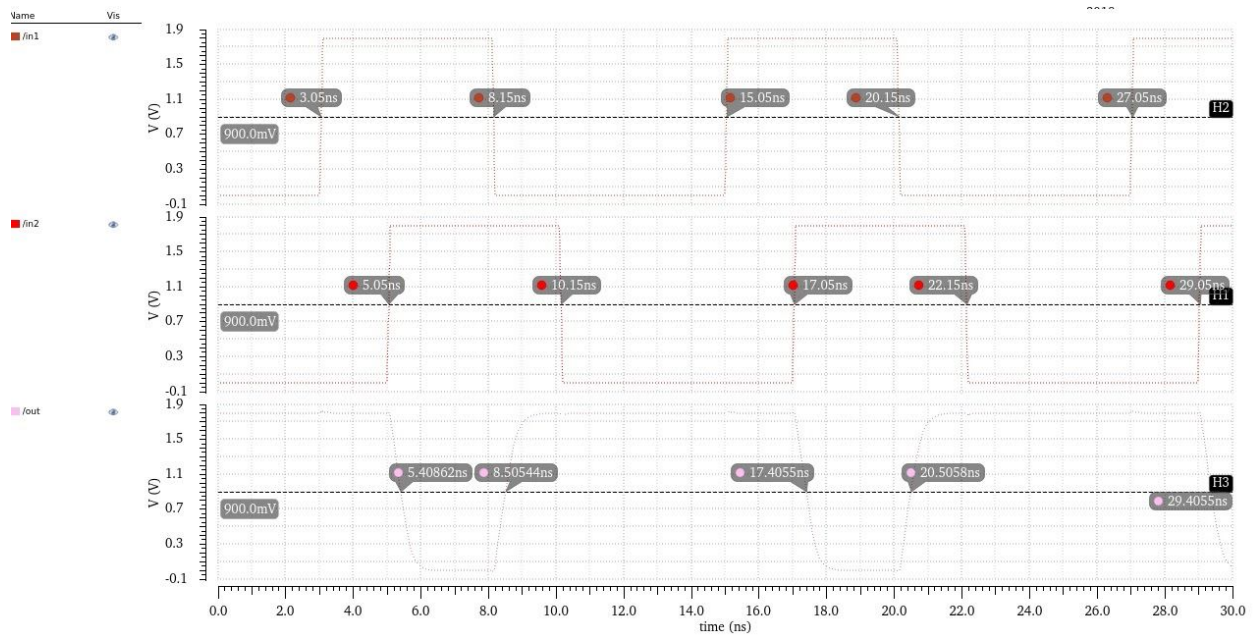
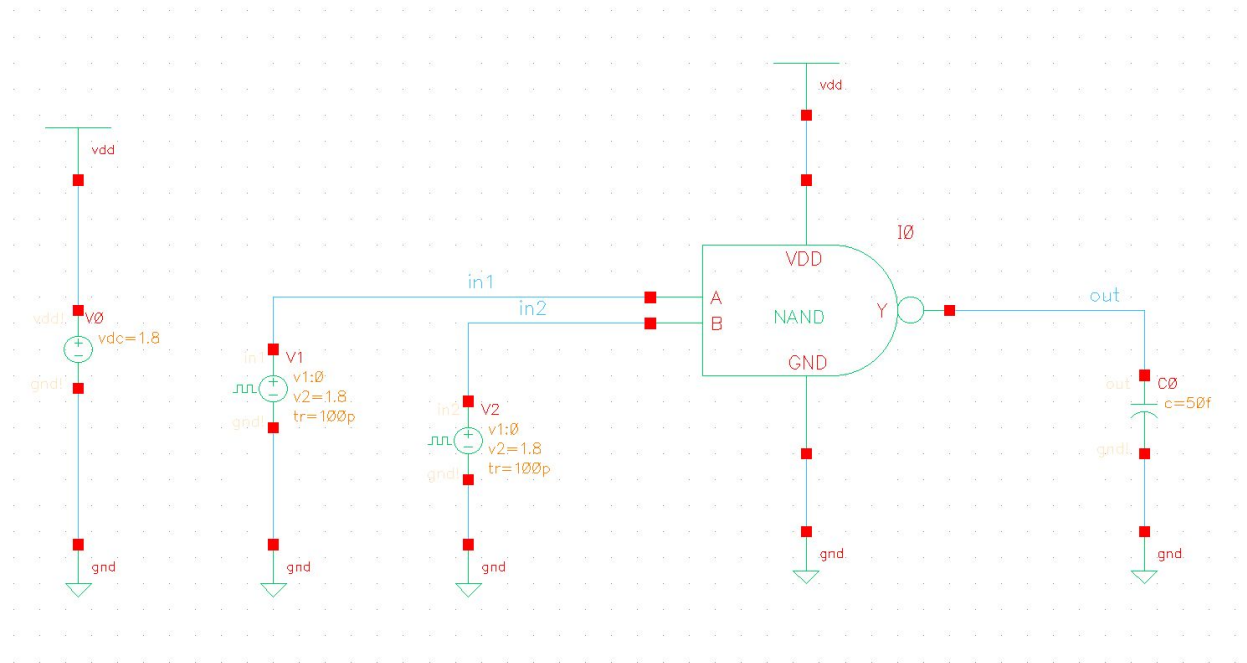
Rising Delay	Falling Delay	Difference	% of rising	% of falling
481	498	17	3.53	3.41





NAND:

Rising Delay	Falling Delay	Difference	% of rising	% of falling
487	505	18	3.70	3.56



Applications Places Virtuoso (R) Visualization & Analysis XL Table Thu 13:36

Virtuoso (R) Visualization & Analysis XL Table

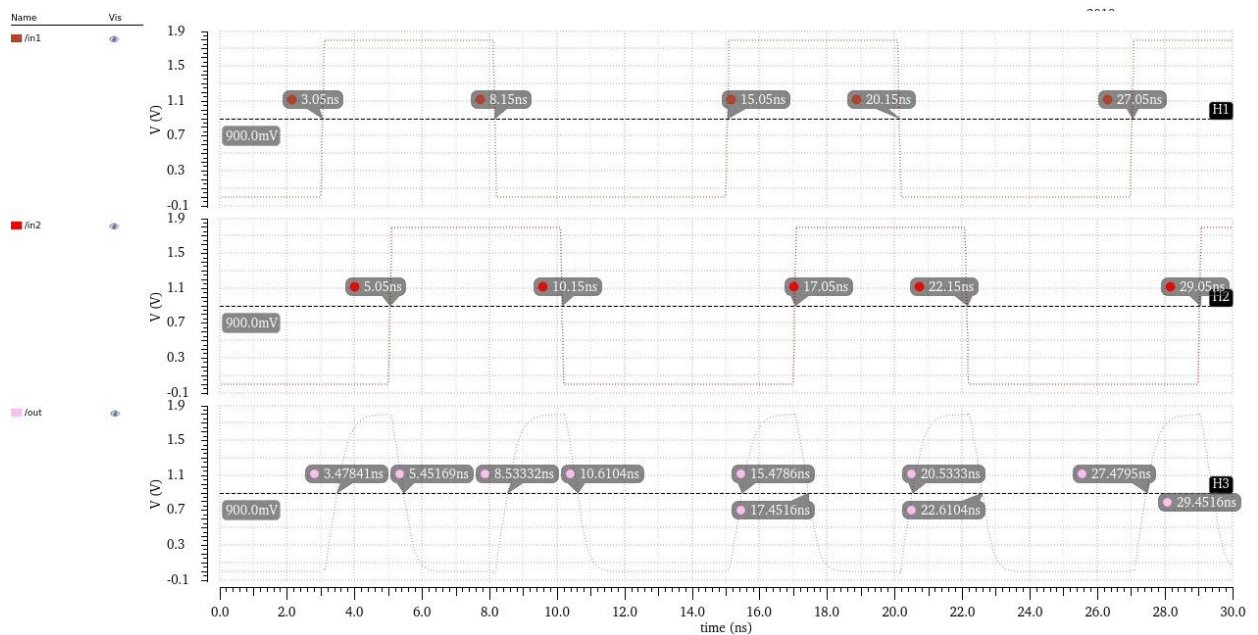
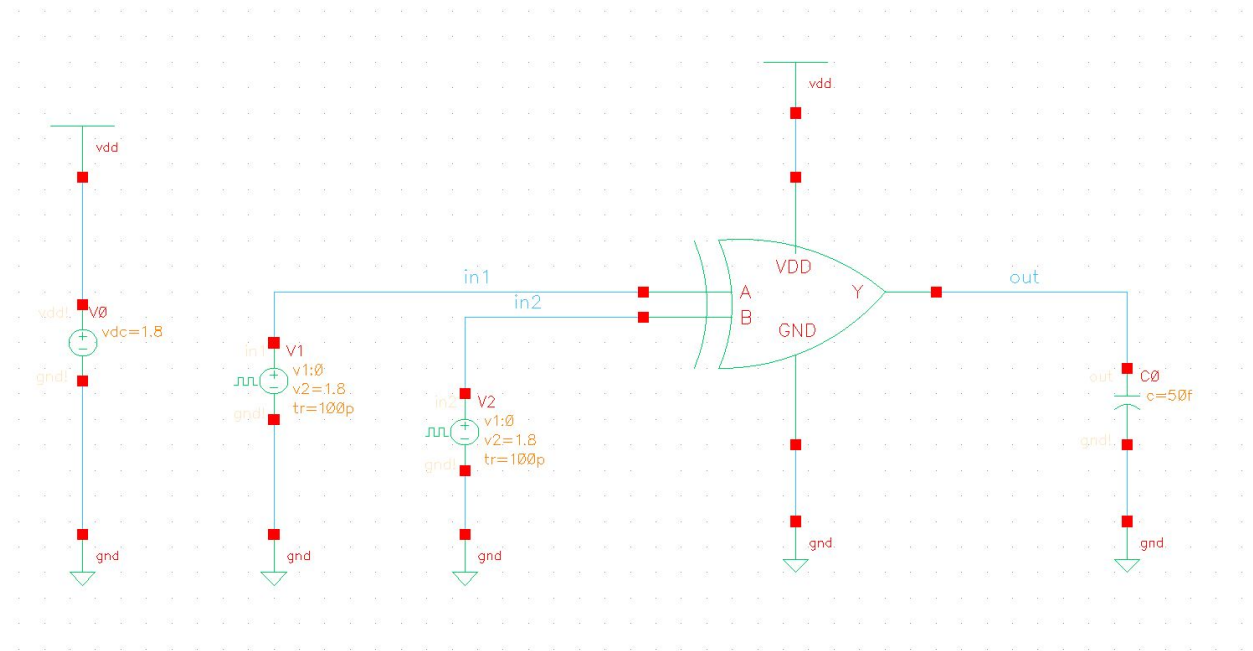
File Edit View Tools Help

cadence

Expression	Value	Expression	Value	Expression	Value
average(v("V0PLUS" result "tran"))	-11.78E-6	average(v("in1" result "tran")Paverage(v("V1PLUS" result "tran"))	-157.9E-9	average(v("in2" result "tran")Paverage(v("in1" result "tran"))	527.8E-3

XOR:

Rising Delay	Falling Delay	Difference	% of rising	% of falling
658	649	9	1.37	1.39



Applications Places Virtuoso (R) Visualization & Analysis XL Thu 14:14

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

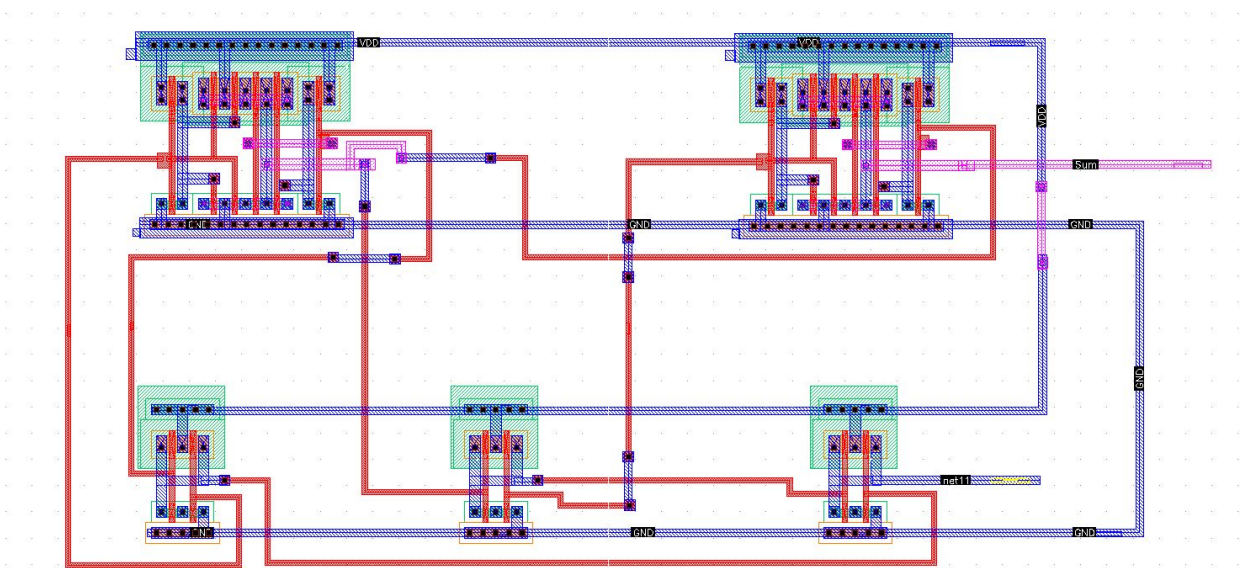
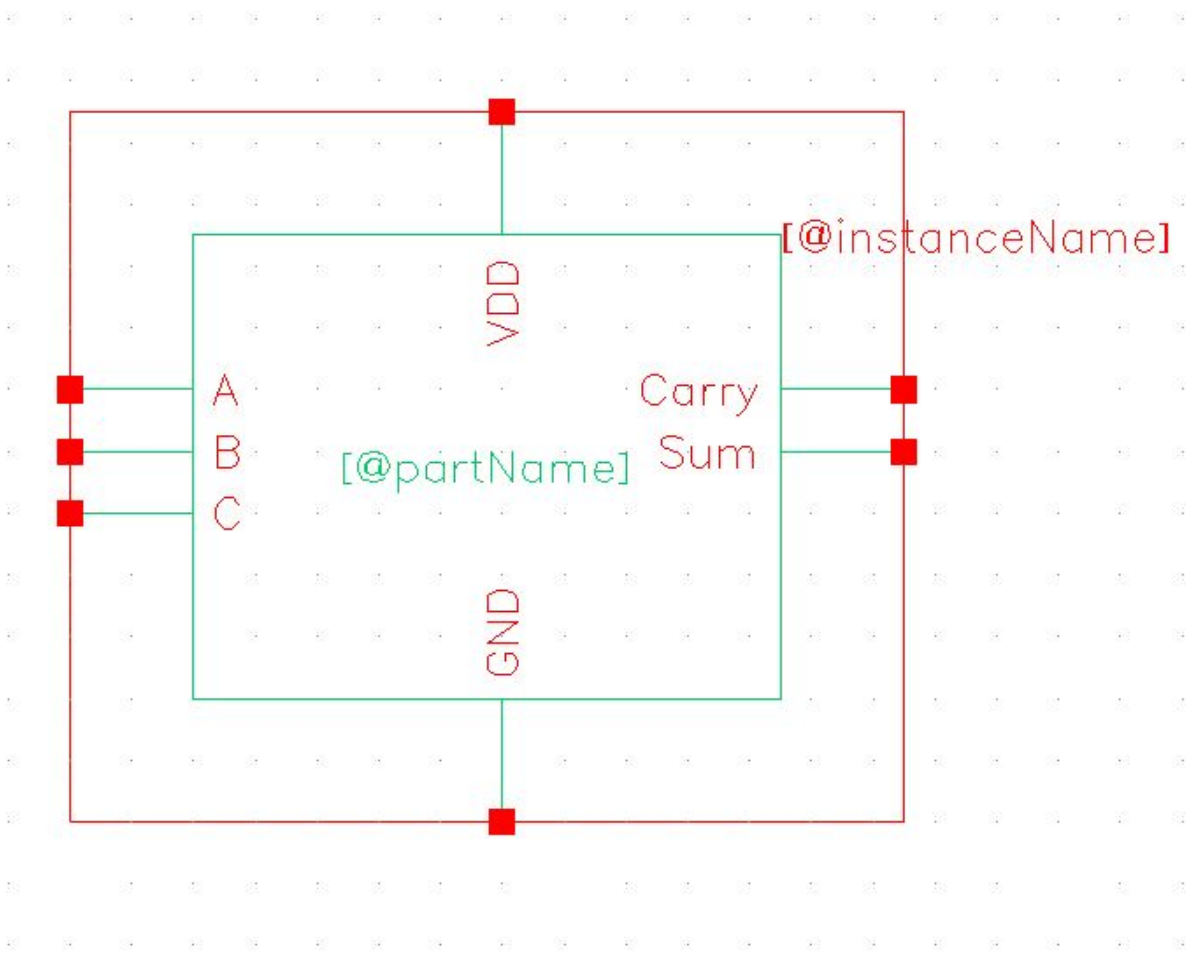
cadence

Expression	Value	Expression	Value	Expression	Value
average(v("V0PLUS" result "tran"))	-35.688-6	average(v("in1" result "tran"))	average(v("V1PLUS" result "tran"))	average(v("in2" result "tran"))	average(v("out" result "tran"))
average(v("V0PLUS" result "tran"))*1.8	-35.688-6	average(v("in1" result "tran"))	-340.88-9	average(v("in2" result "tran"))	5.27.88-3

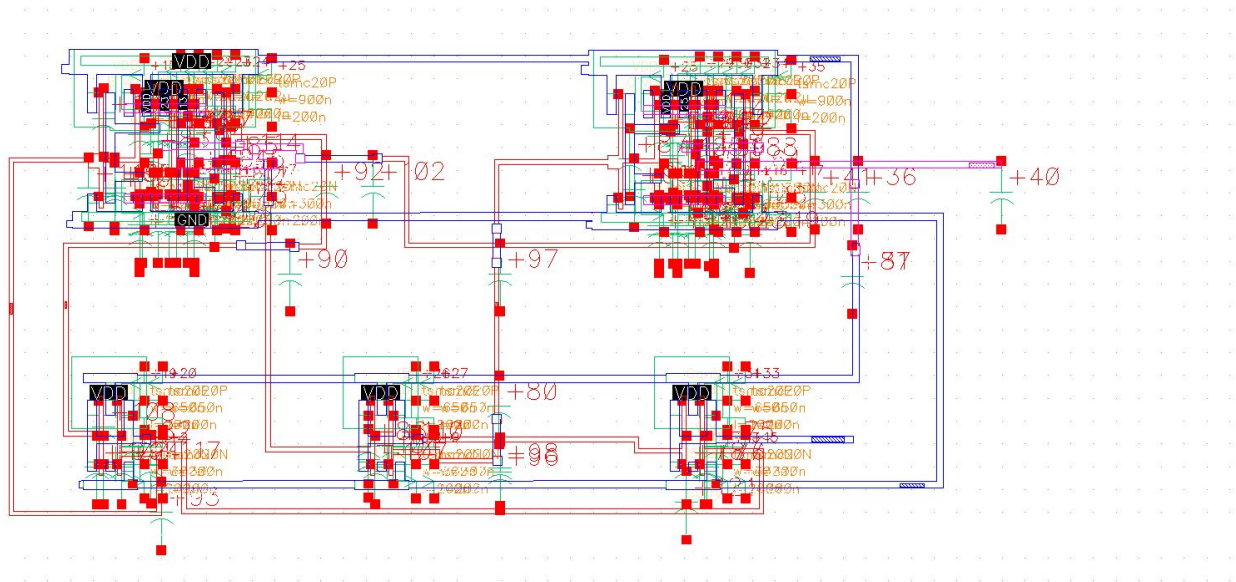
1 Bit Adder:











As the pulse width was decreased on Cin the SUM output peak increased more and more rapidly until it maxed out at 1.8 Volts at 1.6ns

	Inverter	NAND	XOR	Adder
Ia	-320.5nA	-181.7nA	-554.6nA	17.83nA
Va	789mV	789mV	789mV	867.8mV
Pa	-181.9nW	143.4nW	437.6nW	15.47nW
Ib		-198.1nA	-431.7nA	13.14nA
Vb		783mV	783mV	727.7mV
Pb		155.1nW	338nW	9.56nW
Ic				-6.24nA
Vc				734.4mV
Pc				-4.58nW