

# The electronic interface for quantum processors

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## ABSTRACT

Quantum computers can potentially provide an unprecedented speed-up with respect to traditional computers. However, a significant increase in the number of quantum bits (qubits) and their performance is required to demonstrate such *quantum supremacy*. While scaling up the underlying quantum processor is just as relevant and arduous. This paper discusses the challenges in designing a scalable electronic interface for quantum processors. To that end, we discuss the requirements dictated by different qubit technologies and present existing implementations of the electronic interface. The limitations in scaling up such state-of-the-art implementations are analyzed, and possible solutions to overcome those hurdles are reviewed. The benefits offered by operating the electronic interface at cryogenic temperatures in close proximity to the low-temperature qubits are discussed. Although several significant challenges must still be faced by researchers in the field of cryogenic control for quantum processors, a cryogenic electronic interface appears the viable solution to enable large-scale quantum computers able to address world-changing computational problems.

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## 1. Introduction

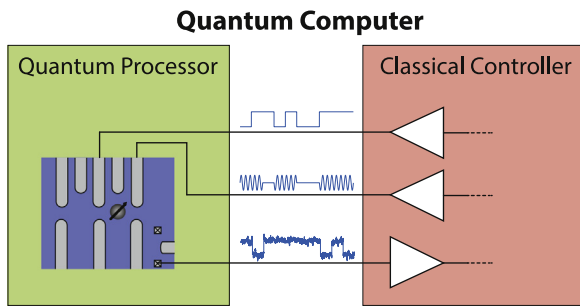
Quantum computers hold the promise to ignite the next technological revolution as the classical computer did for last century's digital revolution, both by efficiently solving problems that are intractable even for today's supercomputers, such as simulation of quantum systems, and by accelerating classical applications. For instance, by enabling the efficient simulation of quantum systems, quantum computing could help in synthesizing a room-temperature superconductor, which would significantly reduce energy loss in power lines, generators, and supercomputers [1]. It could also contribute to improving the efficiency of industrial nitrogen fixation into fertilizers, which is currently achieved through the 117-year-old Haber process and uses up to 5% of the natural gas produced each year worldwide [2,3]. Furthermore, quantum computers have the potential to solve classical problems with much higher efficiency, such as searching in huge datasets, solving large linear systems, and even addressing privacy concerns by running algorithms without the operator being able to detect what is

being computed [1]. The ability to solve currently intractable problems and significantly accelerate certain computations represents a game changer with the potential to revolutionize entire industries.

To achieve such tremendous progress, a quantum computer relies on processing the information stored in quantum bits (qubits) that must be typically cooled at cryogenic temperatures in dilution refrigerators for proper operation. Nevertheless, a quantum computer is more than only a quantum processor hosting several qubits, since all operations must be controlled by a classical (i.e. non-quantum) electronic interface, as shown in Fig. 1. Today, such an electronic interface can be implemented by off-the-shelf electronic components and instrumentation, as state-of-the-art quantum processors comprise only a few qubits (less than 20 [7–9]), thus showing very limited complexity in the number of subsystems. However, quantum processors comprising thousands or even millions of qubits will be required to address any of the practical computing problems mentioned before [10]. Although building such a large-scale quantum processor is a daunting task by itself, realizing a large-scale electronic infrastructure to handle a very large number of qubits is also a formidable challenge. Due to the limited size of existing quantum processors, the electronic interface is not yet the main limitation in the performance of quantum computers, but it could become a major bottleneck in

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**Fig. 1.** A quantum computer comprises a quantum processor and a classical electronic controller that generates and processes the various signals.

the near future, as both the performance and the complexity of quantum processors advance.

To address this challenge, this paper presents the obstacles to be faced when scaling up a quantum computer, with specific focus on the electronic interface connecting to the quantum processor. Section 2 discusses the requirements of such electronics when employed in combination with processors adopting different qubit technologies. Since we focus on the need for large-scale quantum computation, the scope will be limited to the qubit technologies that today promise large-scale integration, i.e. solid-state qubits requiring only purely electrical control, such as spin qubits and superconducting qubits. An overview on how the requirements dictated by the quantum processor are handled by state-of-the-art electronic controllers is given in Section 3. Then, the challenges in scaling up the existing controllers and possible approaches to tackle them will be treated in Sections 4 and 5, respectively. Conclusions are drawn in Section 6.

## 2. Quantum processor requirements

DiVincenzo defined five criteria that a quantum processor must satisfy to be employed in a quantum computer [11]. In short, the quantum processor must be scalable and contain well characterized qubits (I) that can be initialized (II) and can preserve their quantum state for a time<sup>1</sup> ( $T_2^*$ ) sufficiently longer than the duration of a quantum operation (III). Finally, it must be possible to operate on the qubits with a universal set of quantum gates, i.e. both single-qubit and two-qubit operations, (IV), and to read out the state of a qubit (V).

This section will give a brief overview of the implementation of the read-out, the single-qubit and the two-qubit gates in different quantum technologies, and the implications for the electronic controller. As the state of a qubit can be represented geometrically as a point on a sphere and single-qubit operations correspond to rotations along this sphere, these operations will also be referred to (here and in the literature) as rotations in the following<sup>2</sup>. Specific attention will be devoted to assess the performance of each technology in terms of coherence time, and to analyze their potentials and hurdles for scalability. The technologies under consideration are superconducting qubits (Fig. 2a [4,5]), specifically transmons, and spin qubits in semiconductors (Fig. 2b [6]), specifically single-electron spin-qubits (in quantum dots or bound to donors) and multiple-electron qubits, such as singlet-triplet qubits, exchange-only qubits and hybrid qubits. Typical values and control methods as used in current experiments are reported, but these may shift in the future as the various quantum technologies develop.

<sup>1</sup> The coherence time is the characteristic time constant of the process of a qubit losing its relevant quantum behavior due to unwanted interactions with the environment.

<sup>2</sup> To satisfy DiVincenzo's criteria, it is in general sufficient to be able to rotate the qubit state around two axis, typically the  $X$  and  $Z$  axis.

### 2.1. Superconducting qubits

Various superconducting-qubit implementations have been proposed based on encoding the quantum information in the charge, phase or flux state of a superconducting resonator. However, the research community has generally converged to the adoption of the *transmon*, a superconducting charge qubit with reduced sensitivity to charge noise, leading to improved coherence times [12–18], e.g.  $T_2^* - 18.7 \mu\text{s}$  [18].

In a transmon, the qubit states are defined as the two lowest energy levels of a non-linear resonator implemented using Josephson junctions in a loop shunted by a capacitor (Fig. 2a). The magnetic flux coupled to the loop of Josephson junctions can be controlled by means of a current, called the flux bias, running in close proximity. This allows for the qubit energy levels, and hence the qubit frequency, to be tuned externally. To allow for rapid changes of the qubit frequency, the flux-bias lines are typically implemented as transmission lines with short-circuit termination.

Transmons can be fabricated as integrated circuits by depositing and patterning a superconducting film and integrating Josephson junctions on a solid-state substrate, typically made out of silicon or sapphire. Control and read-out is performed by coupling the qubit to microwave cavities on the same chip. Single-qubit rotations that flip the qubit state ( $X$ -rotation) can be obtained by applying a microwave pulse with frequency matching the qubit resonance, typically in the 4–6 GHz range [14,17]. Microwave pulses with Gaussian envelopes and in/quadrature-phase (I/Q) modulation adopting the Derivative Reduction by Adiabatic Gate (DRAG) approach [19] are used to minimize leakage to higher energy states of the resonator. Typical parameters for the Gaussian envelope of the in-phase component are a 5-ns  $\sigma$  and 20-ns total duration for a  $\pi$ -rotation [17]. As an alternative to a  $Z$ -rotation in software [20], a single-qubit rotation around the  $Z$ -axis can be obtained by temporarily detuning the qubit frequency by adapting the flux bias [13].

A two-qubit gate can be obtained between two qubits coupled to the same microwave cavity. The cavity is off-resonance with both qubits during normal operation, but, by detuning the qubit frequencies via their flux biases, the cavity can couple to the qubits by virtual photon exchange [13]. In this way, by applying proper pulses to the flux-bias lines of the two qubits, either a SWAP gate or a CPHASE gate can be implemented, depending on whether the flux bias is pulsed suddenly (typ. 12 ns [17]) or fast but adiabatically (typ. 40 ns [13,14,17]), respectively. Alternatively, a microwave-controlled two-qubit CPHASE gate can be engineered [21,22].

The qubit state is read out by probing the frequency response of a microwave cavity coupled to the qubit. A frequency shift of the cavity resonance frequency dependent on the qubit state can be observed in the measurement of the transmission coefficient of the cavity. The microwave excitation used for the measurement has a typical frequency in the range of 7–8 GHz with a duration of  $\sim 1 \mu\text{s}$  [17].

Superconducting qubits can be reliably fabricated nowadays, having led to quantum processors containing up to 72 qubits [23]. However, the individual qubits are currently very large (in the order of 0.1–1 mm<sup>2</sup> per qubit), which will hinder further scaling to thousands and millions of qubits per quantum processor. Furthermore, superconducting qubits have to operate at extremely low temperatures (typically < 100 mK).

### 2.2. Single-electron semiconductor qubits

Semiconductor qubits are significantly smaller than transmons, with a typical pitch between neighbouring qubits in the order of 100 nm, therefore representing promising candidates for large-scale

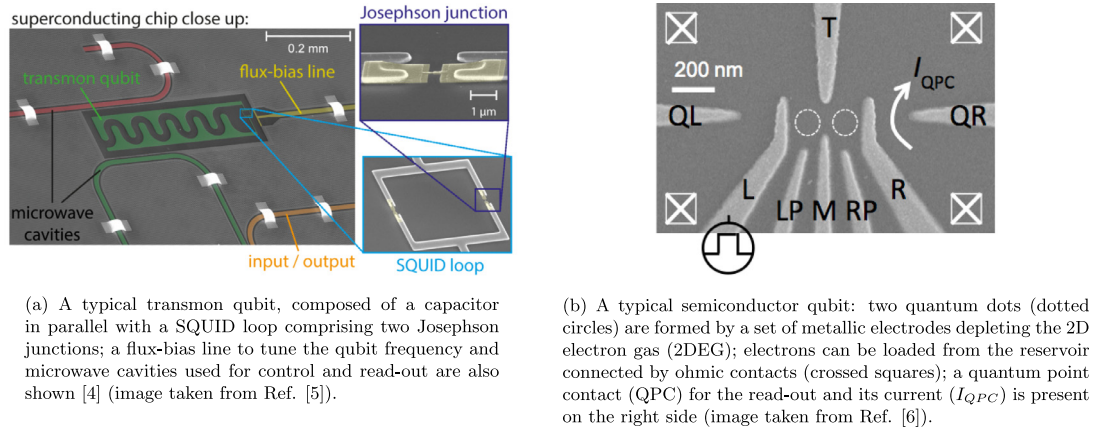


Fig. 2. Pictures of the actual quantum processor chips in different solid-state quantum technologies.

quantum processors. As charge qubits in semiconductors show poor coherence times due to their sensitivity to charge noise, most research is currently focused on spin qubits, in which the quantum state is encoded in the spin of one or more particles, such as nuclei and electrons, trapped in a specific location in a semiconductor solid-state substrate. A large magnetic field in the order of one Tesla is required to obtain a sufficiently large energy difference between the spin-up and spin-down states. The energy splitting between those two states determines the resonant frequency of the qubit. While such a magnetic field can be relatively easily generated and applied, it becomes challenging when a field gradient is desired over many qubits on the same chip to create addressability [24,25]. The decoherence of spin qubits is typically limited by the interaction with nuclear spins of all the other atoms in the substrate, which in turn can be minimized by using isotopically purified silicon [26]. As a major advantage, semiconductor qubits can be fabricated using industry-standard CMOS fabrication processes [27], thus leveraging the very-large-scale of integration (VLSI) and the yield and the reproducibility of the semiconductor industry. An additional advantage is that they can potentially be operated at higher temperatures, up to 4 K, although this has not yet been demonstrated [28,29]. However, the required small qubit pitch poses a challenge in routing all control lines individually.

The simplest spin qubit uses the spin of a single electron trapped in a quantum dot [24–26,30,31] with the qubit states encoded in the spin-up and spin-down states, as initially proposed by Loss and DiVincenzo [32]. A quantum dot hosting single electrons can be created by a set of gate electrodes locally forming an island in a 2-dimensional electron gas (2DEG), as shown in Fig. 2b. Coherence times of  $T_2^* = 1 \mu\text{s}$  [25] and  $T_2^* = 120 \mu\text{s}$  [26] can be achieved in natural silicon and isotopically purified silicon, respectively.

Single-qubit rotations across the X-axis can be obtained by applying a varying magnetic field interacting with the magnetic dipole of the electron. Such a field can be simply generated by a current running in a transmission line nearby the qubit [26]. Alternatively, by applying a microwave excitation to a gate that is capacitively coupled to the quantum dot, the electron can be forced to oscillate in a magnetic-field gradient generated by a local magnet [24]. The required microwave frequency must match the energy difference between the two spin states, and is typically in the range of 13–40 GHz with gate times of 0.2–2  $\mu\text{s}$  for a  $\pi$ -rotation [24–26].

Electrons in neighbouring quantum dots must be isolated by tunnel barriers during normal operation. For two-qubit operation, the voltages coupled to the quantum dots or to the tunnel barriers can be adapted to allow interaction between two neighbouring electrons, thereby implementing either a SWAP gate or a CPHASE

gate depending on whether the pulses applied to the gates are sudden or adiabatic. First demonstrations used exchange couplings around 3–10 MHz [25,31], leading to pulse durations ~100 ns.

Read-out is typically performed by converting information on the electron spin into the position of the electron and sensing its charge. For this spin-to-charge conversion, energy-selective tunneling to an electron reservoir [33] or Pauli-exclusion tunneling to another dot [34] can be used. To detect the charge, either a charge sensor, such as a quantum point contact (QPC) or single-electron transistor (SET), or gate-based dispersive read-out [35] can be employed. In both cases, the read-out involves measuring an electrical impedance: for charge sensors, a variation of a few percents in a resistive impedance (~25 k $\Omega$  for QPCs, ~100 k $\Omega$  for SETs); for gate-based read-out, a variation of  $\ll 1$  fF on a capacitive impedance in the order of 1 pF.

Instead of trapping an electron in a quantum dot, an electron bound to a donor in the semiconductor substrate can be used, e.g. the excess electron provided by a phosphorous dopant atom in silicon [36–39]. While accurately placing the donor atoms poses a fabrication challenge, such a system has the advantage that, unlike quantum dots, all atoms are identical, thus allowing for reproducible behavior. In addition, the atom nuclear spin can be used as quantum memory for long-term storage of a quantum state ( $T_{2,nuc} = 30$  s has been demonstrated [39]). A typical donor-based system shows coherence times of  $T_2^* = 55$  ns [36], and  $T_2^* = 160 \mu\text{s}$  [39] in purified silicon. The operations on the donor-bound electron are implemented in the same way as for the electron trapped in a quantum dot. While the single-qubit operation times are similar, the qubit frequency in a donor system is typically slightly higher, i.e. in the range of 30–50 GHz [36,37,39]. Two-qubit gates have not yet been published, since they would require the donors to be placed closer than 20 nm [28]. This is currently hard to fabricate reproducibly, and could hinder the scaling up of the number of qubits.

### 2.3. Multiple-electron semiconductor qubits

The main disadvantage of the single-electron spin-qubits discussed above is that microwave signals are required for single-qubit operations and that these operations are generally much slower than the two-qubit operations based on the exchange interaction. As an alternative, it has been proposed to also use this much faster exchange interaction for single-qubit rotations, but at the cost of requiring multiple electrons to implement one qubit.

In case of the singlet-triplet qubit, the singlet and triplet configurations of two electrons distributed over two quantum dots are used as the basis states of the qubit [40–46]. A coherence time of

$T_2^* = 10$  ns has been demonstrated in a GaAs sample, which can be significantly boosted with e.g. strong magnetic field gradients ( $T_2^* = 700$  ns) [46] or pumping schemes to obtain dynamic nuclear polarization [42]. Single-qubit rotations that flip the qubit state (X rotations) are then implemented by suddenly pulsing the voltage on the gates close to the quantum dots (similar to two-qubit gates for single-electron spin-qubits), with typical  $\pi$ -rotations of  $\sim 1$  ns [41,44]. Single-qubit rotations altering the phase of the qubit (Z rotations) rely on an ever-present magnetic field gradient between the two quantum dots that continuously rotates the qubit. By timing the period between different operations, the desired rotation can be obtained. This rotation is generally slower, e.g.  $10\times$  slower in Ref. [44]. Two-qubit gates can be implemented by capacitively coupling two pairs of quantum dots, each encoding a qubit, resulting in an operation time below  $1\ \mu\text{s}$  [44,46]. The strength of this capacitive coupling is approximately proportional to the exchange interaction in both qubits. Read-out of the quantum state exploits the Pauli-exclusion principle to convert the quantum state encoded in the spin into a different charge occupation in the quantum dots, which is consecutively measured using a charge sensor.

A drawback of singlet-triplet qubits is that a magnetic field gradient is required between the two quantum dots. The design can be simplified by adding a third electron to represent a single qubit, as is the case for the exchange-only qubit and the hybrid qubit. In the exchange-only qubit, three quantum dots in a row, each containing a single electron, are used to implement a single qubit [47–52]. Using the pairwise exchange interaction between the middle quantum dot and one of the outer quantum dots, single qubit rotations can be obtained around two axes at a  $120^\circ$  angle. In Ref. [50], exchange operations with a tunable duration from  $0.01\ \mu\text{s}$  to  $1\ \mu\text{s}$  have been measured around both axes, while obtaining a coherence time of  $T_2^* = 2.3\ \mu\text{s}$  in purified silicon. Proposals exist to implement two-qubit gates using only the exchange interactions between the quantum dots [47,52].

In the hybrid qubit, the three electrons are placed in only two quantum dots, thereby simplifying the gate geometries and fabrication [6,53–57]. Single-qubit rotations around different axes are also obtained by suddenly pulsing the gates. In this way,  $\pi$ -rotations in less than  $100\text{ ps}$  have been demonstrated and coherence times of  $T_2^* \sim 10$  ns have been achieved [6]. For the two-qubit gates, it has been shown that in theory fewer exchange-interactions are required between two double quantum dots than in the case of the exchange-only qubit [53].

#### 2.4. Controller specifications

Table 1 summarizes the electrical signals required for the different qubit technologies to drive the various gate operations and to be acquired for the read-out. In general, it is sufficient for the electronic controller to generate electrical voltage pulses in base-band, e.g. for single and two-qubit gates in singlet-triplet qubits, or at microwave frequency, e.g. for single-qubit gates for transmons. Likewise, the read-out electronics must demodulate pulses at base-band or at microwave frequencies. In addition, but not shown in Table 1, the electronics must bias the quantum hardware appropriately, i.e. provide stable voltage bias for all gates in spin-based systems and provide accurate current for the flux bias for transmons.

On top of providing the required functionalities, the properties of the driving signals must be tightly controlled, both in terms of accuracy in the frequency, the amplitude and the duration, and in terms of low electrical noise levels, in order not to degrade the inherent fidelity of the qubits. The fidelity specifies how accurately an intended operation is performed. As the fidelity achieved in current qubit technologies is too low for algorithm execution, quantum error correction (QEC [10]) can be used to improve the fidelity

by encoding the quantum state on a larger number of physical qubits. QEC requires a minimum fidelity of the physical qubits and employs continuous cycles of qubit measurement with feedback control. Since feedback must be applied well within the qubit coherence timescale for QEC to be effective, fast qubit measurements and low controller latency are required. However, most state-of-the-art experiments do not apply QEC and feedback control, and, as a result, long measurement times ( $< 1$  ms) are typically used to allow filtering of the noise and thereby increase the read-out fidelity in semiconductor qubits. For this reason, Table 1 does not report measurement times for semiconductor qubits, although QEC would ask for a read-out time in the order of  $100\text{ ns} - 1\ \mu\text{s}$ . The control fidelity is inherently limited by non-idealities in the quantum processor, but can be further limited by non-idealities in the applied control signals.

The effect of signal non-idealities can be either simulated [58] or analytically evaluated [59,60]. As an example, the sources of inaccuracy and the related specifications of the microwave pulse that achieves a 99.9% fidelity for a  $\pi$ -rotation on a single-electron spin qubit are shown in Table 2. These have been derived using the methods outlined in Ref. [60]. Although a fidelity of 99.9% has only recently been achieved in several qubit technologies, such fidelity level would be the absolute minimum for QEC [10] thereby representing the absolute minimum specifications that should be targeted. It is important to note that the sensitivity to non-idealities in certain signal properties can be reduced by several techniques, such as pulse shaping [61], dynamical decoupling [62], and by performing the qubit gates in a different operating point that is e.g. less sensitive to charge noise [63].

Furthermore, constraints on the electrical interface are also set by qubit idling, i.e. the periods during which no operation is performed on a qubit that must just preserve its quantum state. Examples are the noise level on the gates of an idle spin-based qubit and the crosstalk on an idle qubit while a microwave signal is driving the single-qubit rotation of a neighbouring qubit. However, the signal specifications are generally more relaxed during idle periods than when performing an operation. For example, the gate bias voltage fixing the exchange interaction for spin qubits must be accurate during the qubit operation, but during idling a lower accuracy can be tolerated, as long as the interaction is sufficiently low [28]. Nonetheless, if the idle time is much longer than the operation time, specifications driven by idling can become significant.

Surprisingly, the electrical requirements for each qubit technology have not yet been systematically analyzed, resulting in quantum-computing experimentalists to simply overdesign their electronic setups, as described in the following section. The interested reader is referred to Ref. [60] for a complete analysis of the electrical specification for single-electron spin qubits, which shows a methodology that can in principle be adapted to any qubit technology.

### 3. Review of state-of-the-Art controllers

In this section, we will show how state-of-the-art experimental setups generate the control signals and acquire the read-out signals, as required by existing quantum processors.

#### 3.1. Superconducting qubits


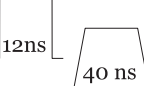
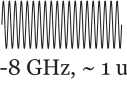







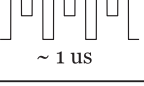


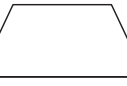


Fig. 3 shows the experimental setup used in Ref. [17] to control a five-qubit transmon chip. A flux-bias line for each transmon is biased with a DC current to set the frequency of the respective qubit.

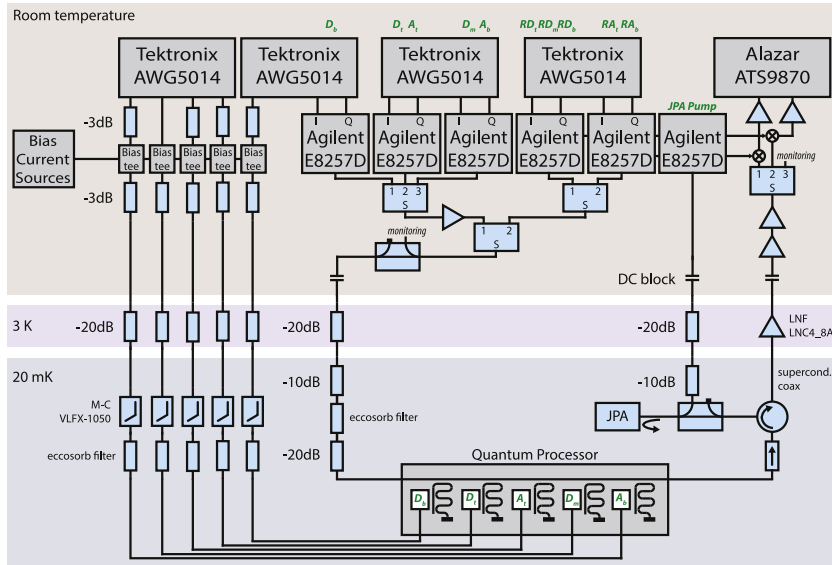
For two-qubit gates, pulses on the flux lines are generated by an arbitrary waveform generator (AWG, here the 4-channel 1.2 GS/s



**Table 1**

Summary of the various signals required to implement the various gate operations in different qubit technologies.

Technology	$T_2^*$	1-Qubit gate	2-Qubit gate	Qubit read-out	DC-Biasing
Superconducting qubits (Transmons)	2.5 $\mu$ s	 ~ 6 GHz 20 ns	 12 ns / 40 ns	 7–8 GHz, ~ 1 $\mu$ s	flux-bias current
Single-electron spin qubits in a quantum dot	120 $\mu$ s	 13–40 GHz ~ 1 $\mu$ s	 ~ 100 ns		gate voltage
Single-electron spin qubits in a donor system	160 $\mu$ s	 30–50 GHz ~ 1 $\mu$ s	 ~ 100 ns		gate voltage
Singlet-triplet qubit	700 ns	 ~ 1 ns	 ~ 1 $\mu$ s		gate voltage
Exchange-only qubit	2.3 $\mu$ s	 10 ns ...1 $\mu$ s	Sequence of pulses between different quantum dots		gate voltage
Hybrid qubit	< 10 ns	 ~ 100 ps	Sequence of pulses between different quantum dots		gate voltage

**Fig. 3.** Example of a setup used for superconducting transmon qubits [17].**Table 2**Example specifications for a  $\pi$ -rotation on a single-electron spin qubit for a fidelity of 99.9%.

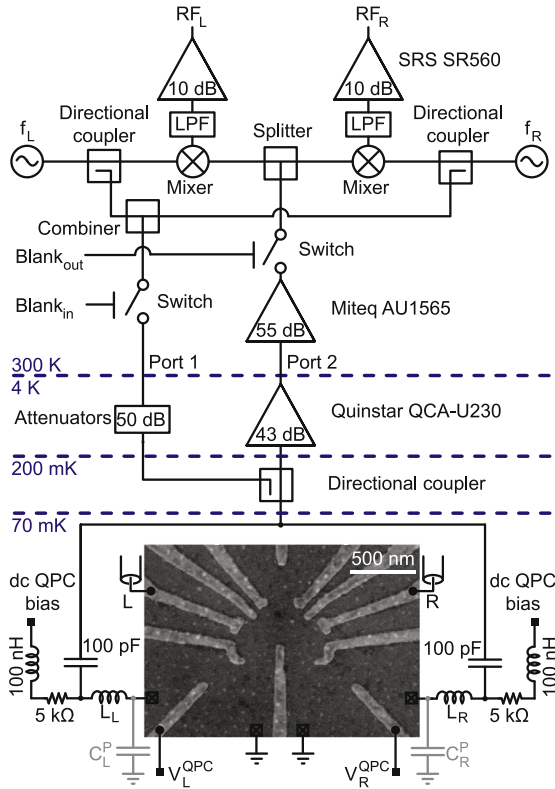
Frequency inaccuracy	11 kHz
Phase noise	−106 dBc/Hz at 1 MHz offset, −20 dB/dec slope
Wideband additive noise	7.1 nV/ $\sqrt{\text{Hz}}$
Phase inaccuracy	0.64 °
Amplitude inaccuracy	14 $\mu$ V on 2.0 mV amplitude
Amplitude noise	SNR = −40 dB
Duration inaccuracy	3.6 ns on 500 ns nominal duration
Timing jitter	3.6 ns <sub>rms</sub>

Tektronix AWG5014), and added to the DC component via wide-band 50- $\Omega$  bias-tees. For single-qubit gates, microwave signals need to be applied to the input port of the respective cavity. The

microwave carrier from a vector signal generator (VSG, here the Agilent E8257D) can be I/Q modulated by an AWG to generate the required DRAG pulses, e.g. for qubit  $D_b$  in Fig. 3. Additionally, the AWG can also provide a single-sideband modulation to drive a qubit at a frequency different from the carrier frequency provided by the VSG, as shown for all other qubits in Fig. 3.

The tones required for qubit read-out are generated in the same way, and all resulting carriers are combined before entering the cryogenic refrigerator. However, for the read-out, the carrier generated by the VSG is also fed into the acquisition circuit to down-convert the signal received from the cavity. A Josephson parametric amplifier (JPA [64]) at base temperature and a cryogenic low-noise amplifier (LNA [65]) are used to improve the signal-to-noise ratio (SNR) to allow for shorter measurement times. The pump signal required by the JPA is provided by a VSG. Additional gain stages are





**Fig. 5.** Example of a setup using RF-reflectometry of a QPC to sense the charge occupation of a triple quantum dot (image taken from Ref. [68]).

plitude accuracy specified in Table 2 translates into an 8-bit amplitude resolution, while the duration accuracy can be achieved with a sample rate of 150 MS/s. Those can be accommodated by the Tektronix 5014C that offers a 14-bit resolution with a 1.2 GS/s rate. The specified jitter of  $5 \text{ ps}_{\text{rms}}$  is significantly better than the required  $3.6 \text{ ns}_{\text{rms}}$ .

In summary, the performance of the analyzed setup is sufficient to drive single-qubit operations in an ideal quantum processor with a 99.9% fidelity. More in general, it can be concluded that typically adopted general-purpose instruments are not limiting the fidelity of state-of-the-art quantum computers, as shown in [60], since solid-state semiconductor qubits with fidelity exceeding 99.9% have been only recently demonstrated [73]. While this situation is desirable for current developments focused on improving the performance of quantum processors, the large performance margin in the electronic interface may not be tolerated as the performance and the scale of quantum processors improve, as discussed in Section 4.

#### 4. Challenges in scaling-up

State-of-the-art controllers for quantum processors described in Section 3 are well suited for current qubit experiments, but will show severe limitations when scaling up to the thousands of qubits as required for any practical quantum computer.

First, the general-purpose instruments used in current experiments are expensive, large and power hungry while only supporting a handful of qubits. Although this can be partially alleviated by sharing the hardware over multiple qubits, e.g. as in Fig. 3 (more details in Section 5.2), this can induce crosstalk effects between qubits, e.g. undesired phase shifts on undriven qubits [17,60]. A more scalable solution is the adoption of tailor-made electronics ensuring the required specifications and optimized for size, power

and cost. Multiple tailor-made controllers that have already been employed will be further discussed in Section 5.1. Tailor-made controllers can also be optimized for speed, thus avoiding issues arising in feedback control due to general-purpose instruments generally being too slow. For instance, the Tektronix 5014C AWG (see Figs. 3 and 4) has a delay longer than 500 ns between the arrival of a trigger and the generation of the actual output signal [71].

Another limitation is that, at the moment, every qubit requires individual control lines connecting the quantum processor in the refrigerator to the instruments at room temperature, e.g. the flux-bias lines for transmons and the gates for spin qubits. Since the number of lines that can be physically fitted in a dilution refrigerator is limited, the wiring can become a serious bottleneck in scaling-up. Moreover, more connections, especially between stages at different cryogenic temperatures, cause the system to become more complex, more expensive and less reliable. Furthermore, the heat conducted through each line from the warmer stages to the colder ones, together with the power dissipated in the various signal attenuators, adds to the thermal load of the dilution fridge, thus increasing the requirements on its cooling power. Lastly, because of the mere size of the typical dilution fridge and because of the large number of bulky instruments, the cables are long enough to cause delays that cannot be neglected in any case. For instance, a 1-meter cable results in a round-trip time of  $\sim 10 \text{ ns}$ , which can be comparable to the duration of the quantum operations (Table 1).

In order to limit the wiring complexity, two main approaches (or a combination of them) can be embraced [28,80]: multiplexing the control and read-out signals over a reduced set of wires (Section 5.2) and/or move the electronic interface closer to the qubits and operate it at cryogenic temperatures (Section 5.3).

### 5. Scalable electronic controller

#### 5.1. Tailor-made room-temperature controllers

Recently, various tailor-made quantum-processor controllers have been developed [74–79], as urged by the demand for highly integrated and flexible solutions for the rapidly evolving quantum processors. To maximize flexibility, these solutions generally use a reconfigurable Field-Programmable Gate Array (FPGA) at their core. Low delay is of utmost importance for quantum algorithms requiring feedback control. Direct processing of the read-out and control signals in an FPGA has a significant advantage in terms of latency compared to any software solution, while keeping the flexibility of in-field programmability. In addition, integrating the full controller around an FPGA eases the synchronization of the various components. A list of controllers and their capabilities is shown in Table 3. Additionally, commercial general-purpose instruments are evolving to fulfill the needs of quantum control, e.g. the Quantum Researchers Toolkit by Keysight offers a scalable modular control platform with a latency below 150 ns [81] and Zurich Instruments' series of HDAWGs a latency below 50 ns [82].

All electronic interfaces employ an FPGA as the main controller, and include hardware for both the generation of signals and analog-to-digital converters (ADC) to digitize the read-out signals. Such hardware can be either tailor-made and assembled on separate slave boards or comprise general-purpose instruments as in the setups described in Section 3. Processing of the read-out signals is performed in the FPGA. In general, this includes signal demodulation, filtering, decimation, signal integration and state discrimination. Special techniques can be used to bring down the latency, such as using frequency-selective kernels to combine the demodulation, filtering and integration in a single processing stage [76], or using digital mixing and multiplier-less filters [77].

**Table 3**  
Comparison of tailor-made room-temperature controllers.

Controller	Qin, 2017 [74]	Fu, 2017 [75]	Ryan, 2017 [76]	Salathe, 2018 [77]	Lin, 2018 [78]	Ofek, 2016 [79]
<b>FPGA</b>	Virtex-7	Cyclone V	Virtex-6	Virtex-4	Xilinx	Virtex-6
<b>Host interface</b>	USB 2.0	USB	1 Gb Ethernet		1 Gb Ethernet	PCIe
<b>Peripherals</b>	2 × TDC 12 × pulse generator	2 × 200 MS/s 8-bit ADC 8 × marker outputs	2 × 1 GS/s 12-bit ADC 2 × 1 GS/s 16-bit DAC	1 × 100 MS/s 14-bit ADC	2 × 2 GS/s 16-bit DAC	2 × 1 GS/s ADC 2 × 1 GS/s DAC
<b>Slave modules</b> with each:	<b>1 DAC board</b> 2 × 1 GS/s 16-bit DAC	<b>3 AWG modules</b> 2 × 200 MS/s 14-bit DAC	<b>up to 9 APS2 modules</b> 2 × 1.2 GS/s 14-bit DAC 4 × marker outputs			
<b>Latency</b>	–	80 ns (AWG only)	428 ns (+110 ns cabling)	283 ns (+69 ns cabling)		200 ns

On the control side, additional functionality can be added on top of straightforward digital-to-analog converters (DAC), such as micro-operations [75]. The Arbitrary Pulse Sequencer (APS2) proposed in Ref. [76] provides additional direct digital synthesis (DDS) to implement single-sideband modulation, thus allowing multiple qubits to be controlled by a single VSG. To control the frequency offset and keep track of the qubit phase, multiple numerically controlled oscillators (NCOs) are implemented in the FPGAs.

One common feature of the controllers in Table 3 is operation at room temperature, resulting in additional latency. Furthermore, these controllers still do not fully replace all required hardware for qubit interfacing, e.g. microwave signal generation is not included.

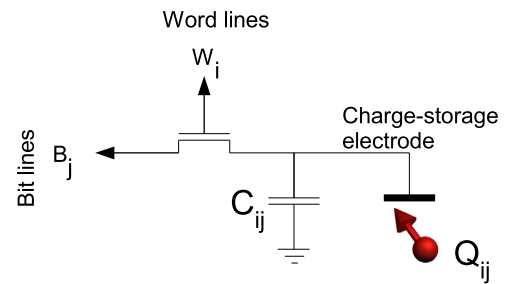
## 5.2. Multiplexing solutions

Multiplexing can help in reducing the number of wires, but comes with additional constraints as summarized in this section for time-division and frequency-division multiplexing.

**Time-division multiplexing.** In the simplest multiplexing form, the same line is alternately connected to different qubits by means of a switch (TDMA). In the control architecture proposed in Ref. [83], calibrated control waveforms are applied to a single line ('prime-line') that is switched over multiple qubits depending on the addressing information supplied by another set of lines ('address-line'). The proposed switch matrix is controlled by an FPGA operating at 4 K and placed at the base-temperature stage of the dilution fridge (20 mK). Switches can be implemented with either GaAs HEMTs or a proposed capacitive switch. In addition to the basic on/off switching, phase and amplitude modulation can also be implemented in the switch matrix by tuning the impedance of each switch [83]. This allows for the generation of specific signals from a limited set of waveforms provided from room temperature, thus representing the simplest example of a cryogenic electronic controller. Similarly, a Vector Switch Matrix (VSM) operating at room temperature is proposed in Ref. [84] to switch single-qubit-gate control pulses over multiple transmons. Additional electronics included with each switch enables the tuning of both the phase and amplitude so that the signals to each qubit can be individually calibrated to take into account qubit fabrication inhomogeneity. In order to further reduce the number of lines, the address can be sent over a serial interface [80].

In Ref. [85], the addressing scheme is extended to a 2D array using word and bit lines as in classical memories. A crossbar addressing scheme, similar to the use of word and bit lines, can theoretically also be directly used to control a large grid of qubits without the need for additional devices like switches, as proposed in Ref. [28,86]. While this is an effective method to reduce the amount of interconnects, it requires a certain level of homogeneity in the qubit grid to obtain sufficiently accurate operations.

Time-division multiplexing may require the terminals of the quantum devices to remain floating for a given period. In order to keep such a terminal properly biased, as required e.g. for gates in



**Fig. 6.** Gate biasing using a local storage element and time division multiplexed access via word and bit lines (image taken from Ref. [28]).

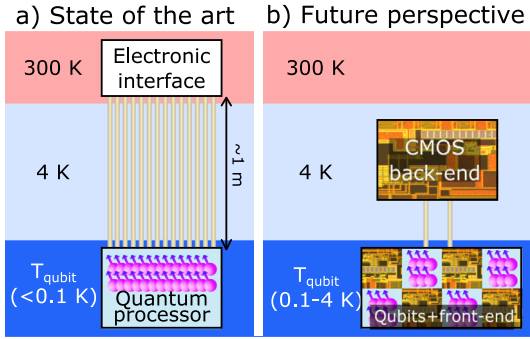
spin qubits, a sample-and-hold capacitor can be used to store the bias voltage at the gate and must be only periodically refreshed, similar to a DRAM cell (Fig. 6) [85,87,88]. However, typically a relatively bulky capacitor in the order of 100 fF is required to achieve low enough voltage fluctuations, limited by either charge quantization or sampling noise [28].

While time-division multiplexing increases the scalability of the system, it strongly limits the amount of parallelism in the execution of quantum gates. As a result, not only the execution of the quantum algorithm becomes longer, but also the qubits will be idle for extended periods of time during which decoherence takes place, as discussed in details in Ref. [80], thereby affecting the qubit fidelity. Furthermore, such multiplexing often requires a switch for each terminal of the quantum device. For qubits demanding a small pitch, such as spin qubits requiring ~100 nm pitch between quantum dots, integrating even a single switching device, i.e. a transistor, per qubit will be extremely challenging, as the needed density for the switching devices is higher than what is currently offered by the most advanced CMOS technologies [89].

**Frequency-division multiplexing.** In case of frequency-division multiple access (FDMA), different frequency bands on the same line are allocated for simultaneous use of different sub-blocks. As each individual superconducting transmon can be designed and tuned to a different resonance frequency at which it is sensitive (Section 2), frequency multiplexing can be directly used for control. In Fig. 3, the read-out of different transmons also uses a different frequency band thanks to the use of different read-out resonators tuned to different frequencies and coupled to the same on-chip transmission line [90].

Similarly, for single-qubit gates, single-electron spin qubits are only sensitive to signals at a given frequency, which is determined by the externally applied magnetic field. Frequency differences among neighbouring qubits, as required for FDMA, can be introduced using the Stark shift [26,31] or by generating magnetic-field gradients by integrating on-chip micromagnets [24,25]. For an RF-reflectometry-based read-out, the use of FDMA is straightforward





**Fig. 7.** Implementing the controller inside the dilution refrigerator can significantly reduce the wiring complexity.

thanks to matching networks tuned to different frequencies [70], as shown in Fig. 5.

In order to limit the crosstalk between different channels, sufficient inter-channel frequency spacing is required. In case of qubit control, the crosstalk causes the AC-Stark shift, i.e. the qubit frequency appears to shift in the presence of signal power at a nearby frequency. As a result, either complex pulse shaping is required [91], or the channels have to be time multiplexed with the addition of a simple phase correction for all idling qubits after each operation [17]. Because of practical limitations on the available spectrum, and the need for sufficient channel spacing, a maximum number of channels of only 10–100 is expected [92]. Besides crosstalk, the application of frequency multiplexing in large-scale processors may be limited by the need for large frequency-selective components, such as waveguide resonators for transmons and matching networks in RF-reflectometry of spin qubits, although for the read-out this may be alleviated by crossbar approaches [28].

### 5.3. Cryogenic controllers

In order to further reduce the wiring complexity and latency, placing the electronic controller close to the qubits, and hence operating it at cryogenic temperatures inside the dilution refrigerator, has been proposed [28,92–97]. Ideally, the electronics should operate directly at base temperature next to the quantum processor. However, as the cooling power of typical refrigerators is lower at colder temperatures [98], only limited functionality could be implemented at sub-K temperatures. Some researchers anticipate that the power dissipation of the electronics can be reduced to a level compatible with the cooling power of existing refrigerators at sub-K temperatures, thanks to optimization of both the design and the microelectronic fabrication. Although Ref. [96] estimates that  $\sim 100$  singlet-triplet qubits can be controlled by electronics fabricated in a commercial 65-nm CMOS process operating at 100 mK, most researchers advocate for the largest section of the electronic interface to operate around 4 K (Fig. 7), i.e. a temperature at which dilution refrigerators have significantly more cooling power (up to a few Watt). However, while a controller at 4 K solves the problems related to the wiring to room temperature, interfacing to a quantum processor operating at sub-K temperatures remains a challenge. Relatively high-power electronics could be placed close to the quantum processor if thermally-isolating interconnect (such as superconducting through-silicon vias [99]) could be employed to avoid heating up the qubits. Using superconducting wires between the 4-K electronics and the quantum processor would drastically reduce the heat load on the sub-K stage [100,101], but would not alleviate complexity and reliability issues, which could otherwise be circumvented by multiplexing at base temperature

(Section 5.2). Alternatively, preliminary studies promise the feasibility of some qubit technologies, spin qubits more specifically, operating at higher temperatures [29]. In that case, both the quantum processor and its electronic interface could be placed at the same temperature (1–4 K) [28].

Several electronic technologies have proven their functionality down to deep cryogenic temperatures, and can hence be used to implement the controller. These include JFET, HEMT, superconducting devices based on Josephson junctions (e.g. single flux quantum logic, SFQ [102]), compound semiconductors (e.g. GaAs) and CMOS transistors [103,104]. CMOS has shown functionality down to 30 mK [105,106], and it is the most advanced among these technologies. Thanks to the push of the semiconductor industry, CMOS offers an established design automation infrastructure and the possibility to integrate billions of transistors on a single chip, as would be required to interface millions of qubits. Consequently, it is generally considered the most promising choice for the integration of a cryogenic electronic interface for quantum processors.

MOS transistors are fully functional at cryogenic temperatures, but their performance is different with respect to its standard temperature range. Improvements appearing at cryogenic temperatures include increased mobility, and hence larger maximum current, higher subthreshold slope, lower leakage and lower thermal noise [107,108]. As a drawback, the threshold voltage increases, thus leading to less voltage headroom, and flicker noise performance and device matching degrade [97,109]. As a major difference with respect to more mature CMOS technologies, advanced nanometer CMOS technologies are not affected by critical cryogenic non-idealities, such as current kink or hysteresis [107,110]. However, accurate device modelling is required even for nanometer CMOS technologies to enable the design of complex optimized cryogenic CMOS (cryo-CMOS) circuits [93,107].

Nevertheless, some commercial CMOS integrated circuits (IC) are functional at cryogenic temperatures, well below their target temperature range. Most notably, some FPGAs remain fully functional down to 4 K with marginal change in operating speed [111], and even DRAM seems functional down to 80 K [112]. The FPGAs could form the basis of a highly reconfigurable cryogenic control platform [94], similar to the current tailor-made controller at room temperature (Section 5.1). The ability to program the device in the field can prevent expensive and time-consuming warm-up/cool-down cycles of the dilution fridge during development. In Ref. [111], the flexibility of a cryogenic FPGA platform has been demonstrated with the implementation of an FPGA-based reconfigurable ADC.

While some commercial ICs can be directly used out of the box, the best performance and highest level of integration can only be achieved by custom cryo-CMOS designs. Several components required for the control and read-out of a quantum processor have been designed and optimized for operation at cryogenic temperatures. In Ref. [113], pulse generators for qubit control using either a mixed-signal or a fully-digital implementation have been integrated in a 500-nm Silicon-on-Sapphire (SOS) CMOS process. Both implementations can generate pulses with variable duration down to 10 ns. In Ref. [114], a 6-bit DAC designed in the same technology uses an analog calibration technique to overcome the increase in device mismatch at 4 K. A smaller 4-bit implementation demonstrates a fast rise time of 600 ps at 4.2 K [114]. A 40-nm CMOS digitally controlled oscillator for signal generation at cryogenic temperature has demonstrated state-of-the-art phase-noise performance at 4 K while generating frequencies (5.5–7 GHz) compatible with transmon control [97].

For the read-out, an LNA fabricated in a 500-nm SOS CMOS process shows noise sufficiently low to measure the impedance of an SET in a measurement time of only  $\sim 520$  ns [115]. Another LNA,

integrated in a bulk 160-nm CMOS technology for the use in an RF-reflectometry read-out achieves a gain of 57 dB and bandwidth of 500 MHz at 4 K with an in-band noise figure of 0.1 dB (7 K noise temperature) [97].

Besides these circuits, which are specifically designed for qubit control and read-out, various circuits operating at cryogenic temperatures exist for applications ranging from space missions to high-energy-physics, but are out of the scope of this review. Furthermore, while cryo-CMOS has many advantages, other technologies show superior performance in terms of noise (e.g. SiGe) or power consumption (e.g. SFQs) and could be a better alternative, e.g. for the use in LNAs and FPGAs [102], respectively. In fact, co-integration of a quantum processor and classical controller has already been demonstrated for an SFQ-based controller [116].

## 6. Conclusions

While state-of-the-art setups are well capable of fulfilling the requirements set by the different quantum technologies, they are subject to severe limitations when quantum processors will scale up. By using tailor-made electronic controllers at room temperature, the cost, size and power consumption can be reduced, while also enabling optimization for low-latency feedback. However, to obtain a truly scalable quantum computer, the interconnect complexity between the quantum processor and the electronic interface must be drastically reduced. While multiplexing techniques are effective in this sense, they still present a number of stringent drawbacks. On the contrary, the adoption of cryogenic electronics promises the deployment of truly scalable controllers. These cryogenic controllers can be implemented in standard CMOS technologies in order to exploit large-scale high-yield fabrication, thus allowing the ultimate vision of co-integrating the electronic interface with the qubits on a single chip, or, at least, to operate the electronics in close proximity to the quantum processor. Initial steps have already been taken in this direction, thus paving the way to large-scale cryo-CMOS electronic interfaces that will make the operation of future quantum computers addressing real world-changing problems possible.

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