

Microwave Drivers for Quantum Computing: Advancements Towards Scalable Qubit Control

Brennan Undseth
5021480

Scarlett Gauthier
5023602

Abstract—Microwave drivers are ubiquitous in the leading approaches for the implementation of fault tolerant quantum computers. Although present devices are small enough to be controlled by general-purpose electronics at room temperature, an important research direction is moving this control to 4 K in such a way that quantum hardware remains thermally isolated and the number of control lines scales sub-linearly with the number of qubits. This approach alleviates many difficulties of room-temperature control at the cost of introducing a new suite of challenges due to the cryogenic temperatures. These are best summarized as a trade-off between power consumption and device performance. Furthermore, enabling frequency-division multiple-access in microwave controllers provides a promising way to overcome the qubit wiring bottleneck. Engineers hence face a diverse set of tasks. In this review, we discuss these hurdles and how they are being tackled in state-of-the-art research.

I. INTRODUCTION

Progress in experimental quantum information processing in recent decades has involved the slow but steady increase in the number of qubits interacting in a single quantum processor. In tandem, attention has been directed towards implementations that can scale to allow a number of qubits that will support the overhead requirements of fault-tolerant quantum computation (FTQC). As such, pioneering implementations such as liquid-state nuclear magnetic resonance have given way to chip-based solid-state platforms that are tasked with supporting millions of well-behaved qubits. While the common appearance of qubits has changed in the past 20 years, many aspects of interfacing quantum computers with the classical environment have remained the same. One such constant is the use of microwave-frequency driving of qubit operations, which are essential to carrying out logical quantum computations. Therefore, just as the number of qubits must scale to achieve FTQC, so too must the accompanying electronics.

In this review, we cover the importance of microwave drivers for the most promising approaches to scalable quantum computing and highlight the obstacles associated with implementing RF circuitry commensurate with a FTQC. Firstly, the specific utility of microwave signals in solid-state qubits is reviewed. Next, we will cover the role microwave control plays in the current bottleneck of scalability, as well as the challenges that the field must overcome. Next, potential solutions are explored. These include: moving microwave drivers to cryogenic temperatures to bring them closer to the quantum hardware they are controlling; and using multiplexing techniques to maximize the number of qubits that may

be manipulated with a single drive. Lastly, state-of-the-art research in the field is discussed.

II. MICROWAVE CONTROL OF SOLID STATE QUBITS

We focus on solid state devices that are suitable for the large scale integration essential to developing processors supporting FTQC. Promising platforms include semiconductor single- and multiple-electron spin qubits, superconducting qubits, and color centers in diamond such as the nitrogen vacancy (NV). See [5] and [3] for recent reviews. With the exception of multiple-electron spin qubits, a commonality between each of these systems is a reliance on microwave control electronics for the purposes of performing gates. We will briefly describe gate implementation in multiple-electron spin qubits on the grounds of exploring a control technique not reliant on microwaves.

The principle advantage of microwave based control systems is that a wide range of high fidelity operations across all applicable platforms can be performed with existing methods. To illustrate this point, we briefly introduce microwave control techniques on each platform.

Control of superconducting transmon qubits can be accomplished by coupling the qubits to on-chip microwave cavities. Single qubit rotations about an arbitrary axis in the X-Y plane can be accomplished by tuning the phase and amplitude of frequency matched microwave pulses, which are usually in the 4-6 GHz range [7], [5]. Since a transmon qubit is not a true two level system, Gaussian pulse shaping and I/Q modulation following the Derivative Reduction by Adiabatic Gate (DRAG) approach are used to combat leakage to higher energy levels. As for the implementation of two qubit gates, interactions from the native set (for example CPHASE) can be accomplished by flux tuning the qubits to couple with the same microwave cavity [5]. The realization of two qubit gates has been reported in many publications and typical gate times range from tens of nanoseconds up to microseconds [7].

With regards to microwave control techniques for single electron semi-conductor platforms we describe qubits defined by the spin of a single electron trapped in a quantum dot. In this platform microwave control is primarily important for executing single qubit gates, as two qubit gates are typically based instead on the Heisenberg exchange interaction. To drive a single qubit gate, a microwave excitation is applied to one of the gate electrodes capacitively coupled to the quantum dot. The success of these gates relies on frequency matching the microwave frequency with the energy difference between the

two spin states, which is often in the 13-40 GHz range. These single qubit gates work on the microsecond timescale [5].

In multi-qubit processors based on NV's single qubit gates are possible using on chip delivery via waveguide of appropriate microwave pulse sequences. In this way it is possible to drive the electronic spin transitions, which can be accomplished on the nanosecond timescale, as well as to induce rotations of the nuclear spins, which is possible on the microsecond timescale [3]. Of particular interest are two qubit gates between the electron and nuclear spin. One exemplary realization of such a two qubit gate interleaves phase controlled radio frequency (rf) driving of the nuclear spin with dynamical decoupling of the electron spin in order to achieve high fidelity multi-qubit control [1].

The above discussion highlights that existing microwave control electronics have been sufficient to demonstrate universal quantum logic in solid state quantum processors. It is thus clear that an advantage of microwave control is that the field is very well established in both a practical and a theoretical sense. Practically speaking, reliable devices that are capable of microwave pulse shaping are commercially available and relatively inexpensive when compared to the other components needed for a quantum processor. On the theoretical side, the broad base of understanding which underpins the field of microwave electronics is a boon to researchers developing controls for quantum devices. As a specific example, consider the use of I/Q modulation for preventing leakage from the computational subspace of transmon qubits. The inherited benefit is clear since I/Q modulation is a well established tool in the field of microwave engineering [10].

Advantages withstanding, challenges have also arisen from interfacing microwave technology with the several micron and sub-micron scale devices engineered to be quantum processors. One important challenge comes from the inherent mismatch between the device sizes and the wavelengths of microwaves, which are in the 1 mm - 30 cm range. Since the wavelength of a wave directly determines the area over which it carries energy to, if a comparatively small area is targeted by a long wavelength carrier, then more cycles are needed to impart a given energy than would be necessary for a shorter wavelength carrier of the same power. Increasing the power of the microwave drive is possible at the cost of dissipating a larger amount of energy. The result is then heating of the cryogenic environment of the devices, thereby impacting processor performance and gate fidelities. Thus there is a trade-off between the power of a microwave drive and the time required to execute a gate operation. For a specific example, consider single-electron semiconductor qubits, where the scale is set by the pitch between neighboring qubits which is on the order of 100 nm [5]. In conventional electron spin resonance (ESR) control, a global microwave magnetic field is applied which can simultaneously implement rotation on many qubits. However, alternating current magnetic fields can give rise to excessive dissipation and heating. Electric dipole spin resonance (EDSR) enables more focused all-electrical control by introducing a permanent local magnetic field gradient through

which a microwave-frequency electric field can oscillate the electron and drive single qubit gates.

A further consideration concerning the use of microwave control techniques is the speed at which gates can be performed. In general, it is desirable to minimize gate times to allow the fast execution of a quantum computation before decoherence occurs. In the field of semiconductor based qubit devices, long gate times have served as one motivation for exploration of multiple electron spin qubits. These designs make use of the Heisenberg exchange interaction to implement fast single qubit operations, but typically suffer from much shorter decoherence times. Importantly, these implementations demonstrate that microwave control may not be necessary to achieve FTQC.[5].

In summary, for each of the solid state platforms of interest high quality microwave based qubit operations are possible and represent a precisely tunable control mechanism. Moreover, two performance based attributes which are important for microwave controllers are heat dissipation and achievable gate times.

III. THE NEED FOR SCALABLE ELECTRONICS

In present implementations of small quantum processors, the electronic interface with quantum hardware is usually not a limiting factor. For example, small universal quantum computers containing 2 to 5 qubits, such as those currently available via cloud access (e.g. Quantum Inspire, IBM Quantum Experience), may be controlled with room temperature electronics that are attenuated for use at cryogenic temperatures. This approach has worked for proof of principle experiments and early stage investigations into the performance of quantum processors [11], [4]. Despite these successful demonstrations it is highly questionable if the same approach can accommodate another order of magnitude expansion in the number of qubits, let alone the many orders required for fault tolerance [2].

Multiple properties associated with a system of room temperature electronics coupled to a processor at Kelvin or sub-Kelvin temperatures act as limitations. For one, the length of cabling spanning such a system imposes a fundamental speed limit in the transfer of information from controller to processor. This delay, on the order of 10 ns, can be on the same scale as the duration of qubit operations [5], [10]. Such a time overhead hampers the efficacy of any quantum error correction protocol, since delays between quantum operations introduce a greater probability of errors piling up. Second, the cooling power of dilution refrigerators is fundamentally limited, even at the coldest stages. Specifically, modern refrigerators may extract approximately 15 μ W at 10 mK [2]. Keeping the thermal load within this limit—a challenge in its own right—is exacerbated by the additional thermal load associated with cabling. To make sense of the origin of this thermal load, consider that the cabling connects systems at very different temperature scales and approximately thermalizes on both ends. Thus, heat dissipation must occur along its length.

An extreme alternative is attempting to place all electronics at the same temperature as the quantum hardware. Transmon

qubits require very low temperatures to maintain permissible decoherence times, and the cooling power of dilution refrigerators at these temperatures is fundamentally limited. Due to the amount of heat dissipation associated with operating classical CMOS circuitry, its implementation at these temperatures is considered infeasible. The intermediate approach has been favoured in recent proposals, whereby classical electronics are placed at the 4 K stage while superconducting transmission lines are used to couple to the much colder quantum hardware. The details of implementing a microwave driver at these temperatures is discussed in Section V.

It should be noted that the recent advent of "hot" spin qubits [9], which operate at temperatures on the order of 1 K as opposed to 10 mK, provide hope that a spin qubit processor may be able to support both quantum and classical hardware on one refrigeration stage with sufficient cooling power.

IV. MULTIPLEXING TECHNIQUES

A bottleneck common to all proposals of scalable FTQC is the number of control lines required to perform state initialization, manipulation, and readout. At present, every quantum dot spin qubit, NV center and transmon qubit requires connection to a wire off chip. For scaling beyond 1000 qubits, this is believed to be untenable. In classical electronics, Rent's rule quantifies a power law trend in the number of control terminals T as a function of internal components g :

$$T = tg^p, \quad (1)$$

where t is the number of connections for each internal component, and $p \leq 1$ is an optimization parameter. For an X86 architecture, $p = 0.36$. It is believed that a similar optimization will be necessary for the practical wiring of quantum processors [6]. Several approaches to this problem have been proposed. For the purposes of focusing the discussion on microwave driving technology, we will here discuss frequency-division multiple access (FDMA). This technique takes advantage of the frequency tunability of qubits. In transmons, the flux bias can be manipulated to make a qubit sensitive to driving at a particular frequency [5]. In single-electron spins, this frequency addressability can be achieved by applying a local magnetic field gradient between qubits or a local electric field to utilize the Stark shift [5]. In NV's on chip electrodes can supply a DC electric field to Stark tune the emission frequency [3]. The different interaction frequencies may be used to selectively drive qubit operations and, in the case of transmons, selectively read-out qubit states. Beyond the practicality of reducing the number of connections, FDMA does not restrict parallel quantum operations, as time-division multiple-access (TDMA) does, nor does it present difficult size constraints that come with a cross-bar addressing scheme [5]. This makes multiplexing using FDMA attractive both from an electrical engineering and an overall systems design perspective.

A microwave driver accommodating FDMA must support a wider range of frequencies in order to address qubits at sufficiently spaced bands. Furthermore, the frequency-selectivity

in classical electronics necessary for reading out transmon qubit states requires matching networks comprised of bulky components. These constraints place a limit on the number of channels that may be addressed using FDMA. Moreover, frequency multiplexing can cause cross-talk to occur between qubits due to the AC Stark effect. To mitigate this, sophisticated pulse shaping or corrective operations need to be applied. Implementing these features adds to the complexity of the electronic interface. Therefore, FDMA offers a path forward in reducing the number of connections required to interface with quantum hardware but brings its own set of technical challenges.

V. MICROWAVE DRIVERS AT CRYOGENIC TEMPERATURES

Interfacing classical CMOS technology with quantum hardware at 4 K requires a trade-off between limiting power consumption while retaining adequate performance such that fault-tolerance is achievable. Bardin et al. have proposed a limit of 250 μ W per qubit as a plausible level of power consumption for a cryogenic microwave driver. This considers the few-Watt cooling power available at 4 K as well as the power drawn by other electronics. Such a driver must maintain the bandwidth required by the associated quantum hardware. This can range from few GHz for transmons and NV's to tens-of GHz for single electron spins in donors [5],[3].

Furthermore, the fidelity of operations must be sufficiently high such that error rates are within the threshold for quantum error correction. Bardin et al. [2] use a benchmark of a 0.01% total error rate. Allowing a tenth of this error to be attributed to amplitude damping, an integrated π -pulse amplitude must be within 0.25% of the specified value. Similarly, the carrier phase must be kept within a 0.22% tolerance. Other constraints apply. For example, the spectral content of a microwave driver for a transmon qubit must not drive transitions out of the computational subspace. Depending on the hardware, pulse shapes, amplitudes, and durations must be designed for. For all hardware, noise on the driveline must not be the dominant source of decoherence.

VI. STATE-OF-THE-ART

Here, we highlight two developments in cutting-edge cryogenic microwave driver technology. As described in Section V, the designs balance power consumption, performance, and robust component selection. The focus in this section will remain on the design choices illustrating this trade-off. The first is a controller for transmon qubits developed by Google [2]. The second is Intel's "Horse Ridge" quantum control chip for driving both spin and transmon qubits [8].

The former is a 28 nm Bulk-CMOS controller designed to control XY rotations in transmon qubits in the 4 - 8 GHz frequency range from cryogenic temperatures [2]. Here we will refer to it as the "Google" controller. The basic operation of the controller is as follows: multiple DAC-controlled current sources are used to create two arbitrary symmetric pulse envelopes. The envelopes are passed through a low-pass filter and upconverted to the carrier frequency. The output pulse

is the combination of the two quadratures. An instruction set is integrated on the chip in order to save significant power consumption due to reduced digital I/O. A switched current-mirror architecture using minimum feature-size transistors was employed for the DACs to reduce both dynamic and static power consumption, at the expense of DAC performance. Furthermore, flip-flops in the pulse controller used to generate the current envelopes are gated such that they are only clocked when the output is scheduled to transition, reducing the power consumption further. The vector modulator circuit was similarly designed to limit frequency range to improve power consumption. In total, the controller dissipates 2.5 mW/qubit, which was chosen to be an order of magnitude greater than the quoted value in V with improvement expected in future designs [2].

The Google controller was fabricated and mounted on the 3 K stage of a commercial dilution refrigerator and used to control a single transmon qubit mounted to the 10 mK stage. Using the cryogenic controller, Rabi oscillation patterns were generated which showed that the calibrated amplitude control of pulses was sufficient to drive $|0\rangle \leftrightarrow |1\rangle$ qubit rotations, limited by the independently-determined fidelity of state read-out. The phase control was also evaluated experimentally, and it was concluded that deterministic control errors, rather than stochastic noise, were the primary source of errors. This could be ameliorated through improved pulse calibration. Lastly, neither the qubit relaxation time T_1 nor leakage prevention to the $|2\rangle$ state was found to deteriorate when using the cryogenic controller.

Horse Ridge [8] extends the capabilities of Google's pulse modulator as well as addresses some shortcomings in the design. These disadvantages include requiring one local oscillator and cable per qubit, as well as requiring extra circuitry for leakage cancellation due to the local oscillator being at the qubit frequency. Horse Ridge lifts the one-qubit-one-cable requirement by enabling FDMA, as described in Section IV. Additionally, the functionality of the device has been extended to drive both spin qubits and transmons, requiring a wider range in both frequency (2 - 20 GHz) and output power. The use of instruction tables in the digitally intensive architecture increases the versatility of pulses that may be generated while also reducing the data rate to the controller. These improvements allow Horse Ridge to individually address up to 128 qubits while maintaining a power dissipation of 1.7 mW/qubit, which is within the order of magnitude expected to be compatible with fault-tolerant scalability.

Preliminary testing of Horse Ridge has been conducted both by driving Rabi oscillations in a spin qubit as well as performing coherent rotations around different axes in the form of an $X(\pi/2) - Z(\theta) - X(\pi/2)$ pulse sequence. The Rabi oscillations were directly comparable to those obtained on the same setup using room-temperature control electronics. While these initial results are promising, further work will be required to effectively characterize the accuracy of qubit control as well as address multi-qubit crosstalk in the FDMA scheme.

VII. CONCLUSION

Beyond improvements to quantum hardware, the development of functional fault tolerant quantum computers will require significant advances in control technology. To enter the next generation the microwave drivers essential to modern solid state quantum processors will need to be functionally mounted at the 4 K stage of cryogenic housing, and utilize multiplexing techniques. Prototype controllers which incorporate these design requirements have already been actualized and demonstrate performance that is on par with traditional control systems. The next frontier for development in this field will be to push next generation devices beyond the capabilities of existing hardware.

REFERENCES

- [1] C. E. Bradley et al. "A Ten-Qubit Solid-State Spin Register with Quantum Memory up to One Minute". In: *Phys. Rev. X* (2019). DOI: 10.1103/PhysRevX.9.031045.
- [2] J. C. Bardin et al. "Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K". In: *IEEE Journal of Solid-State Circuits* (2019). DOI: 10.1109/JSSC.2019.2937234.
- [3] Lilian Childress and Ronald Hanson. "Diamond NV centers for quantum computing and quantum networks". In: *MRS Bulletin* (2013). DOI: 10.1557/mrs.2013.20.
- [4] L. DiCarlo et al. "Demonstration of two-qubit algorithms with a superconducting quantum processor". In: *Nature* (2009). DOI: 10.1038/nature08121.
- [5] Jeroen P. G. van Dijk, Edoardo Charbon, and Fabio Sebastiano. "The electronic interface for quantum processors". In: *Microprocessors and Microsystems* (2018). DOI: 10.1016/j.micpro.2019.02.004.
- [6] David P. Franke et al. "Rent's rule and extensibility in quantum computing". In: *Microprocessors and Microsystems* (2019). DOI: 10.1016/j.micpro.2019.02.006.
- [7] Morten Kjaergaard et al. "Superconducting Qubits: Current State of Play". In: *Annual Review of Condensed Matter Physics* (2020). DOI: 10.1146/annurev-conmatphys-031119-050605.
- [8] B. Patra et al. "A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 432 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020. DOI: 10.1109/ISSCC19947.2020.9063109.
- [9] Eenink H.G.J. Russ et al. M. Petit L. "Universal quantum logic in hot silicon qubits". In: *Nature* (2020). DOI: 10.1038/s41586-020-2170-7.
- [10] David M. Pozar. *Microwave Engineering 4th Edition*. Wiley, 2011. ISBN: 1118213637.
- [11] L. Vandersypen, M. Steffen, and G. Breyta et al. "Experimental realization of Shor's quantum factoring algorithm using nuclear magnetic resonance". In: *Nature* (2001). DOI: 10.1038/414883a.