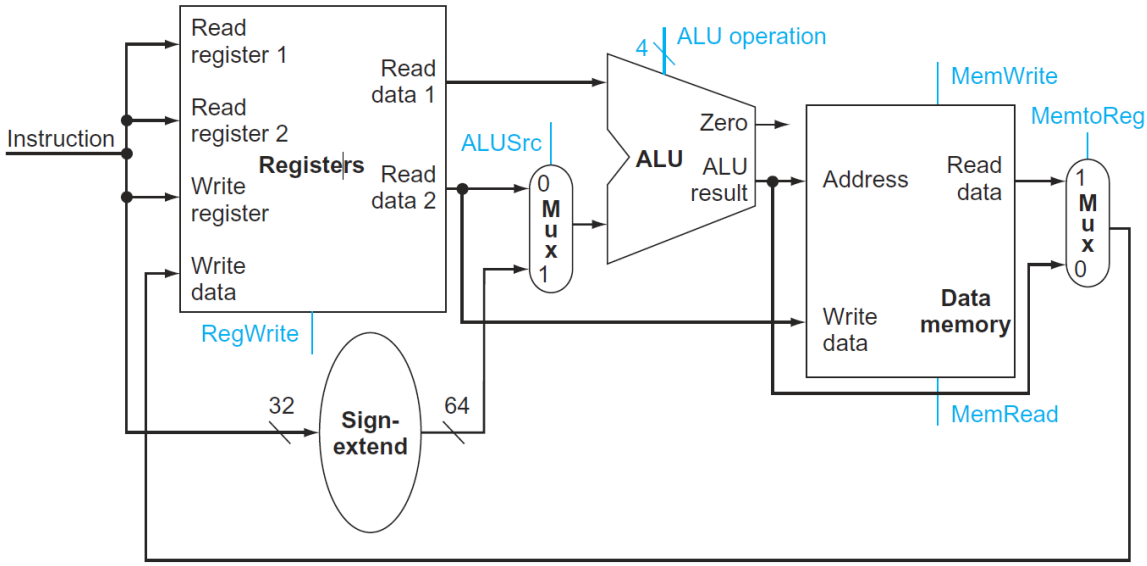
Homework 3

Requirement：

Please type your answers in this .docx file. Do **not** submit handwriting documents.

1. (18 points) Consider the following instruction:
   Instruction: AND Rd, Rn, Rm
   Interpretation: Reg[Rd] = Reg[Rn] AND Reg[Rm]
   (1) Configure these control signals: RegWrite, ALUSrc, MemWrite, MemRead, MemtoReg, to make the following hardware execute the above AND instruction. Assume that ALUoperation has been configured to let ALU do AND operation.
   (2) Which resources perform a useful function for this instruction?
   (3) Which resources produce no output for this instruction? Which resources produce output that is not used? Please select from these resources: Registers, ALUSrc MUX, ALU, Data memory, MemtoReg MUX, and Sign-extend.



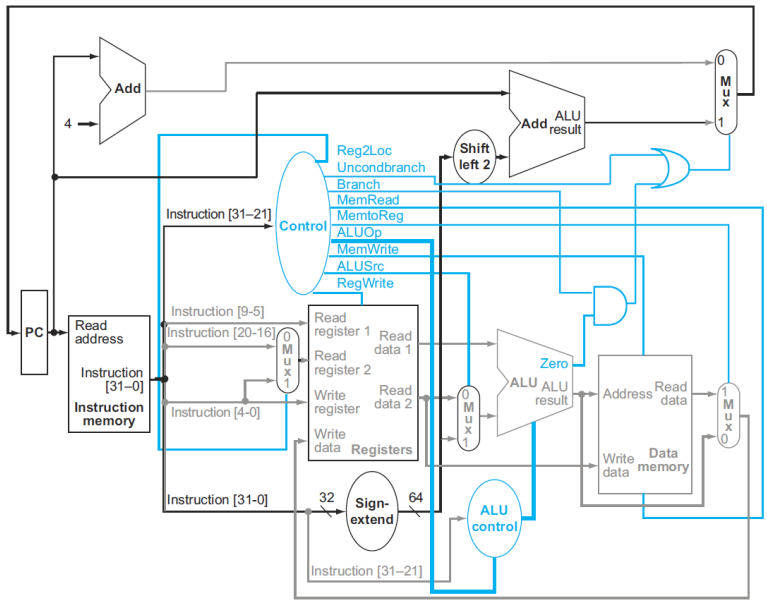
2. (16 points) Consider the following instruction mix:

R-type	LDUR	STUR	CBZ
52%	25%	10%	13%

   (1) What fraction of all instructions use data memory?
   35%
   (2) What fraction of all instructions use instruction memory?
   13%
   (3) What fraction of all instructions use the sign extend?
   48%
   (4) What is the sign extend doing during cycles in which its output is not needed?

nothing

3. (12 points) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get “broken” and always register a logical 0. This is often called a “stuck-at-0” fault. For the following chip:



(1) Which instructions fail to operate correctly if the MemToReg wire is stuck at 0? Please select from R-type, LDUR, STUR, CBZ.

LDUR, STUR

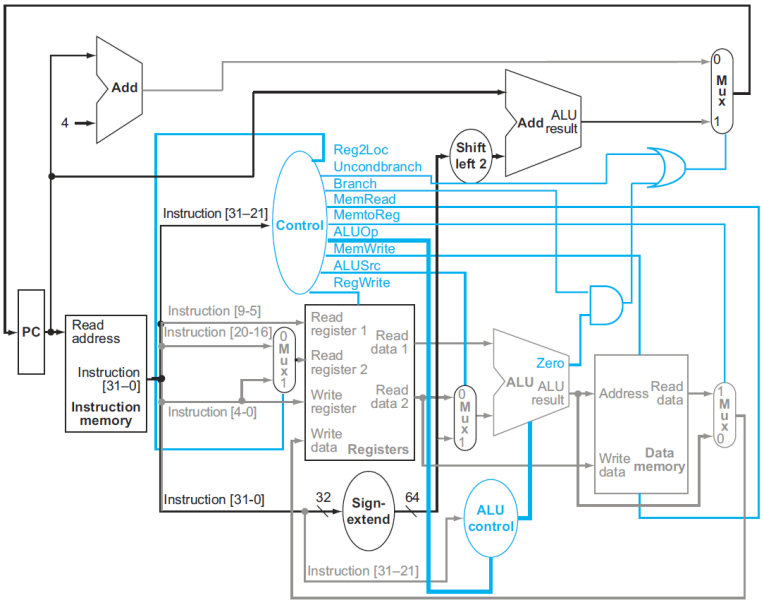
(2) Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0? Please select from R-type, LDUR, STUR, CBZ.

R-type

(3) Which instructions fail to operate correctly if the Reg2Loc wire is stuck at 0? Please select from R-type, LDUR, STUR, CBZ.

CBZ

4. (20 points) Instruction 0xf8014062 is fetched and executed in the following single-cycle datapath.



(1) Convert instruction 0xf8014062 from machine language to assembly language.
(2) What are the values of the control unit's outputs for this instruction?
(3) What is the new PC address after this instruction is executed?
(4) What are the input values for the ALU and the two add units?

5. (15 points) The execution time for different stages of a datapath is shown in the following table:

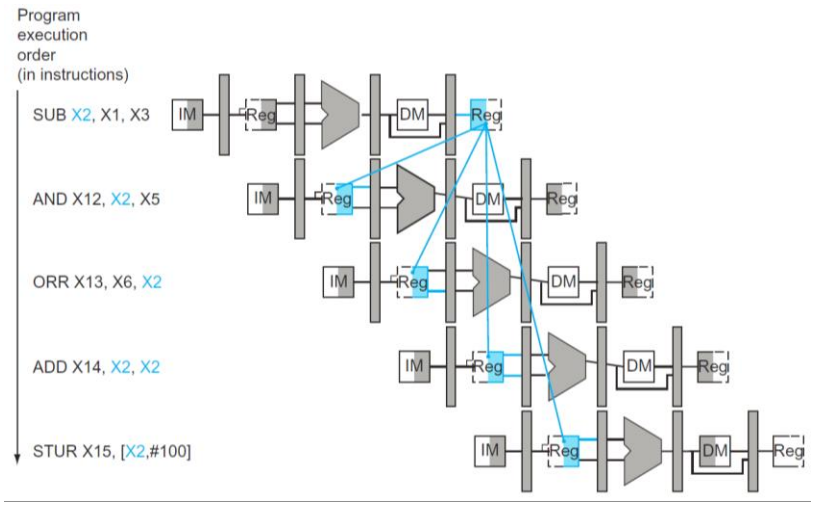
IF	ID	EX	MEM	WB
250 ps	350ps	150ps	300ps	200ps

(1) What is the clock cycle time in a pipelined and non-pipelined processor?
(2) What is the total latency of an LDUR instruction in a pipelined and non-pipelined processor?
(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

6. (6 points) ADDI X1, X2, #5
ADD X3, X1, X2
ADDI X4, X1, #15
ADD X5, X3, X2

Add NOP instructions to the code so that it will run correctly on a pipeline that does not have extra hardware to handle data hazards.

7. (13 points) (1) In the following figure, which instructions would cause data hazard and which would not? Explain the reason.
(2) Give two solutions to deal with the hazard.


Program
execution
order
(in instructions)
SUB X2, X1, X3
AND X12, X2, X5
ORR X13, X6, X2
ADD X14, X2, X2
STUR X15, [X2,#100]
IM
Reg
DM
Reg