

Chapter 6: Synchronous Sequential Circuits

- A State Diagram
- Synchronous Counter
- Finite State Machine
- Binary sequence detector
- State Encoding

- Today's lecture will be recorded and posted on Canvas.

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Announcement

- HW #5 due Friday (12/10).
- Please submit the online Course Evaluation

<https://unh.bluera.com/unh/>

• Final Exam 12/20 (Mon) 8am - 10am

Room: PCAC M223

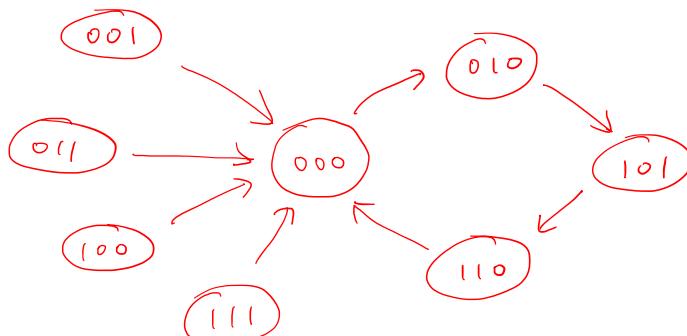
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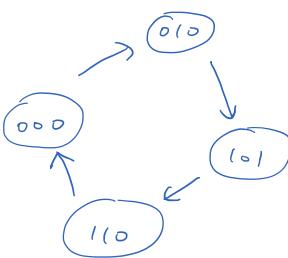
Part #1: Solve the following problems.**HW #5**

1. (a) Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.
- (b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares.

(a)

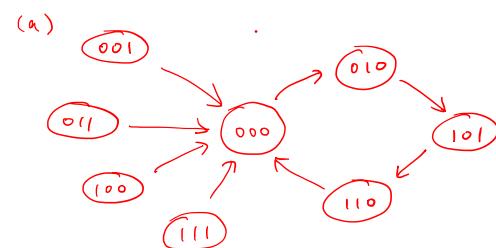


(b)

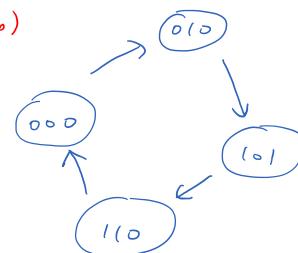


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HW #5

(b)



Present state	Next state	Needed (MSB)			CLS0		
		J ₂	K ₂	J ₁			
0 0 0	0 1 0	0	d	1	d	0	d
0 0 1	0 0 0	0	d	0	d	d	1
0 1 0	1 0 1	1	d	d	1	1	d
0 1 1	0 0 0	0	d	d	1	d	1
1 0 0	0 0 0	d	1	0	d	0	d
1 0 1	1 1 0	d	0	1	d	d	1
1 1 0	0 0 0	d	1	d	1	0	d
1 1 1	0 0 0	d	1	d	1	d	1

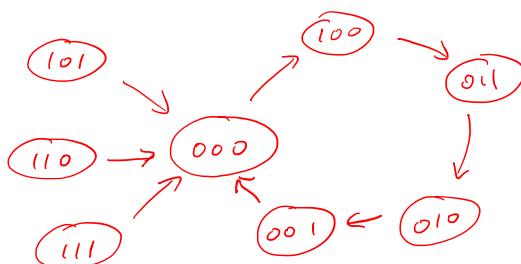
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HW #5

2. Design a synchronous, recycling, MOD-5 down counter that produces the sequence 100, 011, 010, 001, 000, and repeat. Use J-K flip-flops. Force the unused states to 000 on the next clock pulse.

$$\text{MOD-5} \rightarrow 4, 3, 2, 1, 0, 4, 3, \dots$$



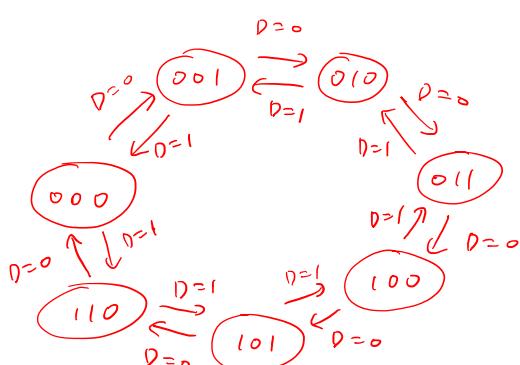
$Q_2 Q_1 Q_0$	$Q'_2 Q'_1 Q'_0$	J_2	K_2	J_1	K_1	J_0	K_0
0 0 0	1 0 0	1	d	0	d	0	d
0 0 1	0 0 0	0	d	0	d	d	1
0 1 0	0 0 1	0	d	d	1	1	d
0 1 1	0 1 0	0	d	d	0	d	1
1 0 0	0 1 1	d	1	1	d	1	d
1 0 1	0 0 0	d	1	0	d	d	1
1 1 0	0 0 0	d	1	d	1	0	d
1 1 1	0 0 0	d	1	d	1	d	1

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HW #5

3. Design a synchronous, recycling, MOD-7 up/down counter with J-K FFs. Use the states 000 through 110 in the counter. Control the count direction with input D (D = 0 to count up and D = 1 to count down).



D	$Q_2 Q_1 Q_0$	$Q'_2 Q'_1 Q'_0$	J_2	K_2	J_1	K_1	J_0	K_0
0	0 0 0	0 0 1	0	d	0	d	1	d
0	0 0 1	0 1 0	0	d	1	d	d	1
0	0 1 0	0 1 1	0	d	d	0	1	d
0	0 1 1	1 0 0	1	d	d	1	d	1
0	1 0 0	1 0 1	d	0	0	d	1	d
0	1 0 1	1 1 0	d	0	1	d	d	1
0	1 1 0	0 0 0	d	1	d	1	0	d
0	1 1 1	0 0 0	d	d	d	d	d	d
1	0 0 0	1 1 0	1	d	1	d	0	d
1	0 0 1	0 0 0	0	d	0	d	d	1
1	0 1 0	0 0 1	0	d	d	1	1	d
1	0 1 1	0 1 0	0	d	d	0	d	1
1	1 0 0	0 1 1	d	1	1	d	1	d
1	1 0 1	1 0 0	d	0	0	d	d	1
1	1 1 0	1 0 1	d	0	d	1	1	d
1	1 1 1	0 0 0	d	d	d	d	d	d

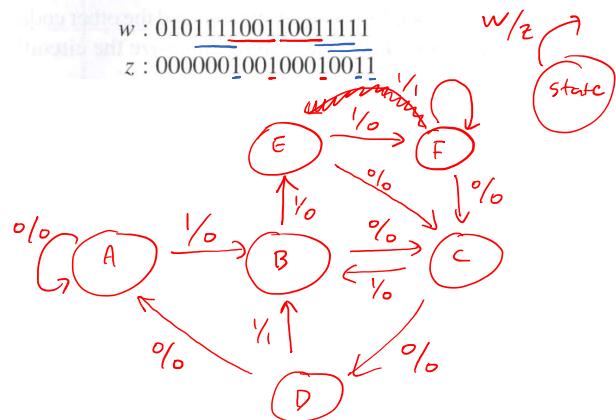
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HW #5**Part #2**

- 6.3** Derive the state diagram for an FSM that has an input w and an output z . The machine has to generate $z = 1$ when the previous four values of w were 1001 or 1111; otherwise, $z = 0$. Overlapping input patterns are allowed. An example of the desired behavior is

- A: 0 is received.
- B: 1 is received
- C: 10 is received
- D: 100 is received
- E: 11 is received
- F: 111 is received.



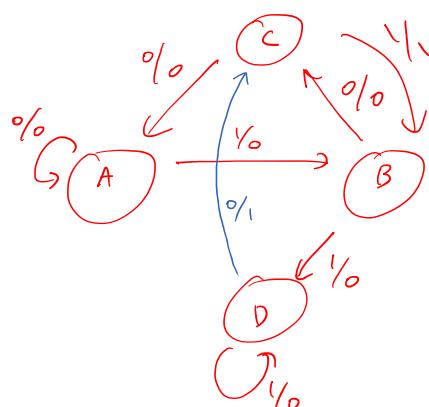
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HW #5

- *6.5** Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.

- A: 0 detected
- B: 1
- C: 10
- D: 11



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HW #5

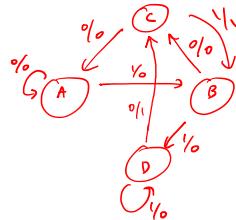
***6.5** Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.

A: 0 detected

B: 1

C: 10

D: 11



2 FFs needed.

Q_1, Q_0	state
0 0	A
0 1	B
1 0	C
1 1	D

input	present state	next state	output
w	Q_1, Q_0	Q'_1, Q'_0	Y
0	0 0	0 0	0
0	0 1	1 0	0
0	1 0	0 0	0
0	1 1	1 0	1
1	0 0	0 1	0
1	0 1	1 1	0
1	1 0	0 1	1
1	1 1	1 1	0

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HW #5

***6.15** Show a state table for the state-assigned table in Figure P6.1, using A, B, C, D for the four rows in the table. Give a new state-assigned table using a one-hot encoding. For A use the code $y_4y_3y_2y_1 = 0001$. For states B, C, D use the codes 0010, 0100, and 1000, respectively. Synthesize a circuit using D flip-flops.

Present state	Next state		Output z
	$w = 0$	$w = 1$	
y_2y_1	Y_2Y_1	Y_2Y_1	
A 00	C 10	D 11	0
B 01	B 01	A 00	0
C 10	D 11	A 00	0
D 11	C 10	B 01	1

present state	next state		output
	$w=0$	$w=1$	
A 0001	0100	1000	0
B 0010	0010	0001	0
C 0100	1000	0001	0
D 1000	0100	0010	1

→

1-hot encoding

$0\ 0\ 0\ 1 \rightarrow A$
$0\ 0\ 1\ 0 \rightarrow B$
$0\ 1\ 0\ 0 \rightarrow C$
$1\ 0\ 0\ 0 \rightarrow D$

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HW #5

***6.15** Show a state table for the state-assigned table in Figure P6.1, using A, B, C, D for the four rows in the table. Give a new state-assigned table using a one-hot encoding. For A use the code $y_4y_3y_2y_1 = 0001$. For states B, C, D use the codes 0010, 0100, and 1000, respectively. Synthesize a circuit using D flip-flops.

			present state	w=0	w=1	next state	output	1-hot encoding
A	C	D	A	0001	0100	1000	0	$0001 \rightarrow A$
B	B	A	B	0010	0010	0001	0	$0010 \rightarrow B$
C	D	A	C	0100	1000	0001	0	$0100 \rightarrow C$
D	C	B	D	1000	0100	0010	1	$1000 \rightarrow D$

w	Present $Q_3 Q_2 Q_1 Q_0$	Next $Q'_3 Q'_2 Q'_1 Q'_0$	Z	
0	0 0 0 1	0 1 0 0	0	$D_3 = Q'_3 = Q_2 \bar{W} + Q_0 W$
0	0 0 1 0	0 0 1 0	0	$D_2 = Q'_2 = Q_0 \bar{W} + Q_3 \bar{W}$
0	0 1 0 0	1 0 0 0	0	$D_1 = Q'_1 = Q_1 \bar{W} + Q_3 W$
0	1 0 0 0	0 1 0 0	1	$D_0 = Q'_0 = Q_1 W + Q_2 \bar{W}$
1	0 0 0 1	1 0 0 0	0	
1	0 0 1 0	0 0 0 1	0	
1	0 1 0 0	0 0 0 1	0	
1	1 0 0 0	0 0 1 0	1	

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