Lab 3

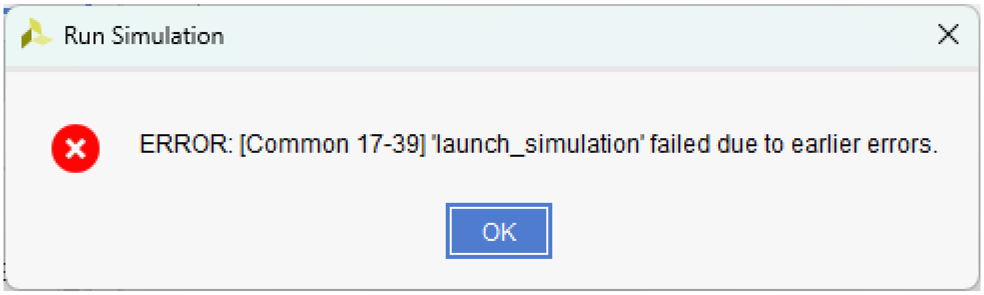
Source

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date: 03/09/2023 02:54:50 PM
// Design Name: 
// Module Name: main
// Project Name: 
// Target Devices: 
// Tool Versions: 
// Description: 
// 
// Dependencies: 
// 
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
// 
//////////////////////////////////////////////////////////////////////////////////


// Define a function to get the segment value for a given switch value
function [6:0] get_segment_value;
    input [3:0] switches;
    reg [6:0] segment;

    // Define named constants for anode select values
    parameter ANODE_SELECT_DIGIT_0 = 4'b1110;
    parameter ANODE_SELECT_DIGIT_1 = 4'b1101;
    parameter ANODE_SELECT_DIGIT_2 = 4'b1011;
    parameter ANODE_SELECT_DIGIT_3 = 4'b0111;

    // Define named constants for switch values
    parameter SWITCH_VALUE_ZERO  = 4'b0000;
    parameter SWITCH_VALUE_ONE   = 4'b0001;
    parameter SWITCH_VALUE_TWO   = 4'b0010;
    parameter SWITCH_VALUE_THREE = 4'b0011;
    parameter SWITCH_VALUE_FOUR  = 4'b0100;
    parameter SWITCH_VALUE_FIVE  = 4'b0101;
    parameter SWITCH_VALUE_SIX   = 4'b0110;
    parameter SWITCH_VALUE_SEVEN = 4'b0111;
    parameter SWITCH_VALUE_EIGHT = 4'b1000;
    parameter SWITCH_VALUE_NINE  = 4'b1001;

    // Define named constants for segment values
    parameter SEGMENT_VALUE_ZERO  = 7'b1000000;
    parameter SEGMENT_VALUE_ONE   = 7'b1111001;
    parameter SEGMENT_VALUE_TWO   = 7'b0100100;
    parameter SEGMENT_VALUE_THREE = 7'b0110000;
    parameter SEGMENT_VALUE_FOUR  = 7'b0011001;
    parameter SEGMENT_VALUE_FIVE  = 7'b0010010;
    parameter SEGMENT_VALUE_SIX   = 7'b0000010;
    parameter SEGMENT_VALUE_SEVEN = 7'b1111000;
    parameter SEGMENT_VALUE_EIGHT = 7'b0000000;
    parameter SEGMENT_VALUE_NINE  = 7'b0010000;
    begin
          // Use a case statement to determine the segment value for the
          // given switch value
        case (switches[3:0])
            SWITCH_VALUE_ZERO:  segment = SEGMENT_VALUE_ZERO;
            SWITCH_VALUE_ONE:   segment = SEGMENT_VALUE_ONE;
            SWITCH_VALUE_TWO:   segment = SEGMENT_VALUE_TWO;
            SWITCH_VALUE_THREE: segment = SEGMENT_VALUE_THREE;
            SWITCH_VALUE_FOUR:  segment = SEGMENT_VALUE_FOUR;
            SWITCH_VALUE_FIVE:  segment = SEGMENT_VALUE_FIVE;
            SWITCH_VALUE_SIX:   segment = SEGMENT_VALUE_SIX;
            SWITCH_VALUE_SEVEN: segment = SEGMENT_VALUE_SEVEN;
            SWITCH_VALUE_EIGHT: segment = SEGMENT_VALUE_EIGHT;
            SWITCH_VALUE_NINE:  segment = SEGMENT_VALUE_NINE;
            default:            segment = SEGMENT_VALUE_ZERO;
        endcase
        // Return the segment value
        get_segment_value = segment;
    end
endfunction

module main(segment, anode, switches, clk);

    // Define output signals
    output reg [6:0]segment;
    output reg [3:0]anode;

    // Define input signals
    input [15:0]switches;
    input clk;

    // Selecting between which digit/anode to refresh
    wire [1:0] digit_select;
    reg [19:0] refresh = 20'h00000;

    // Clock signal
    always @(posedge clk) begin
        refresh <= refresh + 1;
    end

    // Essentially a delay
    assign digit_select = refresh[19:18];

    // For the length of the program, the digit_select will direct
    // flow to refresh a digit/anode
    always @(posedge clk) begin
        case (digit_select)
            2'b00:
            begin
                // Refresh digit 0
                anode = 4'b1110;
                // Update segments
                // Digit 0 will be refreshed to reflect the positions
                // of the first four switches as encoded into decimal
                // numbers
                segment = get_segment_value(switches[3:0]);
            end
            2'b01:
            begin
                // Refresh digit 1
                anode = 4'b1101;
                // Update segments
                    // Digit 1 will be refreshed to reflect the positions
                // of the second four switches as encoded into decimal
                // numbers
                segment = get_segment_value(switches[7:4]);
            end
            2'b10:
            begin
                // Refresh digit 2
                anode = 4'b1011;
                // Update segments
                    // Digit 2 will be refreshed to reflect the positions
                // of the third four switches as encoded into decimal
                // numbers
                segment = get_segment_value(switches[11:8]);
            end
            2'b11:
            begin
                // Refresh digit 3
                anode = 4'b0111;
                // Update segments
                    // Digit 3 will be refreshed to reflect the positions
                // of the fourth four switches as encoded into decimal
                // numbers
                segment = get_segment_value(switches[15:12]);
            end
        endcase
    end
endmodule
```

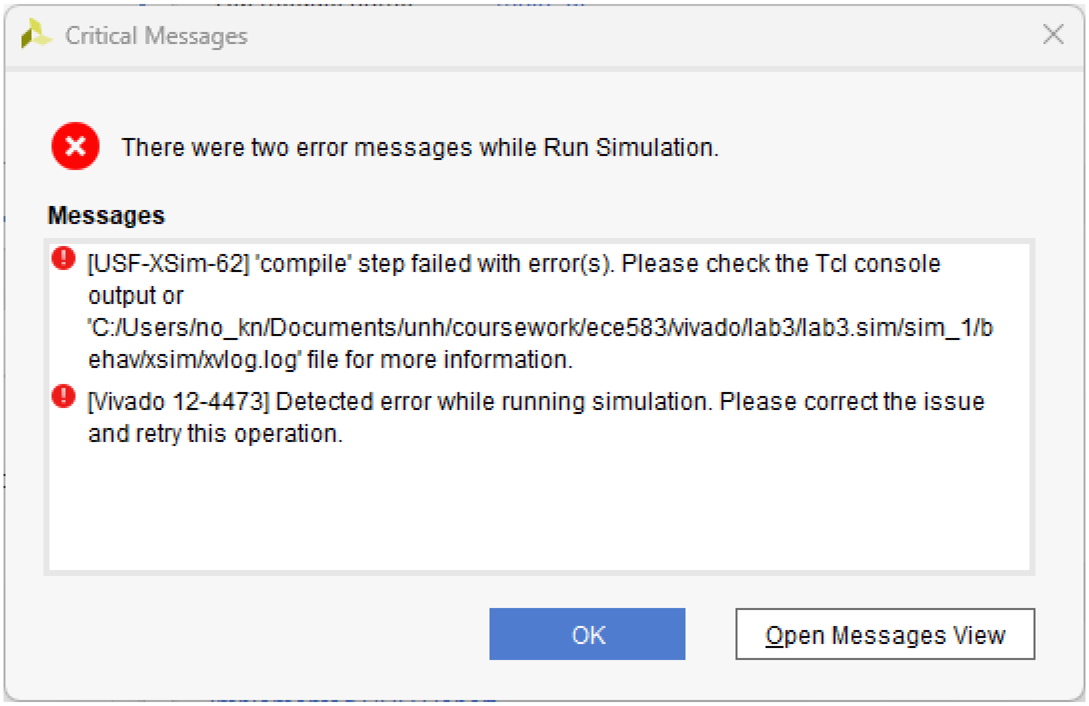
Simulation

I had a problem simulating So I have the errors here along with my testbench.

Error Messages



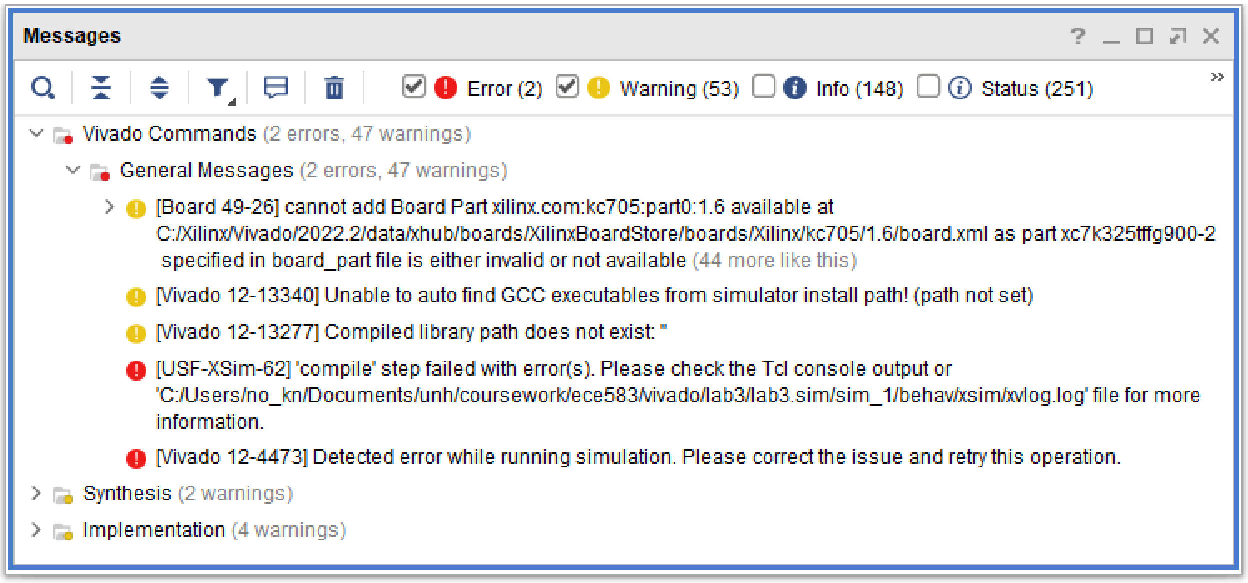
ERROR: [Common 17-39] 'launch_simulation' failed due to earlier errors.



There were two error messages while Run Simulation.

Messages

- [USF-XSim-62] 'compile' step failed with error(s). Please check the Tcl console output or 'C:/Users/no_kn/Documents/unh/coursework/ece583/vivado/lab3/lab3.sim/sim_1/behav/xsim/xvlog.log' file for more information.
- [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.



```
Vivado Commands (2 errors, 47 warnings)
    General Messages (2 errors, 47 warnings)
        [Board 49-26] cannot add Board Part xilinx.com:kc705:part0:1.6 available at
        C:/Xilinx/Vivado/2022.2/data/xhub/boards/XilinxBoardStore/boards/Xilinx/kc705/1.6/board.xml as part xc7k325tffg900-2
        specified in board_part file is either invalid or not available (44 more like this)
        [Vivado 12-13340] Unable to auto find GCC executables from simulator install path! (path not set)
        [Vivado 12-13277] Compiled library path does not exist: ''
        [USF-XSim-62] 'compile' step failed with error(s). Please check the Tcl console output or
        'C:/Users/no_kn/Documents/unh/coursework/ece583/vivado/lab3/lab3.sim/sim_1/behav/xsim/xvlog.log' file for more
        information.
        [Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.
Synthesis (2 warnings)
Implementation (4 warnings)
```

Testbench Source

```
`timescale 1ns/1ps

module main_tb;
    // Inputs
    reg [15:0] switches;
    reg clk;

    // Outputs
    wire [6:0] segment;
    wire [3:0] anode;

    // Instantiate the Unit Under Test (UUT)
    main uut (
        .segment(segment),
        .anode(anode),
        .switches(switches),
        .clk(clk)
    );

    initial begin
        // Initialize inputs
        switches = 16'b0;
        clk = 0;

        // Wait for the clock to start
        #5;

        // Set switches to a value to test display
        switches = 16'b0011000100100100;
        #50;

        // Toggle switches to test display update
        switches = 16'b0000111100001111;
        #50;
        switches = 16'b1111000011110000;
        #50;

        // Stop the clock and end the simulation
        clk = 0;
        #5;
        $finish;
    end

    always #10 clk = ~clk;

endmodule
```

Constraints

```
        set_property PACKAGE_PIN R2 [get_ports {switches[15]}]
        set_property PACKAGE_PIN T1 [get_ports {switches[14]}]
        set_property PACKAGE_PIN U1 [get_ports {switches[13]}]
        set_property PACKAGE_PIN W2 [get_ports {switches[12]}]
        set_property PACKAGE_PIN R3 [get_ports {switches[11]}]
        set_property PACKAGE_PIN T2 [get_ports {switches[10]}]
        set_property PACKAGE_PIN T3 [get_ports {switches[9]}]
        set_property PACKAGE_PIN V2 [get_ports {switches[8]}]
        set_property PACKAGE_PIN W13 [get_ports {switches[7]}]
        set_property PACKAGE_PIN W14 [get_ports {switches[6]}]
        set_property PACKAGE_PIN V15 [get_ports {switches[5]}]
        set_property PACKAGE_PIN W15 [get_ports {switches[4]}]
        set_property PACKAGE_PIN W17 [get_ports {switches[3]}]
        set_property PACKAGE_PIN W16 [get_ports {switches[2]}]
        set_property PACKAGE_PIN V16 [get_ports {switches[1]}]
        set_property PACKAGE_PIN V17 [get_ports {switches[0]}]
        set_property PACKAGE_PIN W7 [get_ports {segment[0]}]
        set_property PACKAGE_PIN W6 [get_ports {segment[1]}]
        set_property PACKAGE_PIN U8 [get_ports {segment[2]}]
        set_property PACKAGE_PIN V8 [get_ports {segment[3]}]
        set_property PACKAGE_PIN U5 [get_ports {segment[4]}]
        set_property PACKAGE_PIN V5 [get_ports {segment[5]}]
        set_property PACKAGE_PIN U7 [get_ports {segment[6]}]
        set_property PACKAGE_PIN U2 [get_ports {anode[0]}]
        set_property PACKAGE_PIN U4 [get_ports {anode[1]}]
        set_property PACKAGE_PIN V4 [get_ports {anode[2]}]
        set_property PACKAGE_PIN W4 [get_ports {anode[3]}]
```

```
set_property PACKAGE_PIN W5 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports {anode[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {segment[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[15]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[14]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[13]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[12]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[11]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[10]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[9]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[8]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {switches[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports clk]
```