ECE 548: Electronic Design I

Lab 5: Three-Terminal Devices – MOSFETs

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Objective:

- To understand and experimentally determine the I-V characteristics of an n-channel MOSFET.
- To build and understand the operation of a CMOS (Complementary MOSFET) logic inverter.

1. N-channel MOSFET (NMOS)

- Assemble the circuit in Figure 1(a) using a 2N7000 n-channel MOSFET. Use channel 1 of the DC supply to power V_{GS} and channel 2 for V_{DD}.
- For a fixed value of V_{GS}, adjust the V_{DD} value until the desired V_{DS} is obtained in order to measure the current (I_D) through the MOSFET. Use the table below.

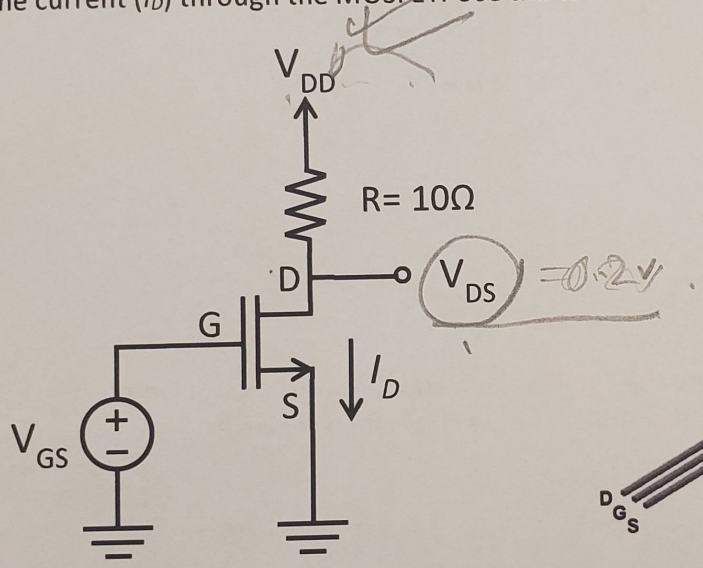
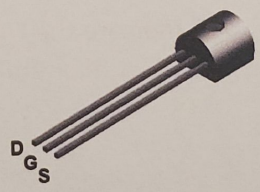


Figure 1(a)

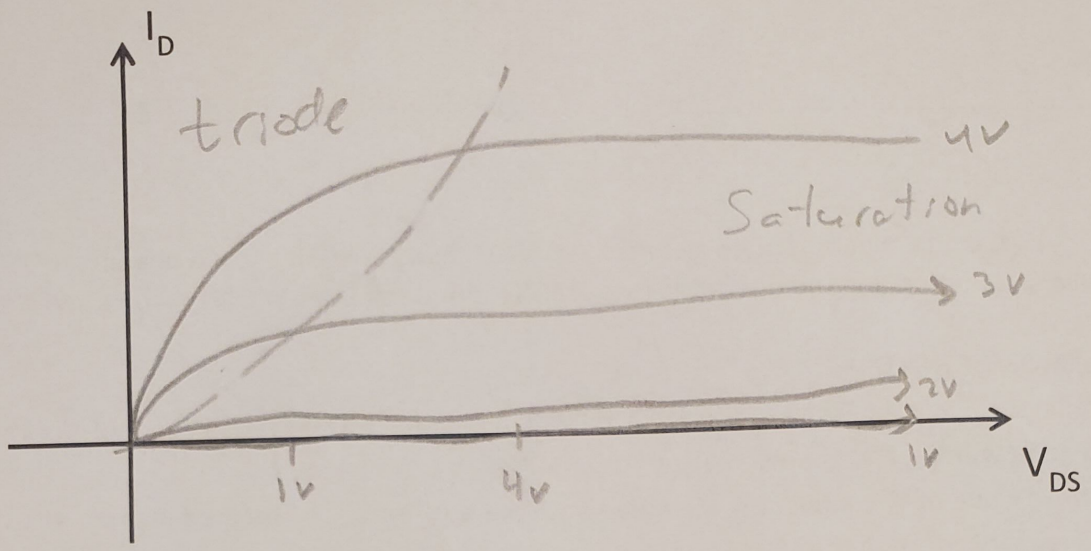


Top view

Figure 1(b)

	V_{DS} = 0.2V		V_{DS} = 0.5V		V_{DS} = 1V		V_{DS} = 1.5V		V_{DS} = 2V	
	V_{DD}	I_D	V_{DD}	I_D	V_{DD}	I_D	V_{DD}	I_D	V_{DD}	I_D
V_{GS} = 1V	0.44	0.024	0.86	0.038	1.42	0.043	1.5	0	2	0
V_{GS} = 2V	0.71	0.052	1.64	0.116	2.76	0.181	1.5	0.099	2	0.098
V_{GS} = 3V	0.83	0.063	2.02	0.154	3.65	0.189	2.05	0.055	2.53	0.053
V_{GS} = 4V	0.90	0.71	2.08	0.163	3.25	0.225	4.28	0.282	5.04	0.309

- Plot I_D vs. V_{DS} for V_{GS} = 1V, 2V, 3V, and 4V.



- What is the estimated threshold voltage (V_t) of the NMOS?

0.6V

- Based on the estimated V_{TN}, indicate the triode region and the saturation region on the graph above (use a dotted line to draw the boundary between the two regions).

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2. **CMOS Logic Inverter**

- Construct the circuit in Figure 2 below using the NMOS (2N7000) and the PMOS (TP0606). Note that Figure 1(b) applies to both NMOS and PMOS transistors.

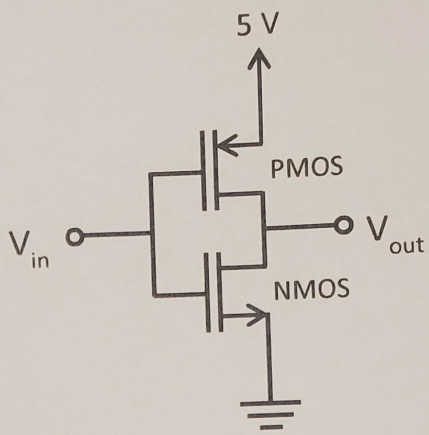
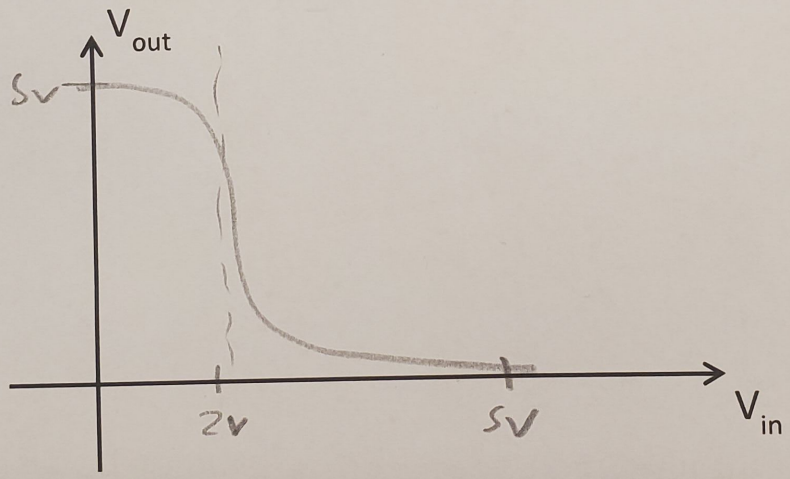


Figure 2

- Complete the following table by varying the input voltage V_{in} from 0 V to 5 V.

V_{in}	0V	0.5V	1V	1.5V	2V	2.5V	3V	3.5V	4V	4.5V	5V
V_{out}	5	5	5	5	5	4.89	4.79	4.60	4.30	4.19	4.18

- Using the data from the above table, plot the voltage transfer characteristics (V_{out} vs. V_{in}) in the axes provided below.



- What is the estimated threshold voltage for the logic inverter?

$V_T = 2v$

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