Lab 4: Design Of An XOR Logic Gate

ECE715: Introduction To VLSI

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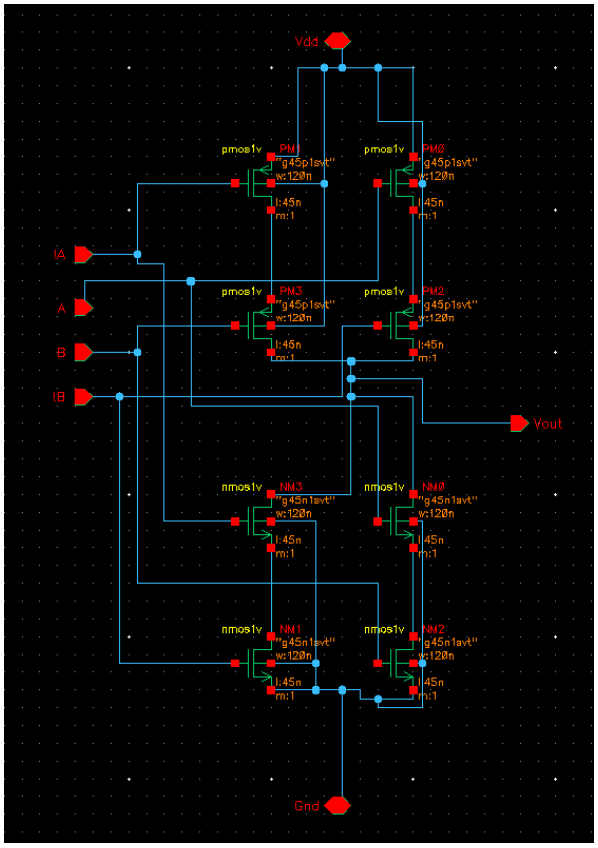
Due Date: 12/11/2023

Background

The culmination of all lab assignments arrives with designing and analyzing an XOR gate using both CMOS and transmission gate technology. This lab assignment gives students the chance to test their knowledge of the course's material in totality. From the schematic, symbol, transient analysis, all the way to the layout and various check tests. This final lab allows students to perfect their implementation skills in the Cadence Virtuoso environment in preparation of their larger scale final project. The XOR gate is one of the fundamental logic gates that students learn about and a perfect way to test knowledge of VLSI.

Lab Tasks

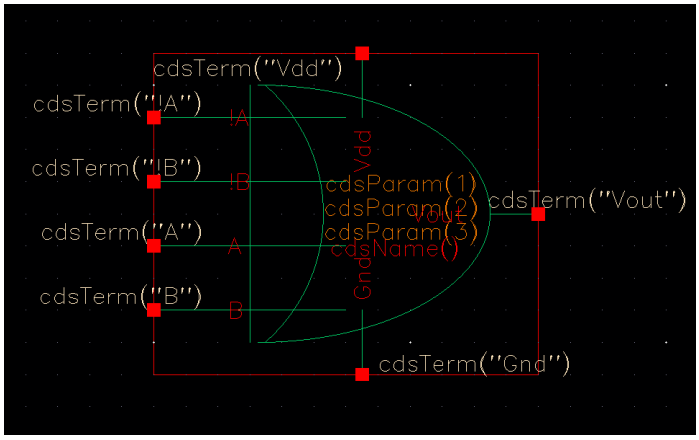
Task 1: XOR Gate Schematic



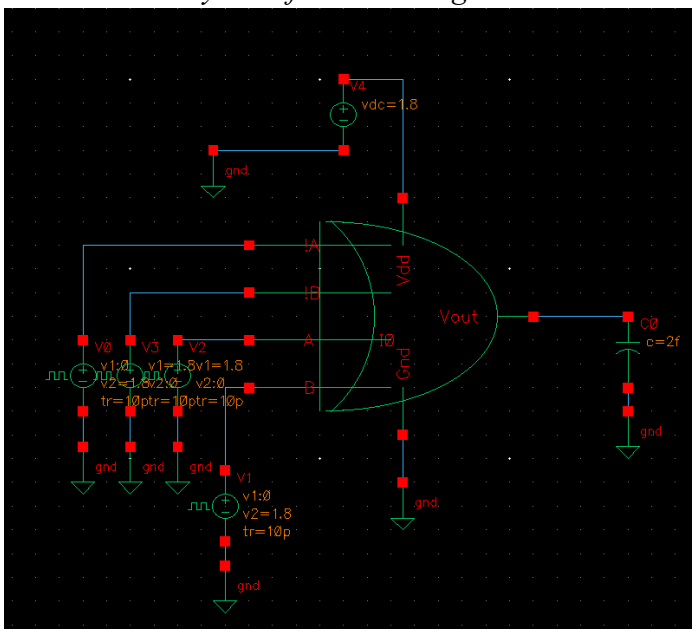
This schematic implements the XOR logic gate with four inputs, a singular output, and pins for both ground and Vdd. The pins for the inverted A and B inputs were used to prevent

extraneous delays due to the use of inverters. The bodies of the NMOS' are all grounded while the bodies of the PMOS' are all connected to Vdd to preemptively prevent DRC and LVS errors.

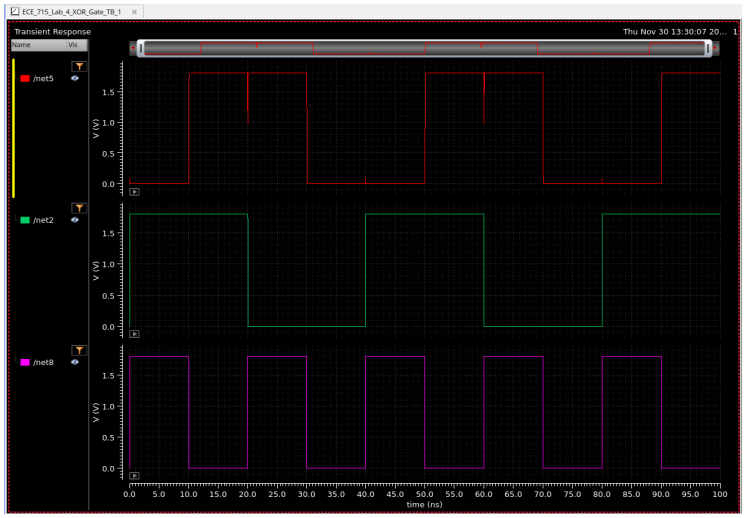
Task 2: XOR Gate Symbol | Transient Simulation



Symbol for the XOR gate



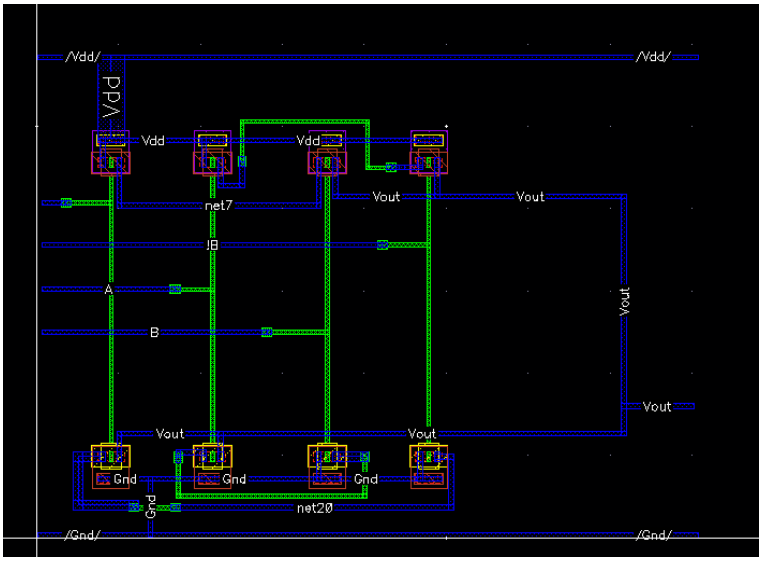
Testbench for transient analysis of the XOR gate



Waveform produced by the XOR gate testbench using transient analysis

This analysis of the original circuit is conducted by using two voltage pulses that have different periods. The bottom signal acts as the base for the above one which has a period that is twice the size of the first. This allows for all possible outputs to be present in the Vout signal and check if they all line up with the truth table of an XOR gate.

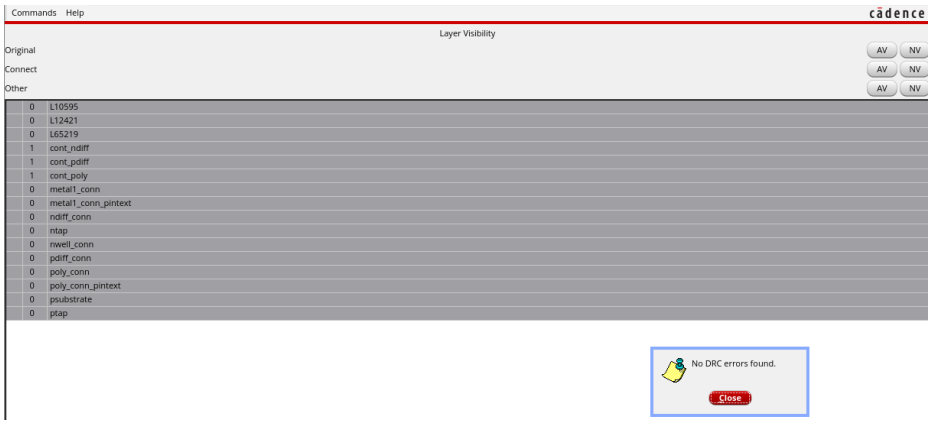
Task 3: Design Layout



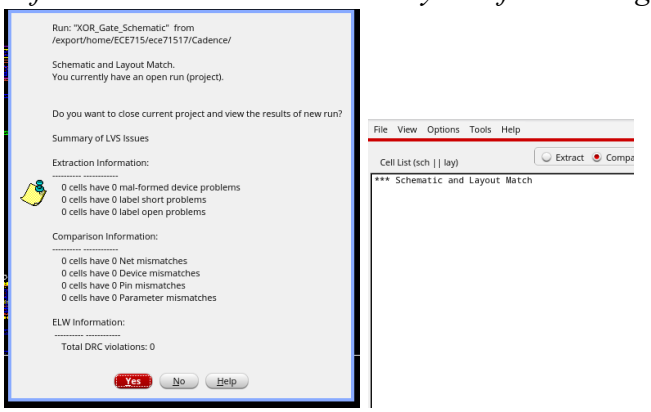
Layout for the XOR gate based off the schematic using the format of a stick diagram

This was a vastly different and more complex layout than the previous assignments although, with the use of strategically using vias to pass over metal materials with poly materials that would otherwise connect, this layout was able to be completed effectively.

Task 4: DRC, LVS



Result from the DRC check on the Layout of the XOR gate



Result from the LVS check on the Layout of the XOR gate

All of the DRC and LVS checks ran smoothly after a couple of errors that had to be fixed that involved various spacing issues in the layout. The QRC check is not included in this section and will be fully shown in totality in the *Time Differences* section. Overall the DRC was the check that had more errors as the LVS fully passed on the first run.

Task 5: Time Differences

riseTime(VT("/net5") 0 nil 1.8 nil 10 ...

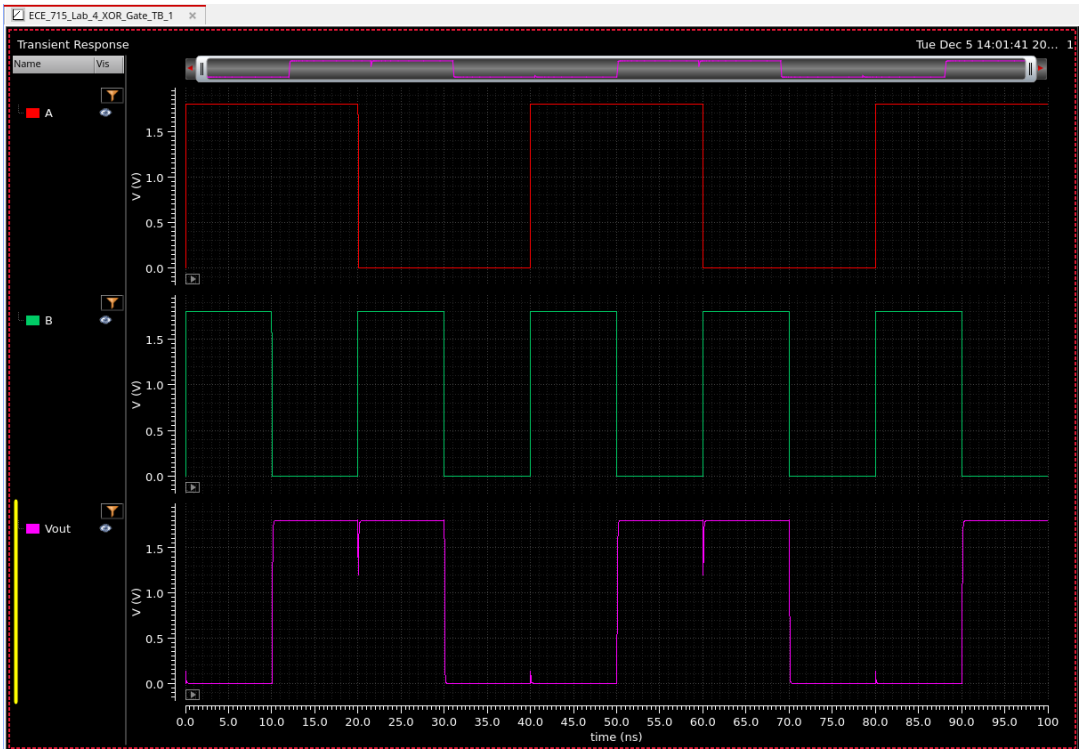
	time (s)	riseTime...me") (s)
1	10.02E-9	72.96E-12
2	50.02E-9	72.98E-12
3	90.02E-9	72.98E-12

TPLH for XOR_TB without capacitances from QRC

fallTime(VT("/net5") 1.8 nil 0 nil 10 9...

	time (s)	fallTime(...ime") (s)
1	30.02E-9	47.89E-12
2	70.02E-9	47.90E-12

TPHL for XOR_TB without capacitances from QRC



Waveform including QRC capacitances and resistances

10.03E-9	126.6E-12
50.03E-9	126.1E-12
90.03E-9	126.1E-12

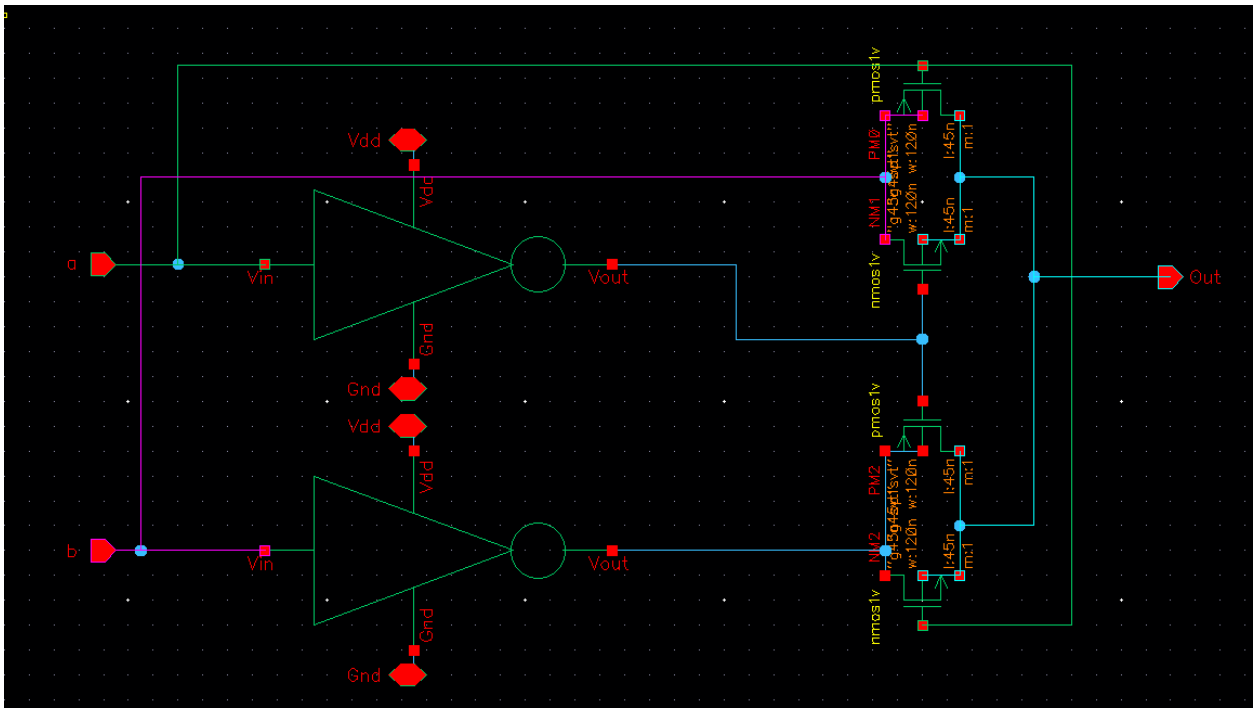
TPLH values including QRC capacitances and resistances

1	30.03E-9	85.61E-12
2	70.03E-9	85.61E-12

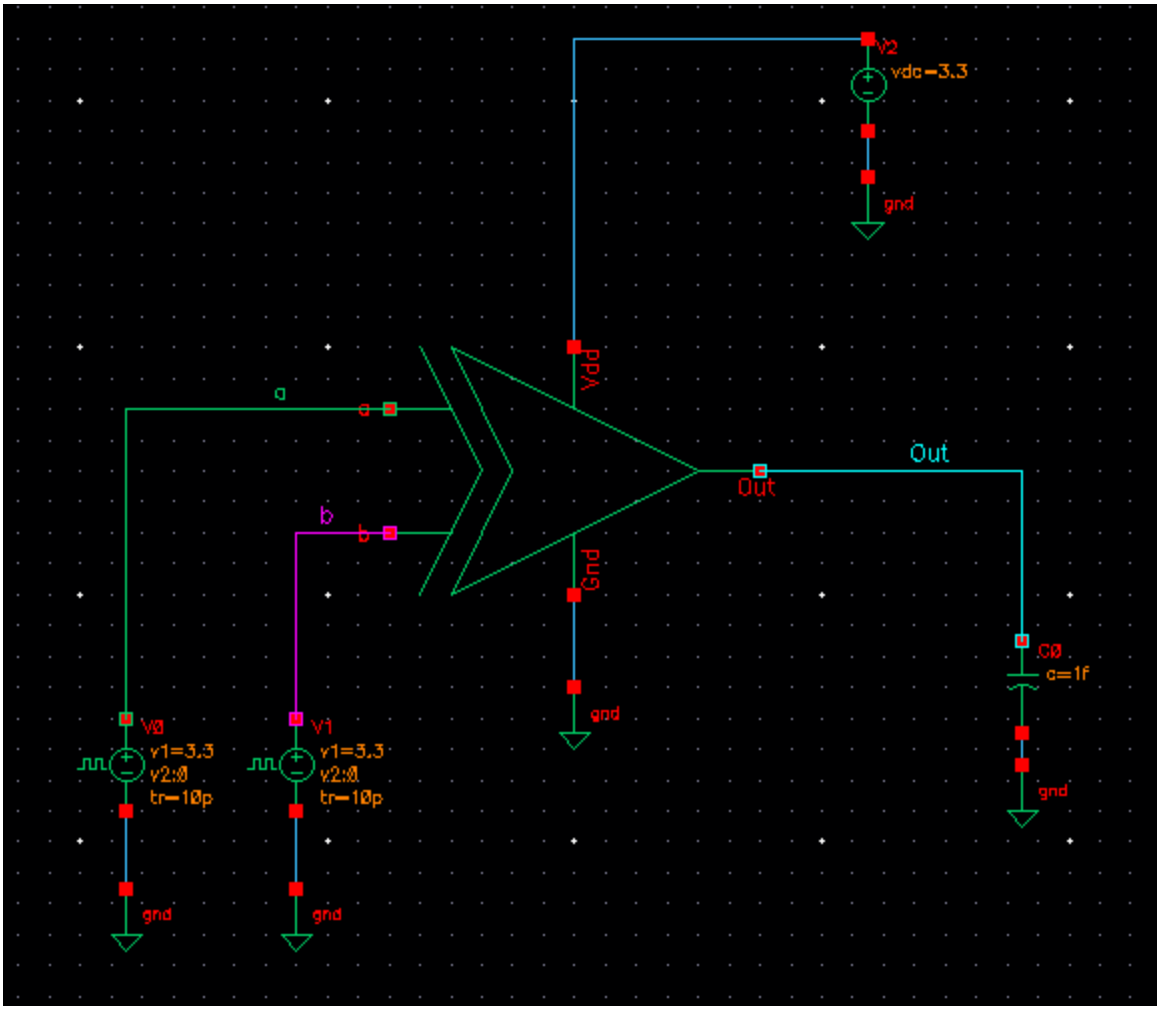
TPHL values including QRC capacitances and resistances

There is a pretty big difference between the time delays between the QRC values and non QRC values. The difference the realistic capacitances and resistances makes is quite substantial. For the TPLH there is a difference of *53.64* picoseconds while the difference for the TPHL is *37.715* picoseconds. In addition to the time differences there are spikes in the center of the Vout signal when B switches from low to high. This can be attributed to the switching of the inputs which allows a quick spike in the output. This can be solved by a small delay in the input switching.

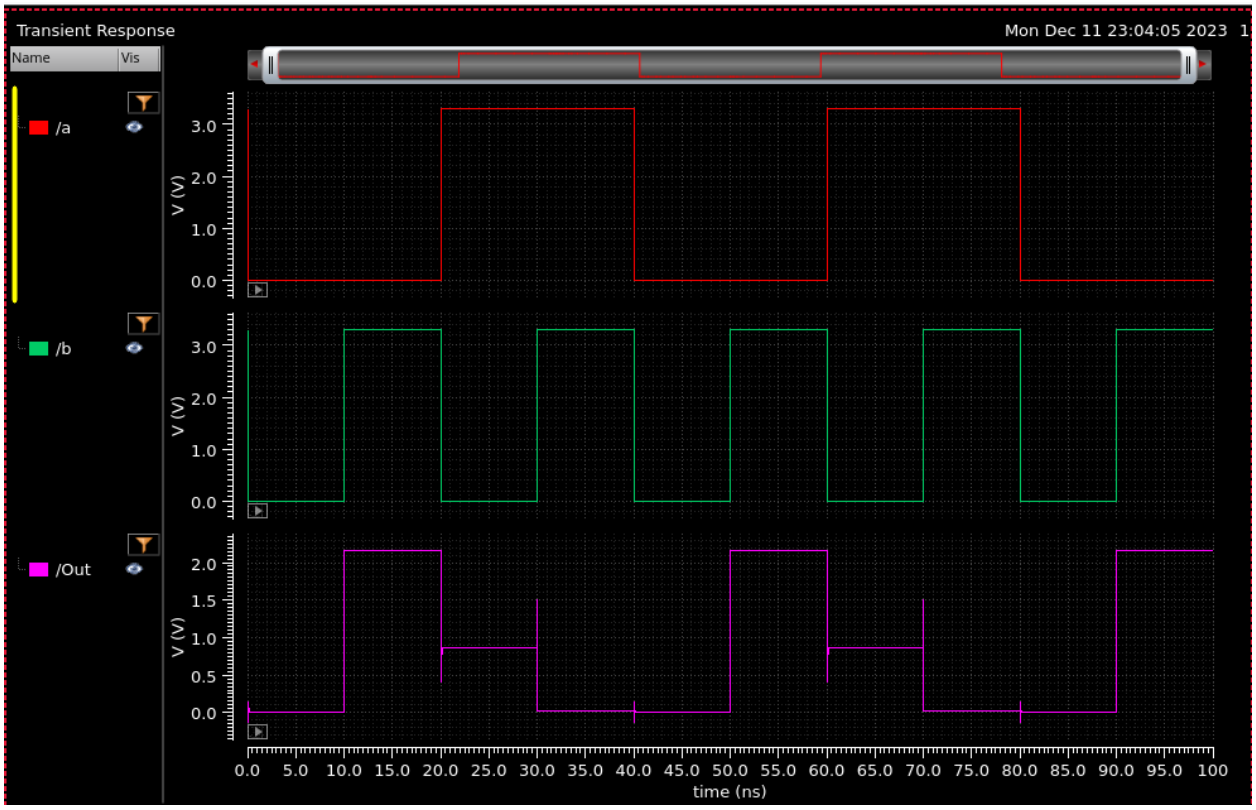
Task 6: Transmission Gate XOR Gate Schematic and Simulation



XOR Gate using Transmission Gate. The inverters were made in CMOS



Simulated testbench for XOR gate



Plotted results for inputs and outputs of XOR gate

Challenges

Andrew: The challenges that Andrew encountered centered around the DRC check within the layout. This layout was more challenging than the previous one, but allowed for a chance to test skills using the various strategies to complete a complex design. Eventually after many trials and errors the DRC check did pass without errors.

Nick: The challenges Nick encountered were from achieving a correct waveform when plotting the XOR gate using TG. The error probably stems from an incorrect schematic from the XOR gate. This error prevented the rise and fall times to be calculated as the calculations start from 3.3v which /Out never reached.

Contributions

Andrew: Andrew conducted the tasks that were involved with making a regular CMOS schematic, layout, and eventually QRC simulation.

Nick: Nick contributed by conducting the extra credit task.

Conclusion

This lab provided students with an opportunity to show their experience with all topics covered within the Cadence Virtuoso software throughout the semester. Starting with the schematic, moving to the symbol, and finally the layout with DRC, LVS, and QRC checks. In addition this lab gave students a chance to test their knowledge of the use of transmission gates as an alternative to CMOS technology.