Homework 2

Constraints

```
set_property IOSTANDARD LVCMOS33 [get_ports {in[9]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[8]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {in[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {out[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {out[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {out[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {out[0]}]
set_property PACKAGE_PIN V19 [get_ports {out[3]}]
set_property PACKAGE_PIN U19 [get_ports {out[2]}]
set_property PACKAGE_PIN E19 [get_ports {out[1]}]
set_property PACKAGE_PIN U16 [get_ports {out[0]}]
set_property PACKAGE_PIN V16 [get_ports {in[1]}]
set_property PACKAGE_PIN W16 [get_ports {in[2]}]
set_property PACKAGE_PIN W17 [get_ports {in[3]}]
set_property PACKAGE_PIN W15 [get_ports {in[4]}]
set_property PACKAGE_PIN V15 [get_ports {in[5]}]
set_property PACKAGE_PIN W14 [get_ports {in[6]}]
set_property PACKAGE_PIN W13 [get_ports {in[7]}]
set_property PACKAGE_PIN V2 [get_ports {in[8]}]
set_property PACKAGE_PIN T3 [get_ports {in[9]}]
```

Behavioral

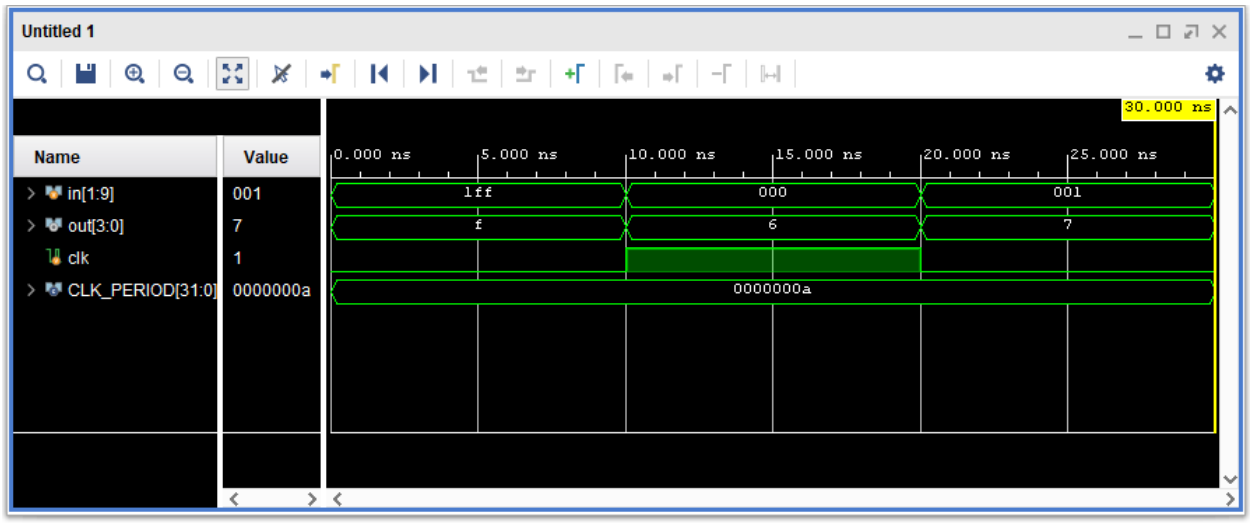
Source

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/23/2023 4:40:31 PM
// Design Name:
// Module Name: behavioral
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module behavioral(in, out);
    input [1:9] in;
    output reg [3:0] out;
```

```
    always @(*) begin
        casez(in)
            9'b????????0: out = 4'b0110;
            9'b???????01: out = 4'b0111;
            9'b??????011: out = 4'b1000;
            9'b?????0111: out = 4'b1001;
            9'b????01111: out = 4'b1010;
            9'b???011111: out = 4'b1011;
            9'b??0111111: out = 4'b1100;
            9'b?01111111: out = 4'b1101;
            9'b011111111: out = 4'b1110;
                9'b111111111: out = 4'b1111;
            default: out = 4'b0000;
        endcase
    end
endmodule
```

Simulation



Dataflow

Source

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 03/23/2023 10:03:40 PM
// Design Name:
// Module Name: dataflow
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
```

```
module dataflow(in, out);
    input [1:9] in;
    output reg [3:0] out;

    always @(*) begin
        out[3] = (in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[4] & in[3] & in[2] & in[1]) |
                 (~in[3] & in[2] & in[1]);

        out[2] = (in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[2] & in[1]) |
                 (~in[1]);

        out[1] = (in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[2] & in[1]) |
                 (~in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[1]) |
                 (~in[6] & in[5] & in[4] & in[3] & in[2] & in[1]);

        out[0] = (in[9] & in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[2] & in[1]) |
                 (~in[4] & in[3] & in[2] & in[1]) |
                 (~in[8] & in[7] & in[6] & in[5] & in[4] & in[3] & in[2] & in[1]) |
                 (~in[6] & in[5] & in[4] & in[3] & in[2] & in[1]);
    end
endmodule
```

Simulation