Lab 2: Simulation Of An Inverter

ECE715: Introduction To VLSI

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Prepared For: Dr. MD Shaad Mahmud

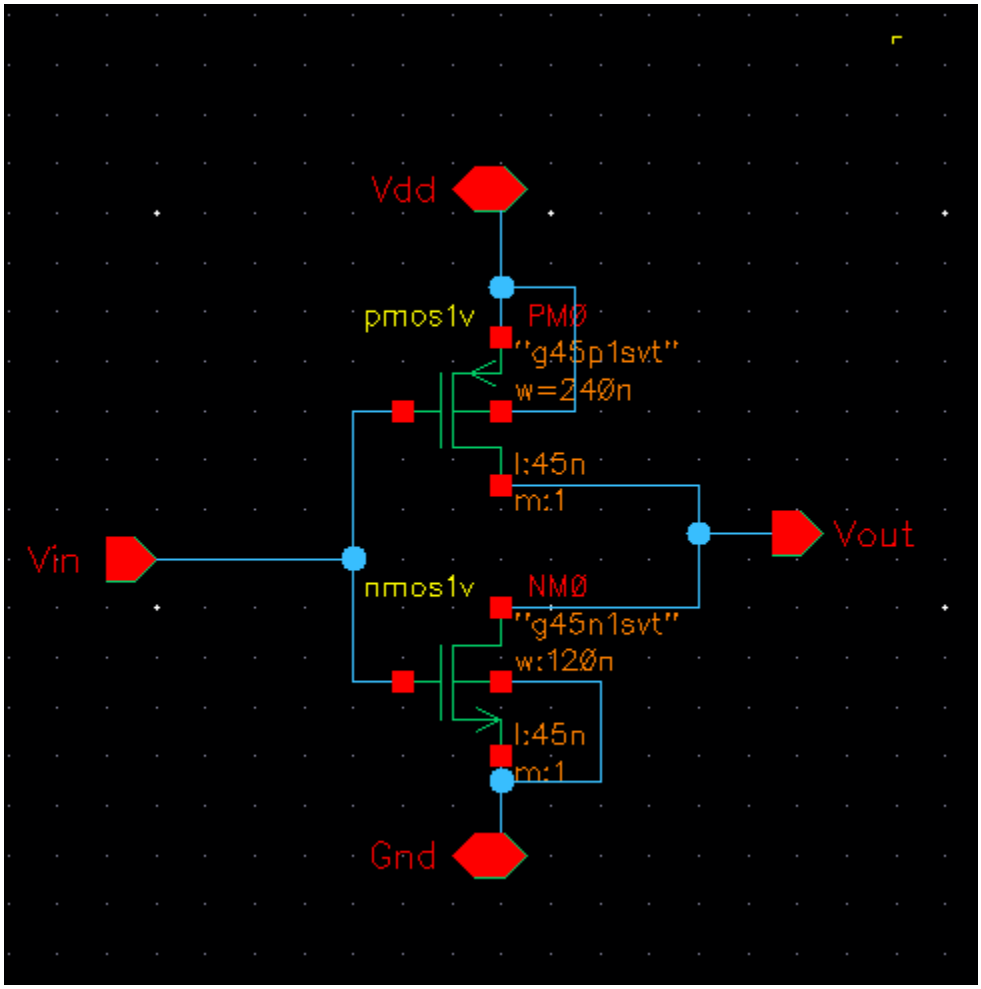
Due Date: 10/16/2023

Background

The main objective of this lab is to familiarize students with the symbol mechanic within the Virtuoso software. Students will create a CMOS inverter and use a symbol of said inverter within a test bench circuit. Students will then perform various analysis operations on the test bench circuit that involves the rising and falling time of the inverter, a parametric analysis of the width of the PMOS within the inverter, as well as various plotting analysis actions on the circuit. This lab report is split into two sections where each student conducted the lab in totality on their own and submitted their results here to compare accuracy.

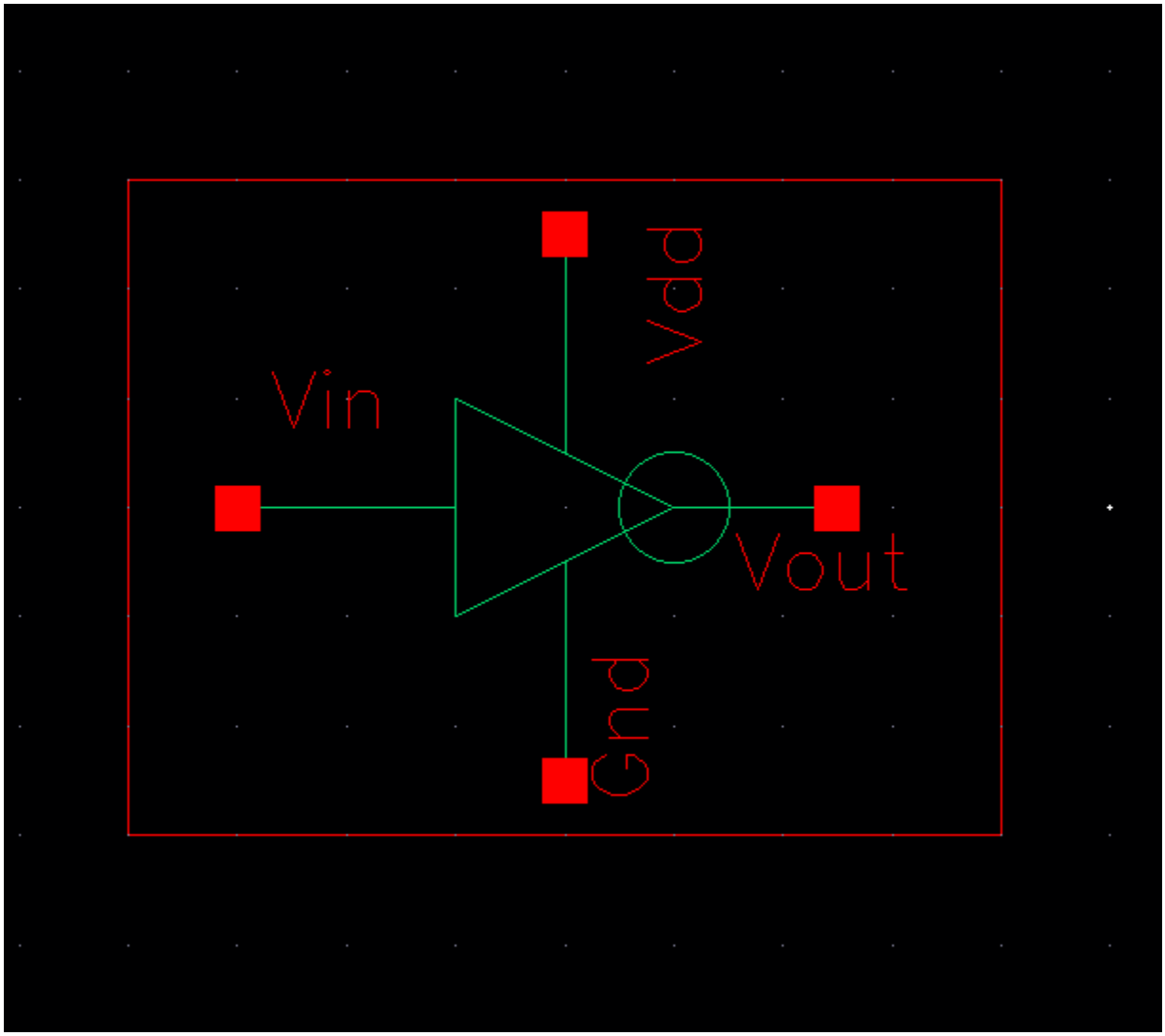
Andrew

Task 1:

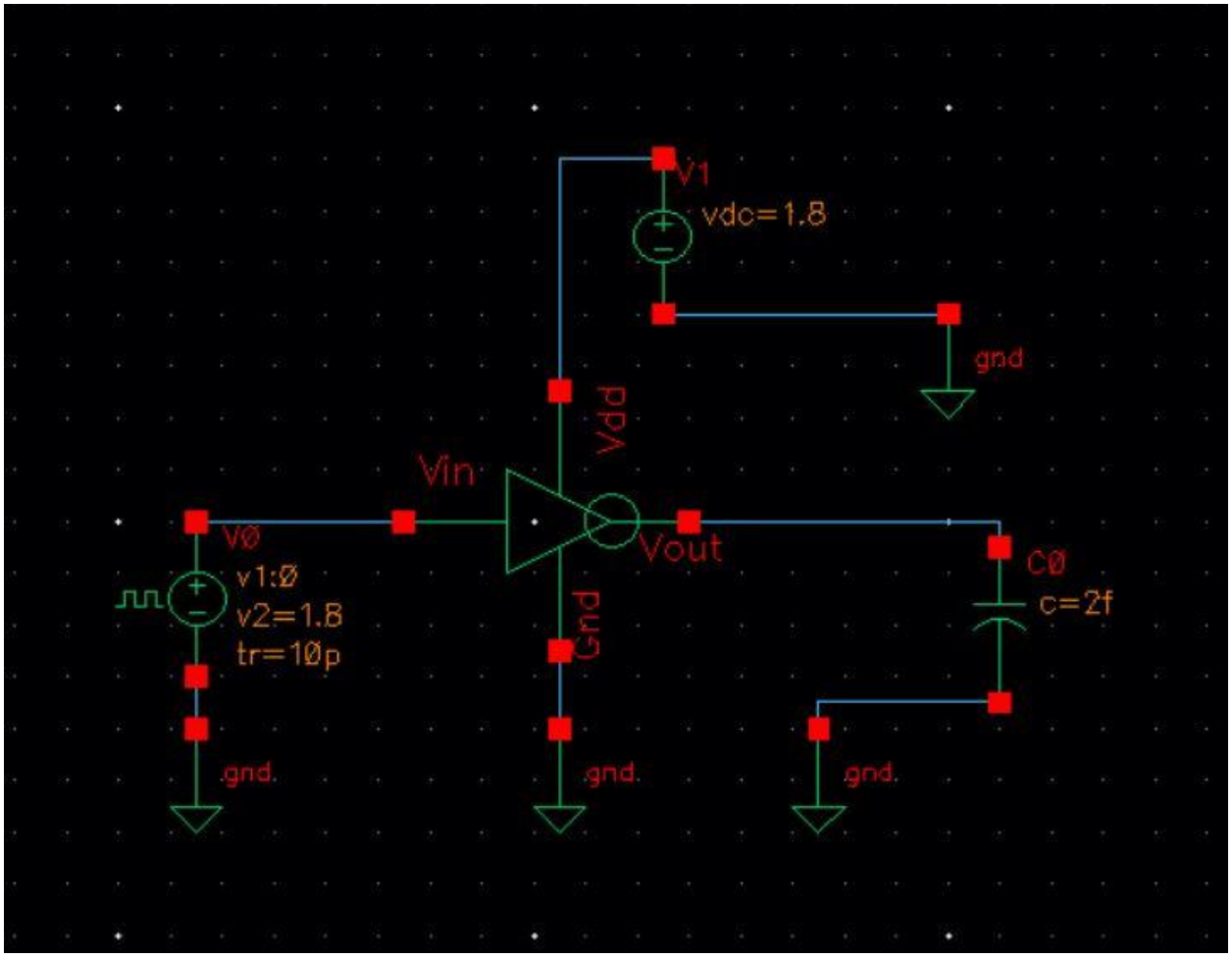


This diagram above shows the CMOS circuit design for an inverter where the pulse voltage goes in through “Vin” on the left side and then is filtered through the NMOS and PMOS system which determines how the inversion will look when coming out of the circuit. If the input is a low voltage Vdd will then go through to Vout, and if the input is a high voltage the PMOS will be cut off grounding Vout.

Task 2:

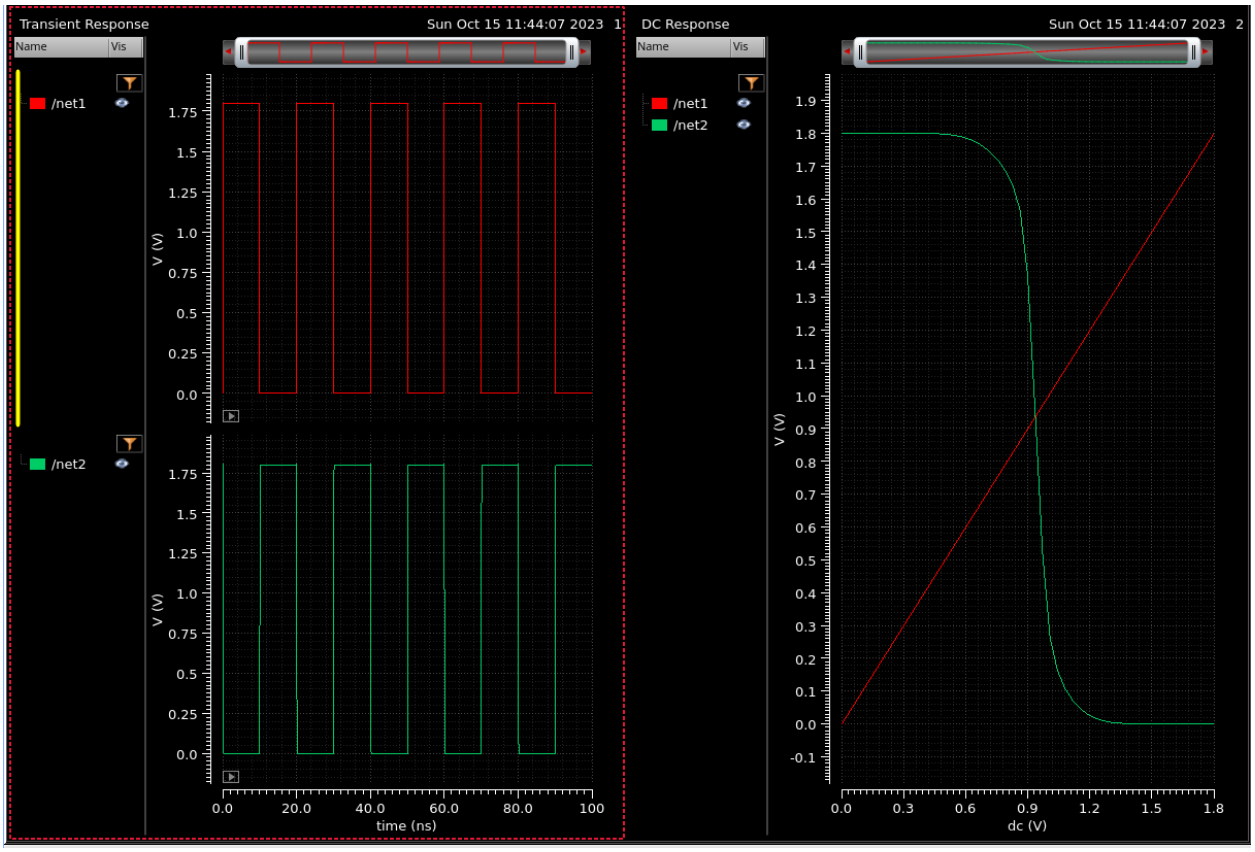


This is a simple symbol diagram of the inverter circuit from task one has all the needed inputs and outputs. Vdd and Gnd are input/output pins while Vin is an input and Vout is an output.



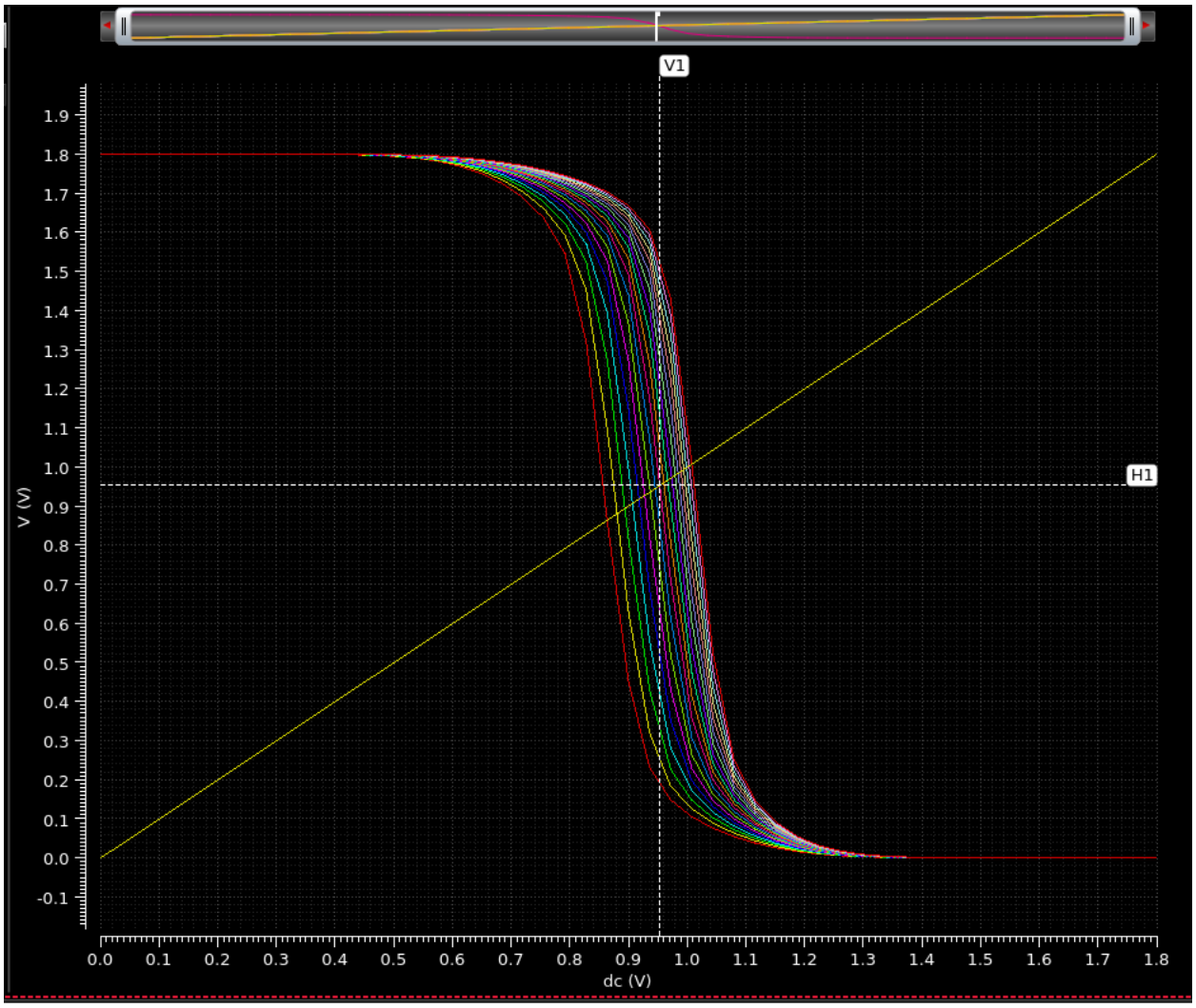
This second diagram shows the final test bench circuit design featuring the Vdd (vdc=1.8), Vin (Vpulse), Ground, and capacitor with a value of 2 femto-farads. This is the circuit used for all testing going forward.

Task 3:

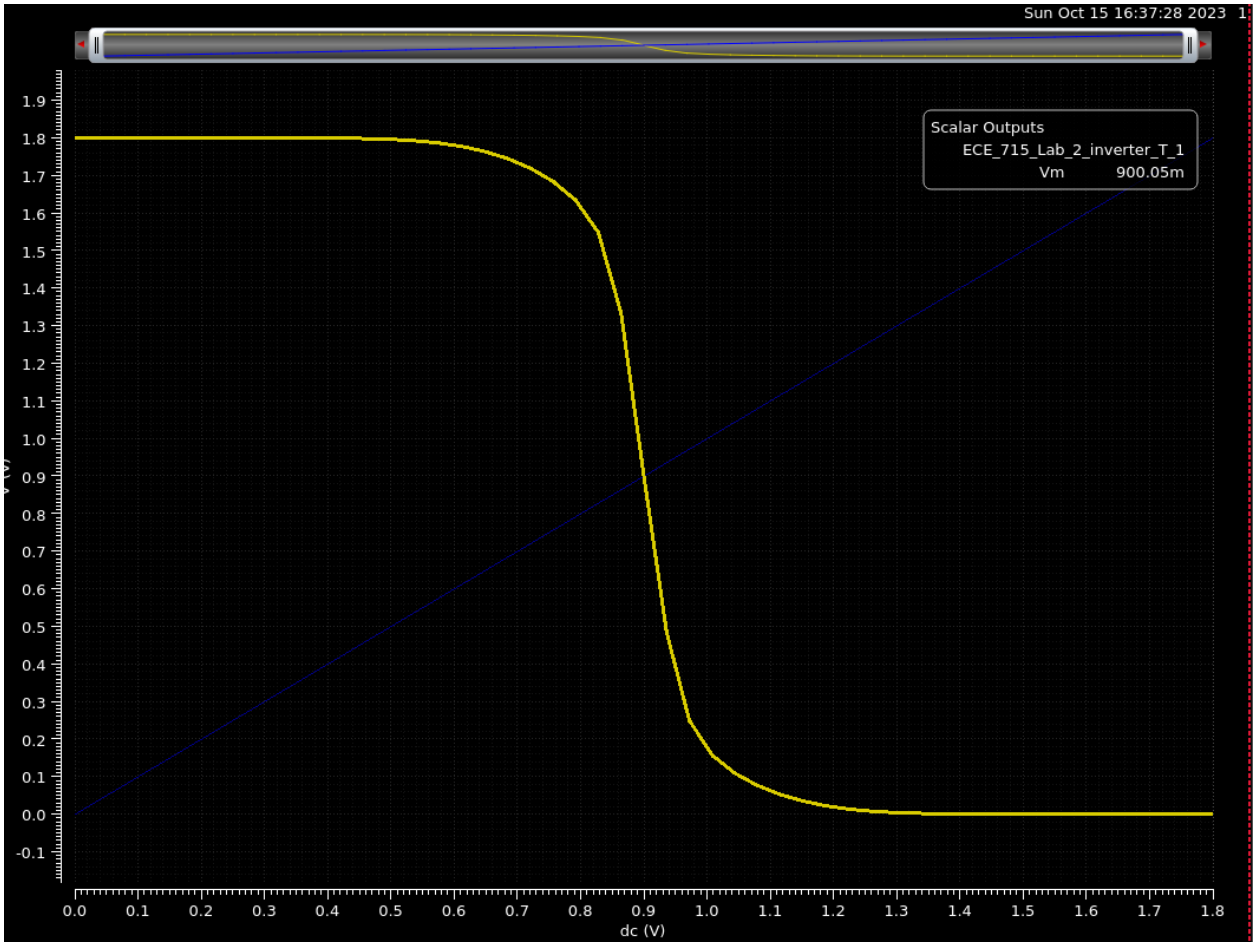


The above graph has three portions showing various aspects of the test bench circuit being tested. The top left plot is the waveform for the incoming pulsating voltage that goes from zero to one point eight volts. Below that is the inverted signal produced by the inverter by taking the incoming signal. The graph on the right side shows the curves of the voltages in and out and shows the midpoint voltage where the two curves intersect (approximately 900mv).

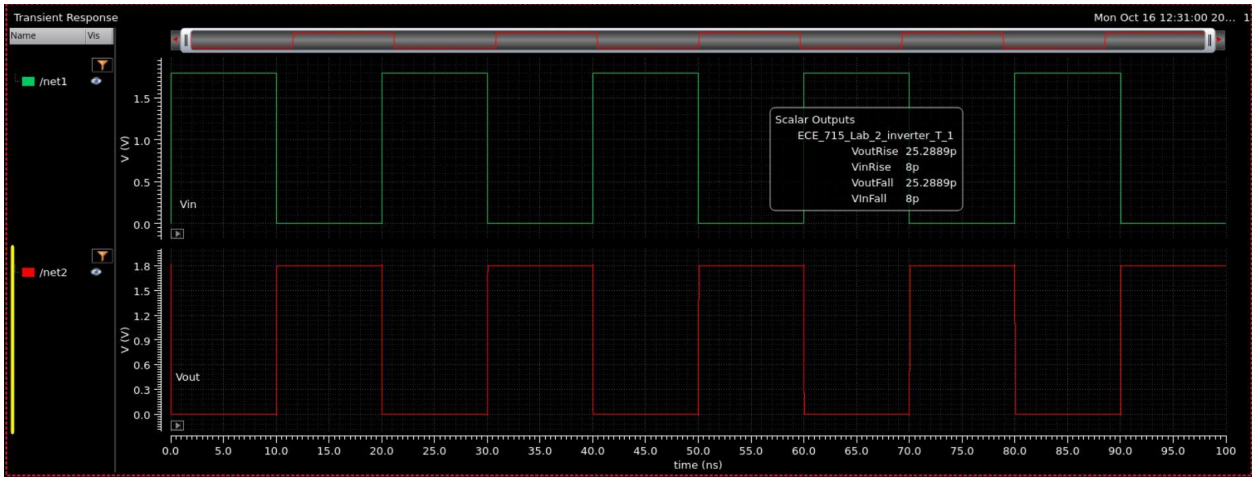
Task 4:



This plot shows the parametric analysis of the width within the PMOS of the inverter. The width of the PMOS sweeps from 120n to 480n in 20 n increments. This allows for analysis of what width would allow for most accurate analysis. The plot below shows the plot of the ideal value of the width for the PMOS which was also found within class to be 169.1847n in this scenario.


Sun Oct 15 16:37:28 2023
Scalar Outputs
ECE_715_Lab_2_inverter_T_1
Vm 900.05m
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8
dc (V)

Task 5:



This plot shows the two waveforms that were shown earlier for Vin and Vout showing the changes in "logic" values. In addition this plot also shows four values describing the rise/fall delays for both the input and output signals. The rise and fall per signal are both the same which makes sense as it is the same distance for said signal. Although between the two, there is a decently significant delay going from input to output. This can be mostly attributed to the capacitance of the capacitor on the output of the inverter as when this capacitance was raised from 2 femto-farads to 10 femto-farads the rise and fall times of the output exceed 100 nano-seconds.

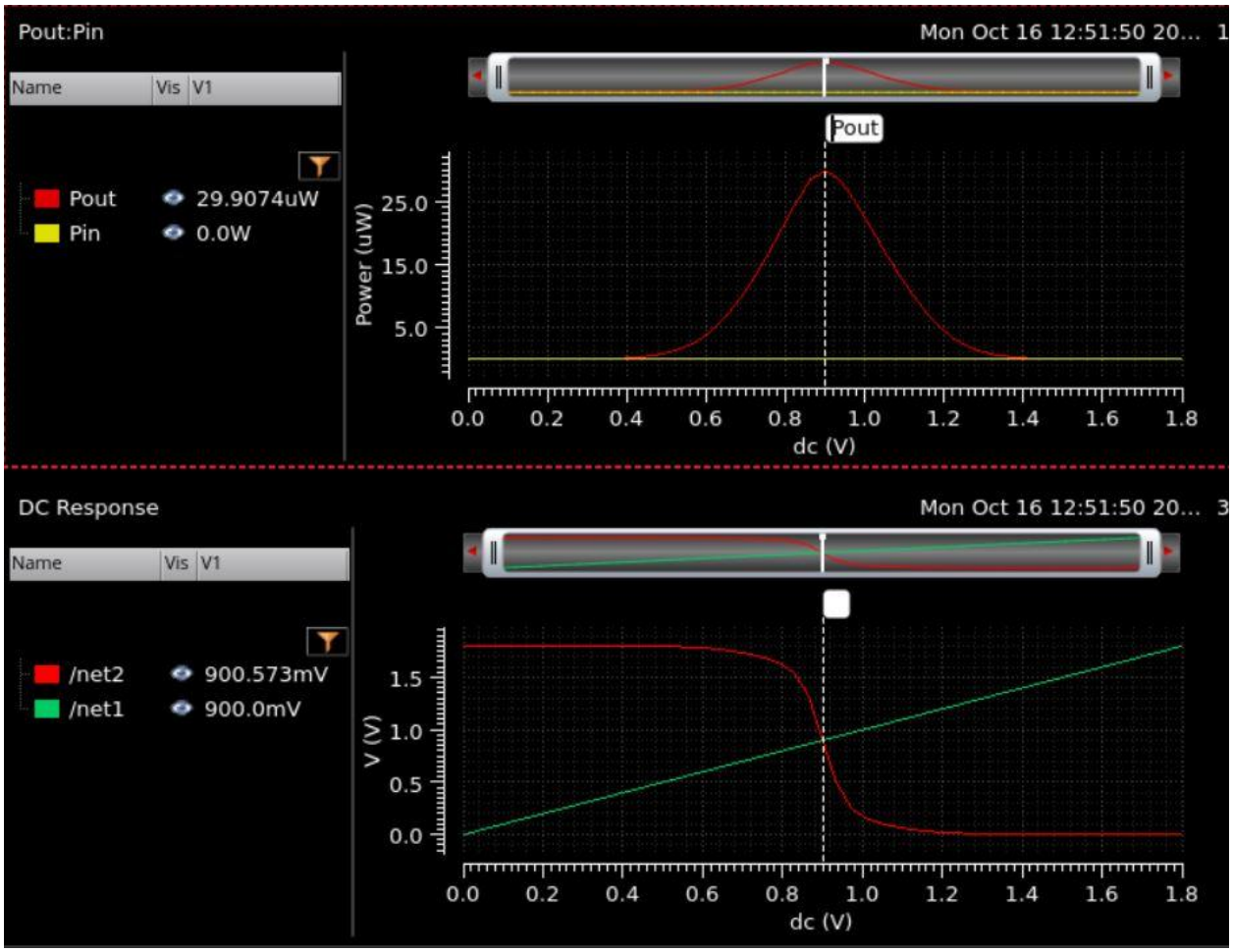
Rise Times:

$$Vin = 8\,picoseconds,\ Vout = 25.2889\,picoseconds$$

Fall Times:

$$Vin = 8\,picoseconds,\ Vout = 25.2889\,picoseconds$$

Task 6:



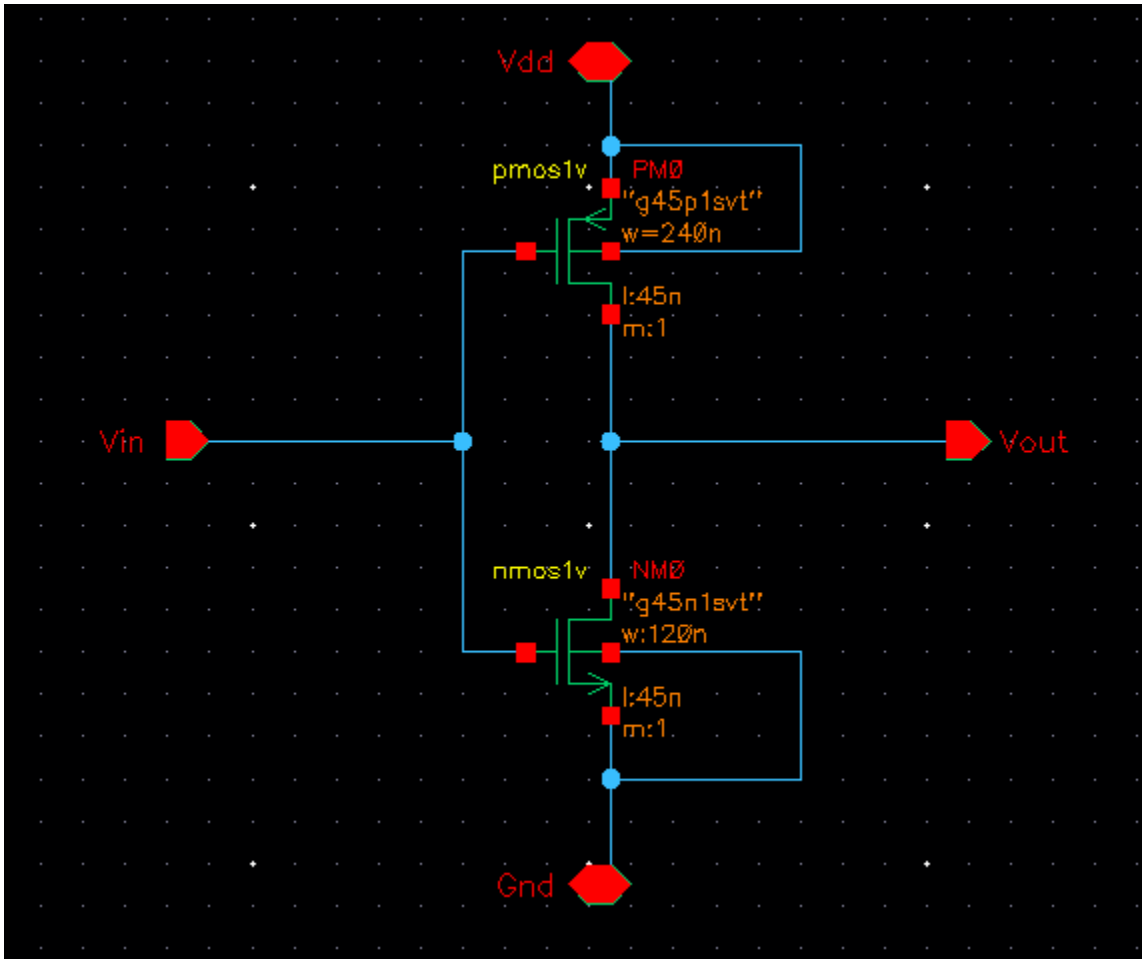
Total Power:

$29.9074\mu W$

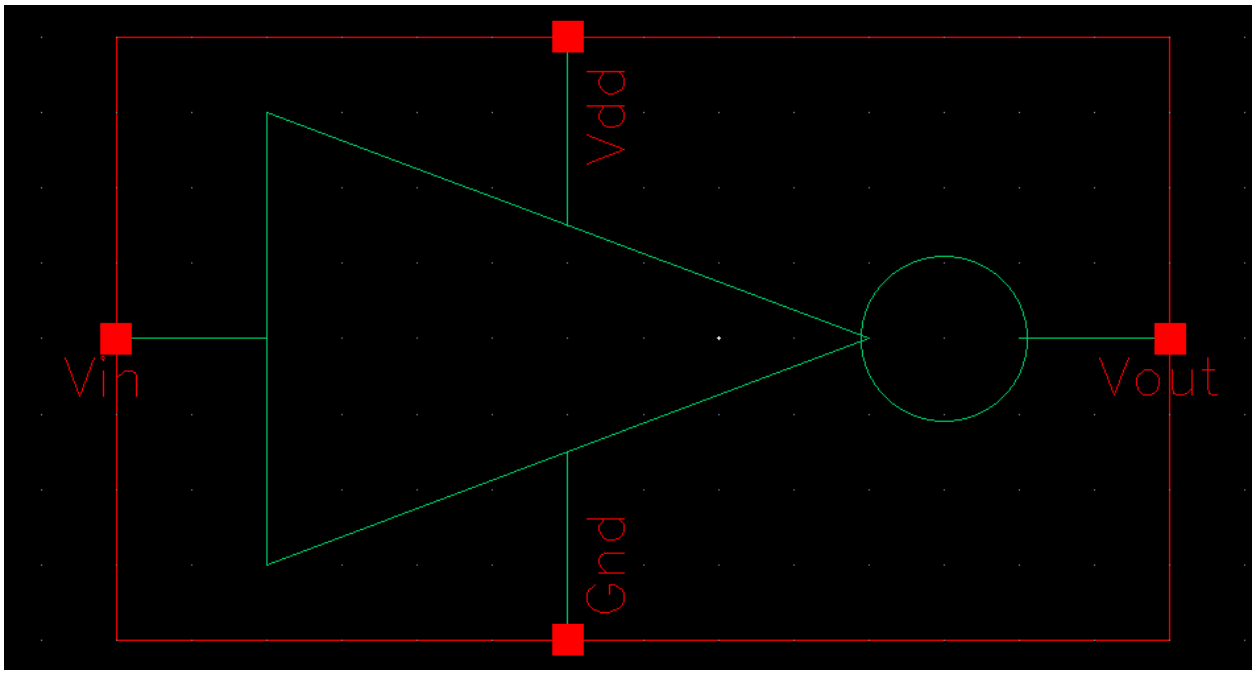
The total power shown in the plot above shows where the power level peaks fully right at the midpoint which makes sense. This calculation was found by using the built in calculator tool in Virtuoso and using the power spectrogram function specifically. The current chosen was from the top of the PMOS which ran down to the NMOS while the voltage chosen was the output voltage. This specific plot is shown in the Pout plot which is shown in red above. Pin can be seen in yellow on that plot which is a straight zero watts which does check out as no power is dissipated from just the input voltage alone.

Nick

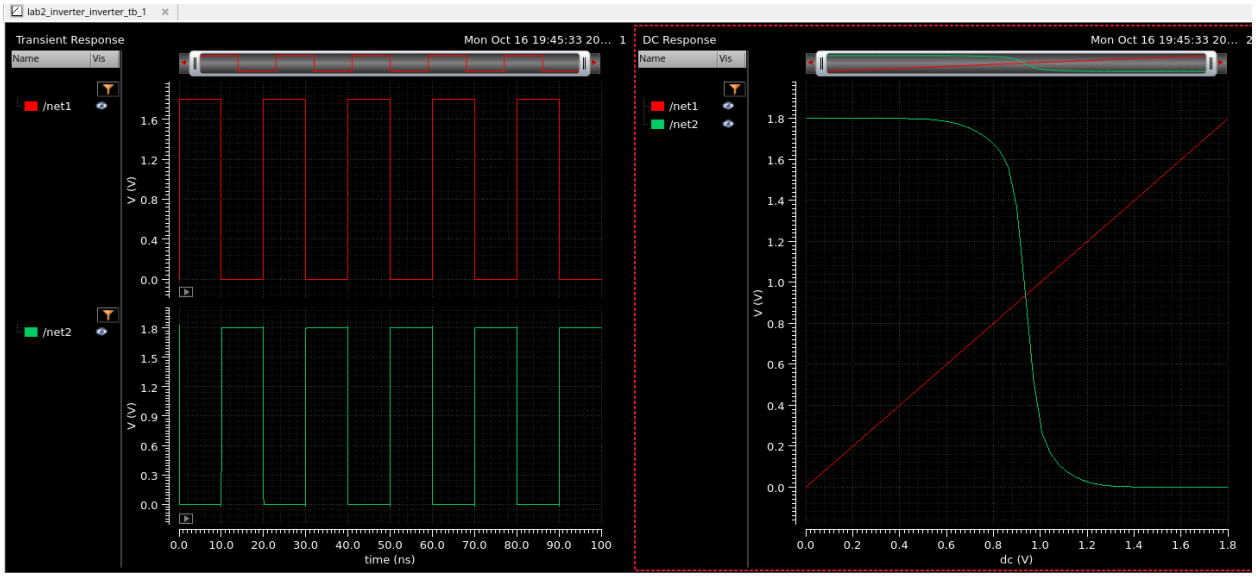
Task 1:


Vdd
pmos1v
PM0
"g45p1svt"
w=240n
l:45n
m:1
Vin
Vout
nmos1v
NM0
"g45n1svt"
w:120n
l:45n
m:1
Gnd

Task 2:

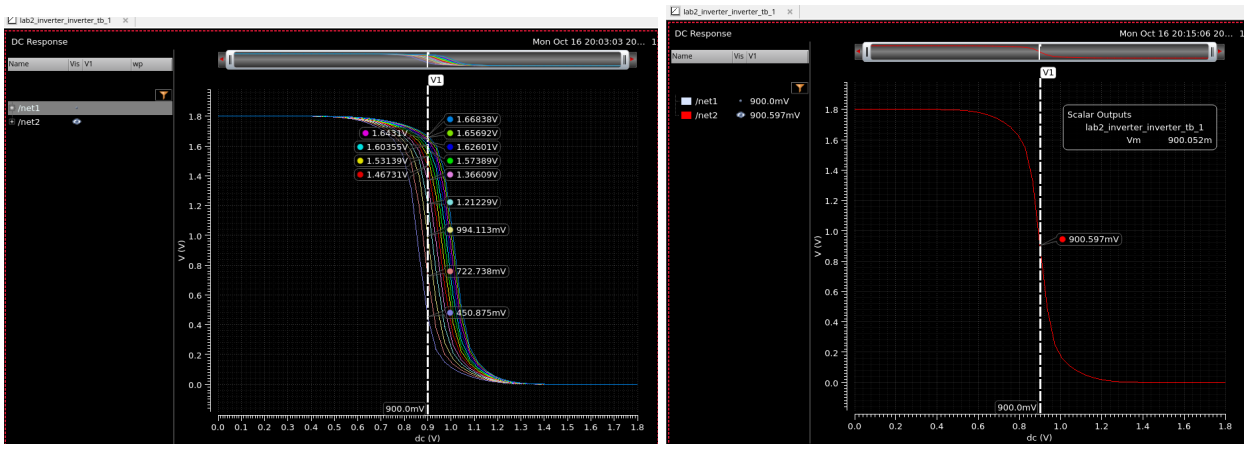


Task 3:



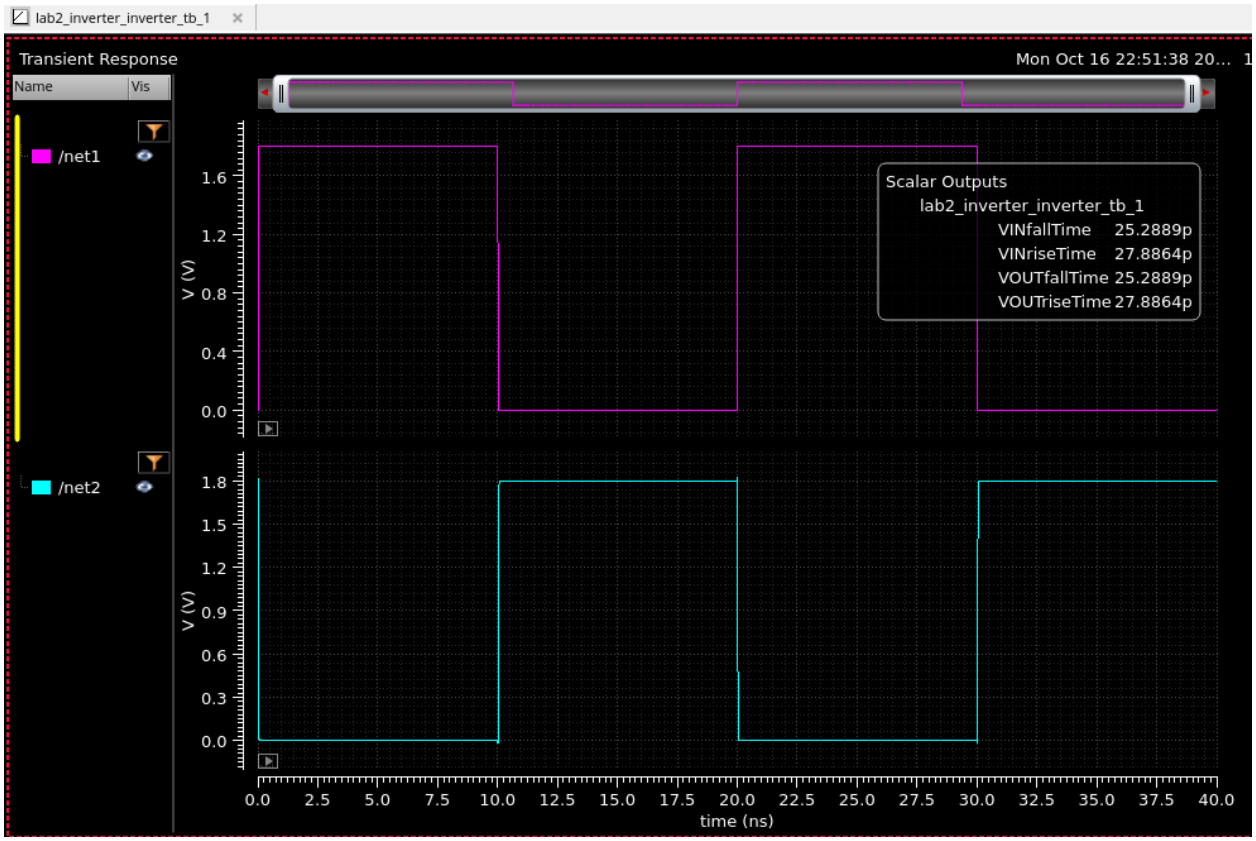
With asymmetric MOSFETs, the equations to find the noise margins grows in complexity. Estimating thresholds of 0.7V and equal electron mobilities (μ), VIL=0.667V_{out}-0.367 and VIH=1.333V_{out}+0.833.

Task 4:



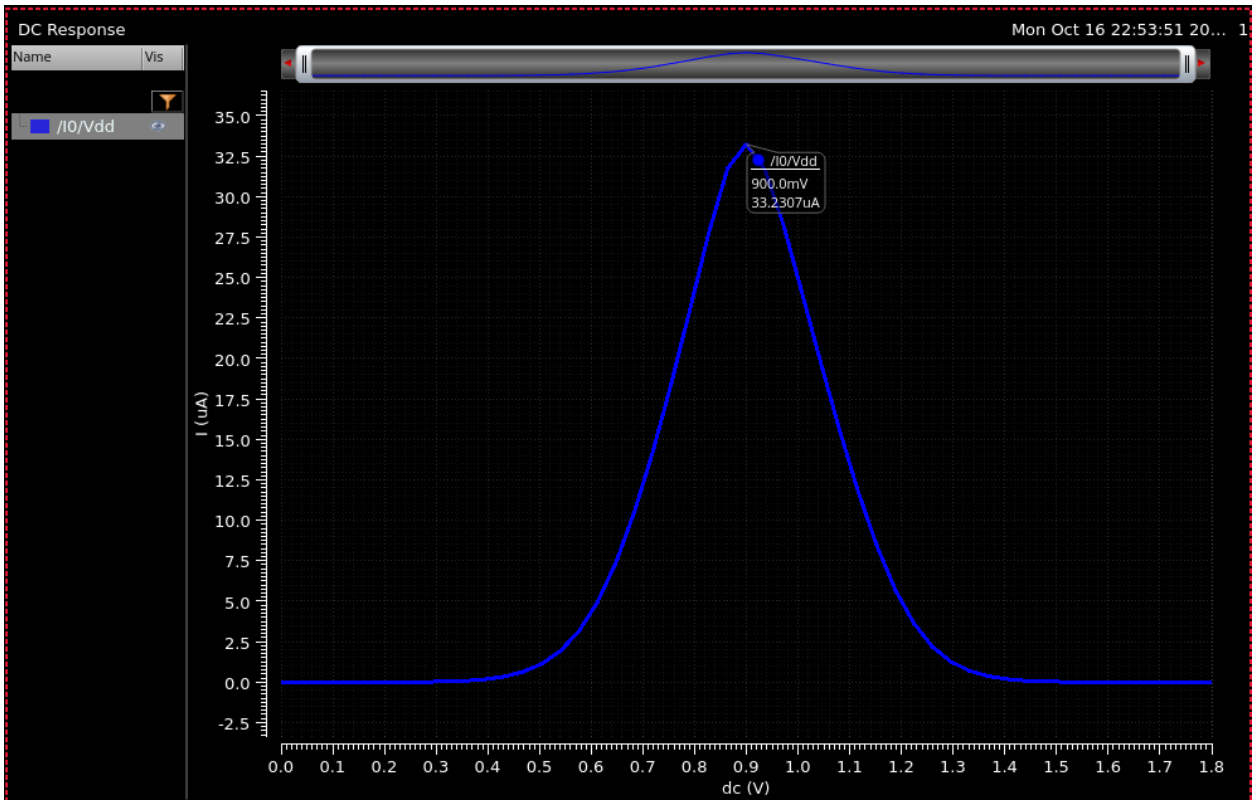
Different widths were simulated and plotted to find the optimal V_M. Further investigation narrowed down the search between 150nm and 180nm which led to a ideally symmetrical inverter with a pMOS with a length of 45nm and a width of 169.1874nm when paired with an nMOS 45nm long and 120nm wide.

Task 5:



Longer MOSFETs equate to longer rise and fall times.

Task 6:



At 0.9V, the current being drawn is 33 microamps. This equates to 29.7 microwatts.

Contributions

Both students contributed equal work by completing all tasks to show a comparison amongst values and results. All correspondence was once again conducted over Discord.

Challenges

Andrew - The challenges faced here included the calculations for the rising and falling times, as well as the power. These were quickly overcome by some quick research, and rewatching of the design jam post. Having started this sooner allowed for more time to make sure certain issues could be looked into effectively.

Nick - Faced connection issues for the second time in a row. This time while accessing the server from Babcock Hall so it wasn't anything VPN related. This could've been avoided by

completing the lab sooner. With access, more analysis could be completed and tasks 5 and 6 could have been finished.

Conclusion

Completing this lab led the students to gain more familiarity with the gpdk library. The students also learned how to create custom symbols that can be used in later labs along with designing testbenches to verify their results. To verify the results, each of the students completed the whole lab on their own and compiled and compared their results in transient and DC analyses. The design jam was very successful in leading the students through the lab.