University of New Hampshire
Department of Electrical and Computer Engineering
ECE 562 – Computer Organization
Fall 2019
Lab #5

Displaying Performance Information

In this assignment, you will improve your assembly programming skills by writing several procedures and learn more about assembly code organization, character encoding and displaying decimal numbers, performance monitoring facilities, measuring instruction latencies and the clock rate.

Step 1 – Prepare for the Lab

Make sure you download and read the `lab5.s`. You will also need `link.ld`, `ft232h.cfg` and `rpi3.cfg` files (unchanged from previous lab) installed in the same directory. The only difference in the `Makefile` is the addition of `lab5` to the list of labs and change of the default target from `lab4.ihex` to `lab5.ihex`. During download file names might change, e.g. `Makefile` might be renamed as `Makefile.txt`. Make sure to rename by running `mv Makefile.txt Makefile`.

Step 2 – Write the Assembly Code

Read the comments in `lab5.s` carefully and fill in your code. You will need to copy the procedures `gpio_configure_alternate_function`, `gpio_set_fsel`, `lcd_print`, `lcd_send`, `i2c_send_byte` from your Lab 4 code and make a change in the last one as instructed by the comments. You will also need to implement the `to_ascii` procedure according to the comments.

Step 3 – Emulation (optional)

(Same as previous labs).

Step 4 – Setup in the Lab

(Same as previous labs).

Step 5 – In the Lab

(Same as previous labs).

Step 6 – Report

Use the template `lab-template.docx` file from the course website to prepare a lab report. Once you make sure your code works, include the contents of the `to_ascii` procedure in your report.

Answer the following questions in your report:

Q1. Explain the purpose of using the following assembler directives in your own words: `.align`, `.skip`, `.8byte`, `.equiv`.

Q2. What is printed on the display? Include everything shown on the display. You can interrupt the program or adjust the delays to get a chance to copy it all down before the screen changes.

Q3. Why do you think we are using repeated measurements and picking the minimum, instead of average or maximum etc.? Do you think our methodology is sound?

Q4. Compare the latency of LDUR and STUR. How do you explain the difference?

Q5. How do the latencies of MUL and DIV compare when measuring a single instruction vs. measuring a loop? Could we infer from the difference that the processor is pipelined?

Q6. Why is the (minimum) latency for B.EQ so different than B? Could we infer from the difference that the processor is predicting the branch result?

Q7. Now that you know the actual processor frequency and the latency of one iteration of the loop, what is the real latency of `delay_half_second` from Lab #3 (assuming the loop is 64B-aligned)?

```
delay_half_second:
     SUB  X9, X9, X9
     ADDI X9, X9, #1
     LSL  X9, X9, #22
1:
     SUBI X9, X9, #1
     CBNZ X9, 1b
     BR   LR
```

Step 7 – Submit

Submit your report and `lab5.s` file online.