Lab 3: Layout Of An Inverter

ECE715: Introduction To VLSI

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Prepared For: Dr. MD Shaad Mahmud

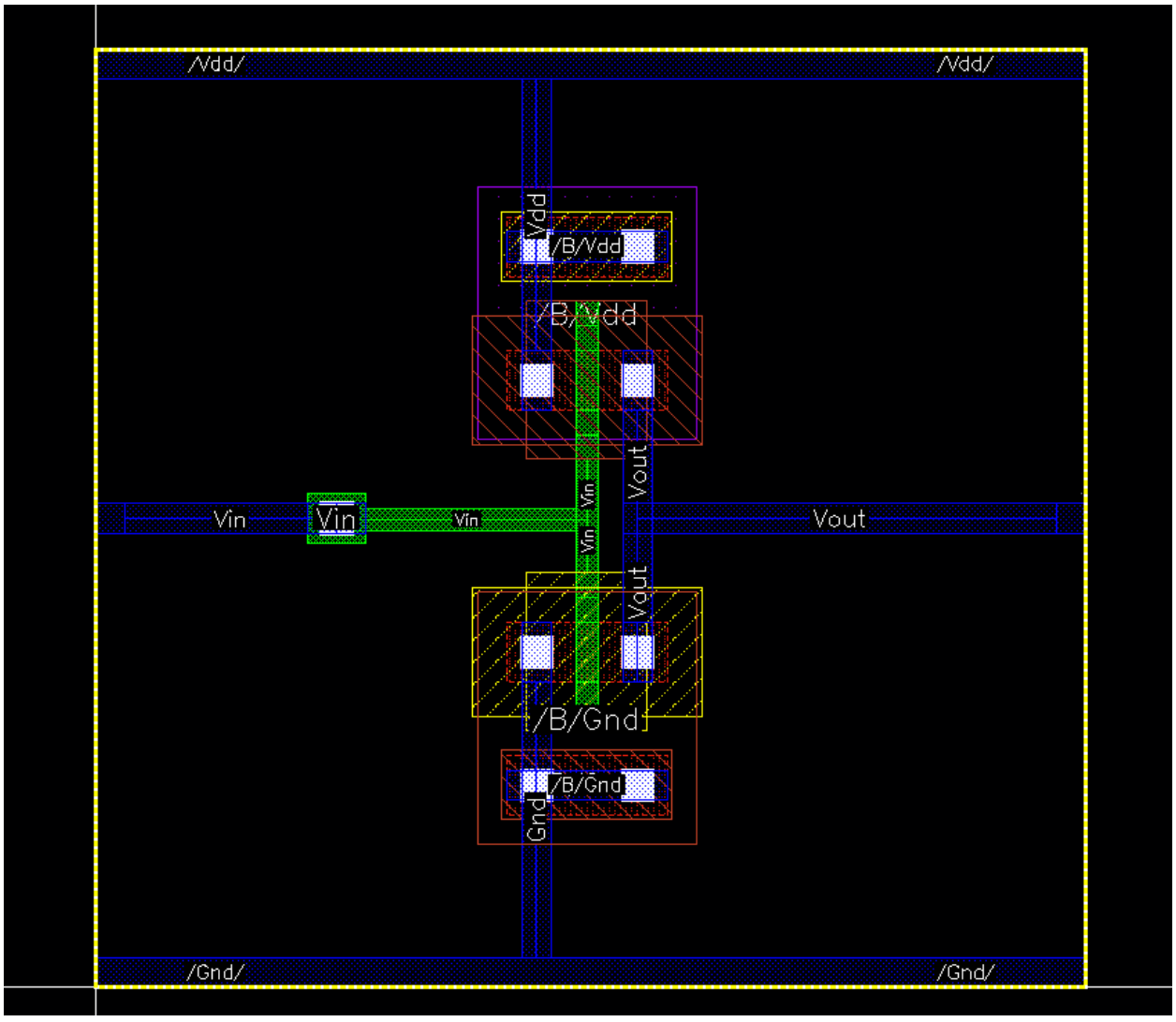
Due Date: 10/16/2023

Background

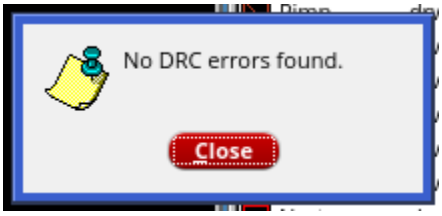
The main objective of this lab is to help students become familiar with all of the intricacies involved in layout design with Cadence Virtuoso. In addition to the general layout design, students will also gain experience using the gpdk045 layout checks such as LVS, DRC, QRC and the waveform signal. The concept of layout design is extremely useful for various design choices and will be utilized throughout the totality of the final project.

Lab Tasks

Task 2:

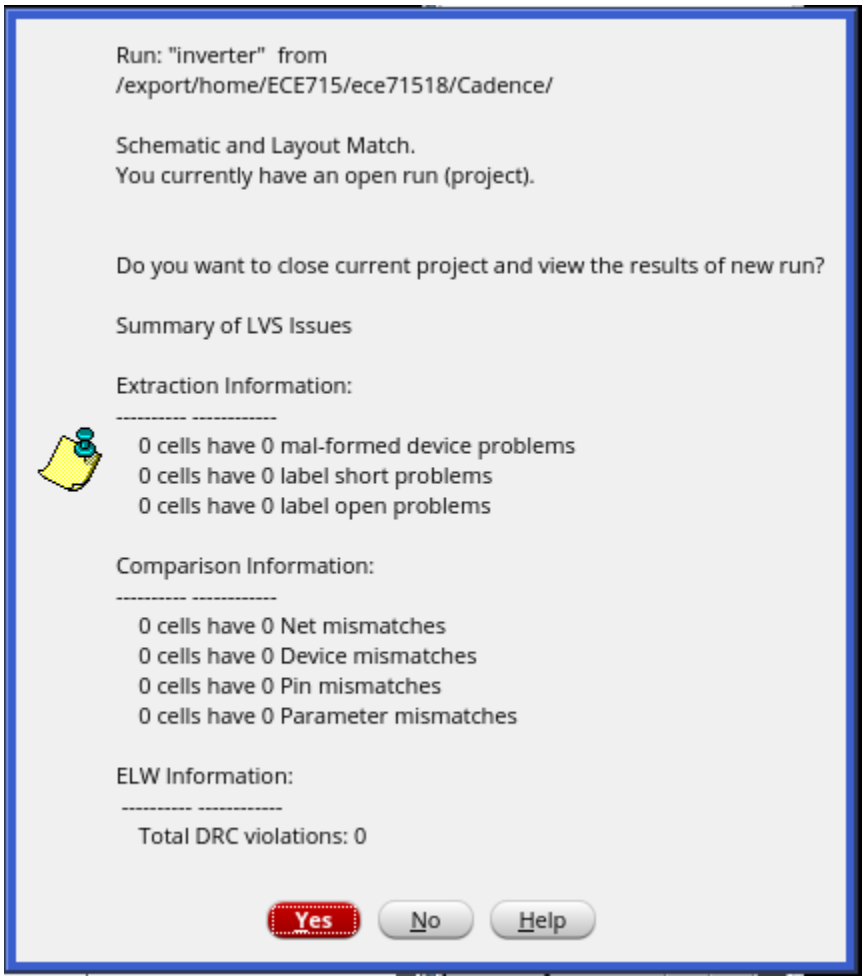


Task 3:



No DRC errors were found in the design

Task 4:



No LVS errors were found in the design

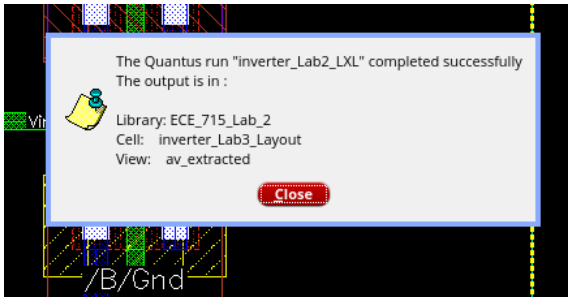
Task 5:

	time (s)	riseTime...me") (s)
1	10.02E-9	40.48E-12
2	30.02E-9	40.48E-12
3	50.02E-9	40.48E-12
4	70.02E-9	40.48E-12
5	90.02E-9	40.48E-12

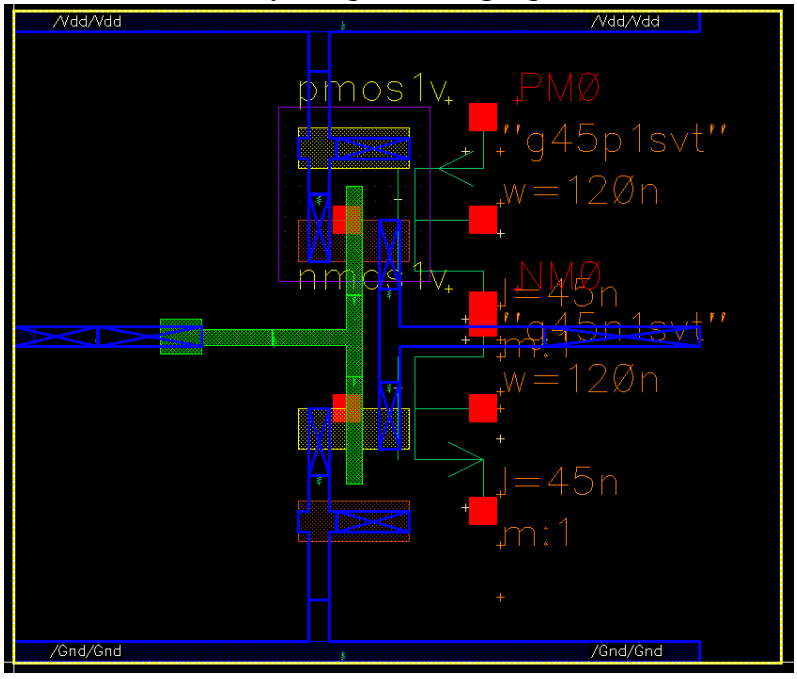
	time (s)	fallTime(...ime") (s)
1	9.681E-12	27.27E-12
2	20.01E-9	27.24E-12
3	40.01E-9	27.24E-12
4	60.01E-9	27.24E-12
5	80.01E-9	27.24E-12

The tpLH and tpHL values for Vout from the inverter without the QRC simulation was 25.2 picoseconds, while the values from the QRC simulation were 40.48 picoseconds for tpLH and 27.27 picoseconds for tpHL.

Appendix:



Results of the QRC through Quantus.



The QRC process combines the layout with the schematic producing an extracted layout titled an ‘av_extracted’ file which allows for more realistic calculations and simulations which are shown below with the waveform.

```
Circuit inventory:
                 nodes 18
                 bsim4 2
      bsource_2b273e 2
              capacitor 14
               resistor 13
                vsource 2
```

Proof of a working simulation with the extracted layout.

The waveform produced by using the config file with an 'av_extracted' file

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Challenges

Andrew The main challenge faced was working with the QRC through Quantus. When trying to assemble the config file the av extracted file was not present which led to it being copied over to the correct view.

Nick: The only challenges faced were slow response time from the server when in class during the design jam. The video posted later was very easy to follow along and add the correct technology files to complete the DRC and LVS checks.

Contributions

Andrew

Andrew took care of the Background section and contributions sections of the lab report. In addition Andrew also did the QRC, waveform simulation, and the comparison of the tpHL and the tpLH from the design in lab-2.

Nick

Nick took care of the conclusion section of the lab report. In addition Nick also did the DRC and LVS checks as well.

Conclusion

This lab taught both Andrew and Nick valuable information regarding the design of a layout in Cadence. Considerations like following Design Rule Checks and Layout Vs Schematics are crucial to implementing a design onto a silicon wafer.