ECE 543: Introduction to Digital Systems

Homework #5

Due: Friday, December 10th, 2021 (6 P.M.)

Student Name: _____

Note:
- **Please use these sheets as cover pages.**
- **Your work must be hand-written (no typing please).**
- **Homework must be submitted electronically through Canvas in a PDF format.**

Part #1: Solve the following problems.

1. (a) Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.

   (b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares.

2. Design a synchronous, recycling, MOD-5 down counter that produces the sequence 100, 011, 010, 001, 000, and repeat. Use J-K flip-flops. Force the unused states to 000 on the next clock pulse.

3. Design a synchronous, recycling, MOD-7 up/down counter with J-K FFs. Use the states 000 through 110 in the counter. Control the count direction with input D (D = 0 to count up and D = 1 to count down).
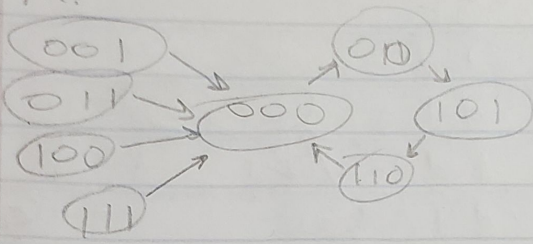
Part #2: Solve the following problems from "Fundamentals of Digital Logic with Verilog Design" by Brown & Vranesic (3rd Edition).
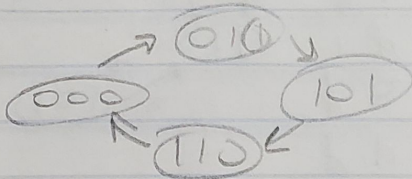
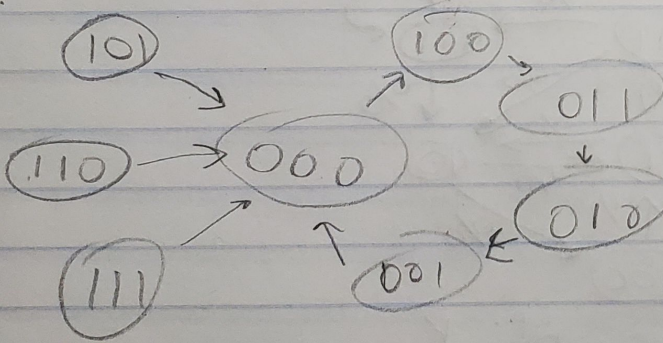Problems from Chapter 6:
6.3, 6.5, 6.15

1a.

Present state	Next state	FF2	FF1	FF0
$Q_2 Q_1 Q_0$	$Q_2' Q_1' Q_0'$	JK	JK	JK
0 0 0	0 1 0	0 d	1 d	0 d
0 0 1	0 0 0	0 d	0 d	d 1
0 1 0	1 0 1	1 d	d 1	1 d
0 1 1	0 0 0	0 d	d 1	d 1
1 0 0	0 0 0	d 1	0 d	0 d
1 0 1	1 1 0	d 0	1 d	d 1
1 1 0	0 0 0	d 1	d 1	0 d
1 1 1	0 0 0	d 1	d 1	d 1

1b.

$Q_2 Q_1 Q_0$	$Q_2' Q_1' Q_0'$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
0 0 0	0 1 0	0 d	1 d	0 d
0 0 1	d d d	dd	dd	dd
0 1 0	1 0 1	1 d	d 1	1 d
0 1 1	d d d	dd	dd	dd
1 0 0	d d d	dd	dd	dd
1 0 1	1 1 0	d 0	1 d	d 1
1 1 0	0 0 0	d 1	d 1	0 d
1 1 1	d d d	dd	dd	dd

2.

$Q_2 Q_1 Q_0$	$Q_2' Q_1' Q_0'$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
0 0 0	1 0 0	1 d	0 d	0 d
0 0 1	0 0 0	0 d	0 d	d 1
0 1 0	0 0 1	0 d	d 1	1 d
0 1 1	0 1 0	0 d	d 0	d 1
1 0 0	0 1 1	d 1	1 d	1 d
1 0 1	0 0 0	d 1	0 d	d 1
1 1 0	0 0 0	d 1	d 1	0 d
1 1 1	0 0 0	d 1	d 1	d 1

D Q_4Q_3 Q_2Q_1 Q_2 J_{K_2} J_{K_1} J_{K_0}

0 0 0 0   0 0 0   0 0   0 0 1 d
0 0 0 1   0 0 1   0 d   0 1 d   1 d
0 0 1 0   0 1 0   0 d   1 d   d 1
0 0 1 1   0 0 0   0 d   d 1   d 1
0 1 0 0   1 0 1   1 d   d 0   0 d
0 1 0 1   1 1 0   d d   0 d   1 d
0 1 1 0   0 1 0   d d   d 0   0 d
0 1 1 1   d d d   d d d   d d d
1 0 0 0   0 1 1   0 d   1 d   1 d
1 0 0 1   1 0 0   d 1   0 d   0 d
1 0 1 0   0 1 1   d 1   d 0   1 d
1 0 1 1   1 0 1   d 0   d 1   0 d
1 1 0 0   1 1 1   d 0   d 0   1 d
1 1 0 1   1 0 0   d 0   d 1   d 1
1 1 1 0   1 0 1   d 0   0 d   d 1
1 1 1 1   d d d   d d d   d d d

6.3

6.5 W Q_1Q_0 $Q_1'Q_0'$ Y

0 0 0   0 0 0   0
0 0 1   0 0 0   0
0 1 0   0 1 0   0
0 1 1   0 1 0   0
1 0 0   0 0 1   0
1 0 1   0 0 1   0
1 1 0   1 1 0   0
1 1 1   1 1 0   1

6.15

	Present state	Next state	output
00	0001	0100 1000	0
01	0010	0010 0001	0
10	0100	1000 0001	0
11	1000	0100 0010	1